MCP Specification

4Gb SLC NAND Flash (X8) + 4Gb LPDDR3 (X32)

4Gb SLC NAND Flash (X8) + 8Gb LPDDR3 (X32)

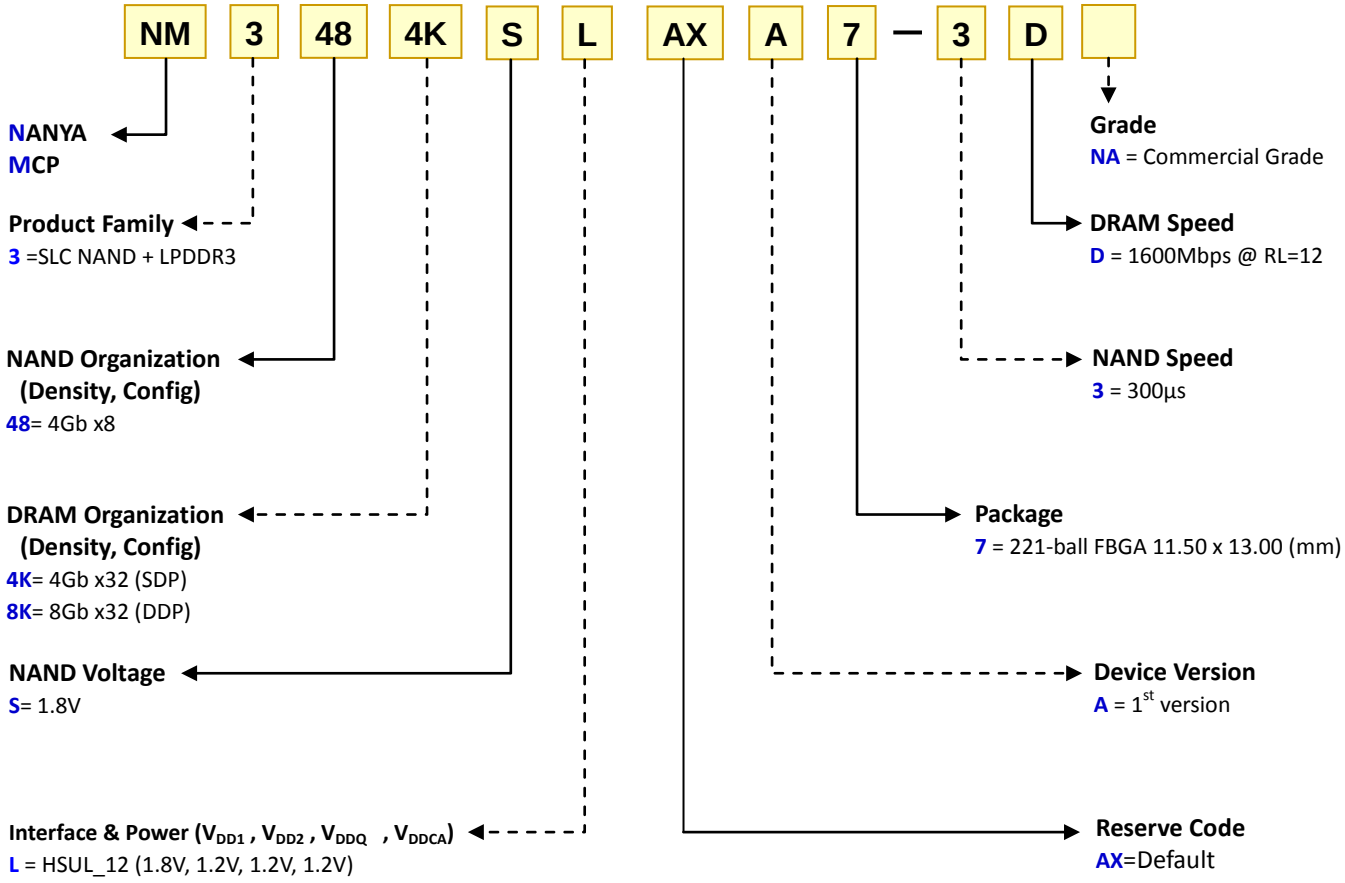
Preliminary Version 1.2

Nanya Technology Corporation

Ordering Information

MCP		NAND				DRAM			
Part Number	Package	Type	Density (Org.)	Program Time	Erase Time	Type	Density (Org.)	Speed	RL
NM3484KSLAXA7-3D	221b FBGA(-7)	SLC	4Gb (512Mb X 8)	300µs	3.5ms	LPDDR3	4Gb (X32, SDP)	1600 Mbps	12
NM3488KSLAXA7-3D	221b FBGA(-7)	SLC	4Gb (512Mb X 8)	300µs	3.5ms	LPDDR3	8Gb (X32, DDP)	1600 Mbps	12

NANYA MCP Part Numbering Guide



Features

MCP

- **Separate SLC NAND and LPDDR3 RAM interfaces**
- **Lead-free (RoHS compliant) and Halogen-free Package :** 221-ball FBGA (11.50mm x 13.00mm x 1.00mm)
- **Operating temperature range:** –25°C to +85°C

4Gb X8 SLC NAND

- **Voltage Supply(VCC/VCCQ): 1.70V ~ 1.95V**
- **Organization**
  - X8 Memory Cell Array: 4352 x 128K x 8
  - X8 Data Register: 4352 x 8
  - X8 Page Program: 4352 Bytes
  - X8 Block Erase: (256K + 16K) Bytes
- **Modes**

  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy, Multi Page Program, Multi Block Erase, Multi Page Copy, Multi Page Read
- **Mode control**
  - Serial input/output
  - Command control
- **Number of valid blocks**
  - Min 2008 blocks
  - Max 2048 blocks
- **Access time**
  - Cell array to register: 25µs max
  - Serial Read Cycle: 25ns min (CL=30pF)
- **Program/Erase time**
  - Auto Page Program: 300µs/page typical
  - Auto Block Erase: 3.5ms/block typical
- **Operating current**
  - Read (25ns cycle): 30 mA max
  - Program (avg.): 30 mA max
  - Erase (avg.): 30 mA max
  - Standby: 50 µA max
- **8 bit ECC for each 512 Bytes is required.**

4Gb(SDP)/8Gb(DDP) X32 LPDDR3

- **Speed, Addressing and Retention Specification**

Organization	128Mb X32
Speed Grade	1600 / RL=12
Number of Banks	8
CA	CA[9:0]
Bank Address	BA[2:0]
Row	R[13:0]
Column	C[9:0]
tREFI (us)	3.9

- **Basis LPDDR3 Compliant**
  - Low Power Consumption
  - 8n Prefetch Architecture and BL8 only
- **HSUL12 interface and Power Supply**
  - VDD1= 1.70 to 1.95V
  - VDD2/VDDQ/VDDCA = 1.14 to 1.3V
- **Signal Integrity**
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240Ω± 1%)
- **Training for Signals' Synchronization**
  - DQ Calibration offering specific DQ output patterns
  - CA Training
  - Write Leveling via MR settings
- **Data Integrity**
  - DRAM built-in Temperature Sensor for Temperature Compensated Self Refresh (TCSR)
  - Auto Refresh and Self Refresh Modes
- **Power Saving Modes**
  - Deep Power Down Mode (DPD)
  - Partial Array Self Refresh (PASR)
  - Clock Stop capability during idle period
- **Programmable Function**
  - RON (Typical: 34.3/40/48/60/80)
  - RON (Typical: 34.3/40/48/60/80)
  - RTT (120/240)
  - RL/WL Select (Set A / Set B)
  - nWRE (nWR≤9 / nWR>9)
  - PASR (bank / segment)

221b Ball Assignment – Flash X8 + DRAM X32(SDP)

Part Number: NE3484KALAXA7-XXX

Top View, A1 in Top Left Corner

•	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DNU	DNU	RFU	$\overline{CE}$	$\overline{WP}$	CLE	VSS	VCC	ALE	$\overline{WE}$	R/$\overline{B}$	RFU	DNU	DNU
B	DNU	VSS	NC	NC	VSS	I/O 0	I/O 1	I/O 4	I/O 5	VSS	NC	NC	VSS	DNU
C		VCC	NC	NC	VCC	I/O 2	I/O 3	I/O 6	I/O 7	VCC	NC	NC	VCC	
D		RFU	RFU	RFU	RFU	$\overline{RE}$	VCC	VSS						
E														
F		VSS	VDD1	VDD1	VDD2			VDD2	VDD1	DQ29	DQ30	DQ31	VSS	
G		ZQ	NC	VSS	VDD1			VSS	VDDQ	DQ26	VSS	DQ27	DQ28	
H		CA9	VSS	VSS	VSS			VDDQ	DQS3	VSS	DQ24	VDDQ	DQ25	
J		CA8	CA7	VSS	VDD2			VSS	$\overline{DQS3}$	DM3	VDDQ	DQ15	VSS	
K		VDDCA	CA6	VSS	VDD2			VSS	VSS	VDDQ	DQ13	VDDQ	DQ14	
L		VDD2	CA5	VSS	VDD2			VDDQ	VDDQ	VSS	DQ12	VSS	DQ11	
M		VREFCA	VSS	VSS	VDD2			VSS	DQS1	VDDQ	DQ10	VDDQ	DQ9	
N		VDDCA	$\overline{CK}$	VSS	VDD2			VSS	$\overline{DQS1}$	DM1	VDDQ	DQ8	VSS	
P		VSS	CK	VSS	VDD2			VDD2	VSS	ODT	VDD2	VSS	VREFDQ	
R		NC	VSS	VSS	VDD2			VSS	$\overline{DQS0}$	DM0	VDDQ	DQ7	VSS	
T		CKE	NC	VSS	VDD2			VSS	DQS0	VDDQ	DQ5	VDDQ	DQ6	
U		VDDCA	$\overline{CS}$	VSS	VDD2			VDDQ	VDDQ	VSS	DQ3	VSS	DQ4	
V		VDDCA	CA4	VSS	VDD2			VSS	VSS	VDDQ	DQ1	VDDQ	DQ2	
W		CA2	CA3	VSS	VDD2			VSS	$\overline{DQS2}$	DM2	VDDQ	DQ0	VSS	
Y		CA0	CA1	VSS	VSS			VDDQ	DQS2	VSS	DQ23	VDDQ	DQ22	
AA	DNU	VSS	VDD1	VSS	VDD1			VSS	VDDQ	DQ21	VSS	DQ20	DQ19	DNU
AB	DNU	DNU	VDD1	VDD1	VDD2			VDD2	VDD1	DQ18	DQ17	DQ16	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

221b Ball Assignment – Flash X8 + DRAM X32(DDP)

Part Number: NE3488KALAXA7-XXX

Top View, A1 in Top Left Corner

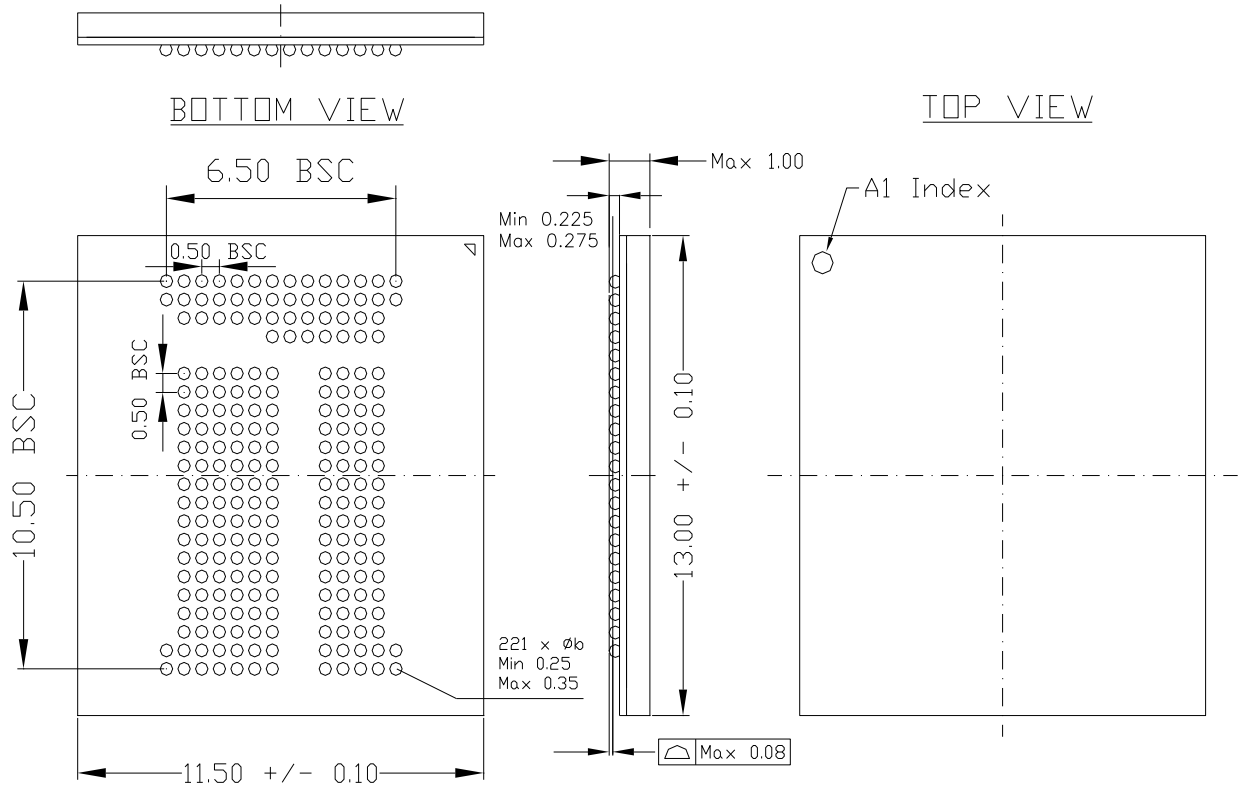
•	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DNU	DNU	RFU	$\overline{CE}$	$\overline{WP}$	CLE	VSS	VCC	ALE	$\overline{WE}$	R/$\overline{B}$	RFU	DNU	DNU
B	DNU	VSS	NC	NC	VSS	I/O 0	I/O 1	I/O 4	I/O 5	VSS	NC	NC	VSS	DNU
C		VCC	NC	NC	VCC	I/O 2	I/O 3	I/O 6	I/O 7	VCC	NC	NC	VCC	
D		RFU	RFU	RFU	RFU	$\overline{RE}$	VCC	VSS						
E														
F		VSS	VDD1	VDD1	VDD2			VDD2	VDD1	DQ29	DQ30	DQ31	VSS	
G		ZQ	NC	VSS	VDD1			VSS	VDDQ	DQ26	VSS	DQ27	DQ28	
H		CA9	VSS	VSS	VSS			VDDQ	DQS3	VSS	DQ24	VDDQ	DQ25	
J		CA8	CA7	VSS	VDD2			VSS	$\overline{DQS3}$	DM3	VDDQ	DQ15	VSS	
K		VDDCA	CA6	VSS	VDD2			VSS	VSS	VDDQ	DQ13	VDDQ	DQ14	
L		VDD2	CA5	VSS	VDD2			VDDQ	VDDQ	VSS	DQ12	VSS	DQ11	
M		VREFCA	VSS	VSS	VDD2			VSS	DQS1	VDDQ	DQ10	VDDQ	DQ9	
N		VDDCA	$\overline{CK}$	VSS	VDD2			VSS	$\overline{DQS1}$	DM1	VDDQ	DQ8	VSS	
P		VSS	CK	VSS	VDD2			VDD2	VSS	ODT	VDD2	VSS	VREFDQ	
R		CKE1	VSS	VSS	VDD2			VSS	$\overline{DQS0}$	DM0	VDDQ	DQ7	VSS	
T		CKE0	$\overline{CS1}$	VSS	VDD2			VSS	DQS0	VDDQ	DQ5	VDDQ	DQ6	
U		VDDCA	$\overline{CS0}$	VSS	VDD2			VDDQ	VDDQ	VSS	DQ3	VSS	DQ4	
V		VDDCA	CA4	VSS	VDD2			VSS	VSS	VDDQ	DQ1	VDDQ	DQ2	
W		CA2	CA3	VSS	VDD2			VSS	$\overline{DQS2}$	DM2	VDDQ	DQ0	VSS	
Y		CA0	CA1	VSS	VSS			VDDQ	DQS2	VSS	DQ23	VDDQ	DQ22	
AA	DNU	VSS	VDD1	VSS	VDD1			VSS	VDDQ	DQ21	VSS	DQ20	DQ19	DNU
AB	DNU	DNU	VDD1	VDD1	VDD2			VDD2	VDD1	DQ18	DQ17	DQ16	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

221b Package Outline Drawing (11.50mm x 13.00mm x 1.00mm)

Might be changed before it's finalized

Unit: mm

* BSC (Basic Spacing between Center)



Ball Description - 4Gb X8 SLC NAND

Symbol	Type	Function
X8: **I/O[7:0]**	Input/output	**Data Bus:** The I/O0 to 7 pins are used as a port for transferring address, command and input/output data to and from the device.
CLE	Input	**Command Latch Enable:** The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.
ALE	Input	**Address Latch Enable:** The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O ports on the rising edge of $\overline{WE}$ while ALE is High.
$\overline{CE}$	Input	**Chip Enable:** The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state (RY / $\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.
$\overline{RE}$	Input	**Read Enable:** The $\overline{RE}$ signal controls serial data output. Data is available tREA after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address = Address +1) on this falling edge.
$\overline{WE}$	Input	**Write Enable:** The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.
$\overline{WP}$	Input	**Write Protect:** The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used protecting the data during the power-on/off sequence when input signals are invalid.
RY/$\overline{BY}$	Output	**Ready / Busy Output:** The RY / $\overline{BY}$ output signal is used to indicate the operation condition of the device. The RY / $\overline{BY}$ signal is in Busy state (RY / $\overline{BY}$ =L) during the Program, Erase and Read operations and will return to Ready state (RY / $\overline{BY}$ =H) afeter completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to Vccq with an appropriate resister. If RY / $\overline{BY}$ signal is not pulled-up to Vccq (“Open” state), device operation cannot guarantee.
VCC	Supply	**Power**
VSS	Supply	**Ground**
NC	—	**No Connect:** These pins should be left unconnected.

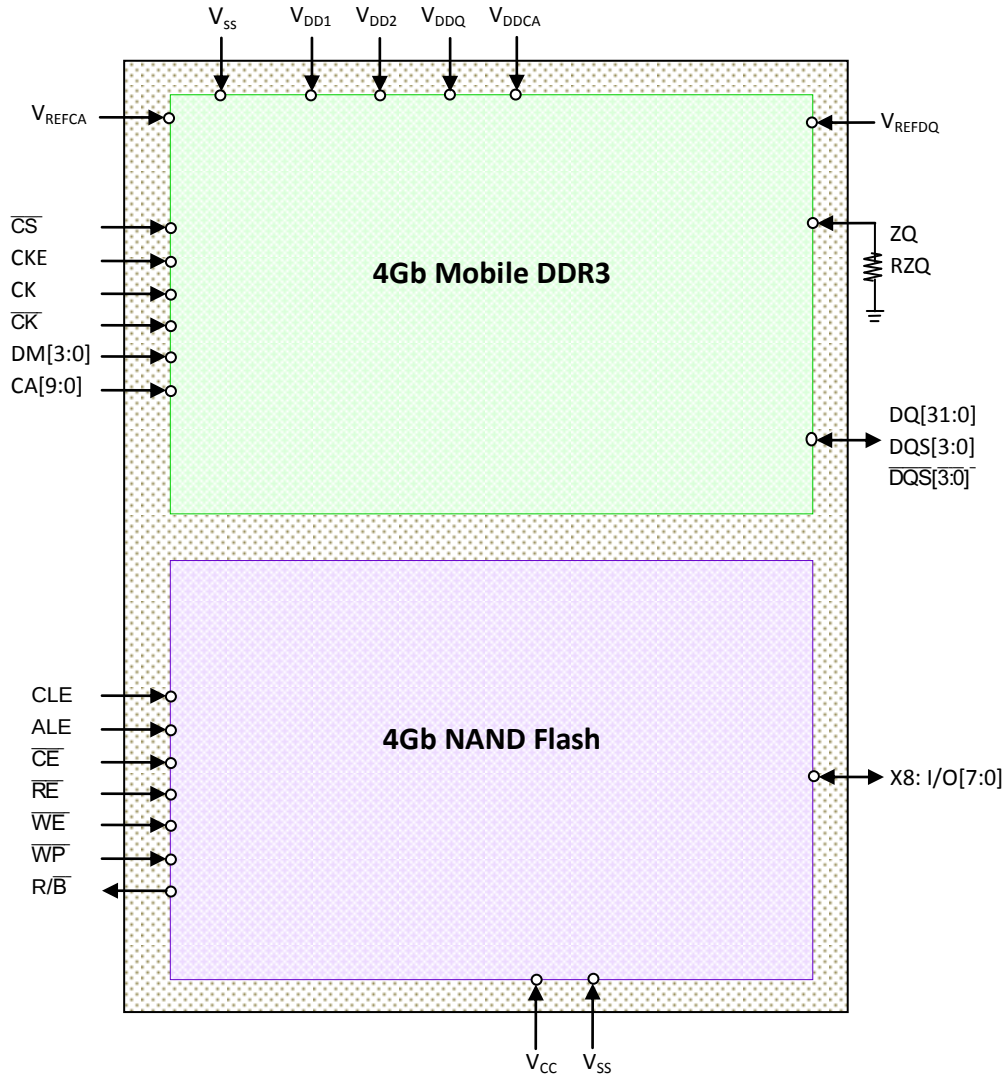
Ball Description - 4Gb(SDP)/8Gb(DDP) X32 LPDDR3

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, $\overline{CS}$ and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK and $\overline{CK}$. The positive Clock edge is defined by the crosspoint of a rising CK and a falling $\overline{CK}$. The negative Clock edge is defined by the crosspoint of a falling CK and a rising $\overline{CK}$.
CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
$\overline{CS0}$, $\overline{CS1}$	Input	**Chip Select:** $\overline{CS}$ is considered part of the command code. See Command Truth Table for command code descriptions. $\overline{CS}$ is sampled at the positive Clock edge.
CA[9:0]	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
DM[3:0]	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS (or $\overline{DQS}$). For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
DQ[31:0]	Input/output	**Data Inputs/Output:** Bi-directional data bus
DQS,$\overline{DQS}$ DQS[3:0], $\overline{DQS}$[3:0]	Input/output	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS and $\overline{DQS}$). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x32 DQS0 and $\overline{DQS0}$ correspond to the data on DQ0 - DQ7, DQS1 and $\overline{DQS1}$ to the data on DQ8 - DQ15, DQS2 and $\overline{DQS2}$ to the data on DQ16 - DQ23, DQS3 and $\overline{DQS3}$ to the data on DQ24 - DQ31.
ODT	Input	On-Die Termination**:** This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.
ZQ	Reference	**External Reference ball for ZQ Calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SS}.

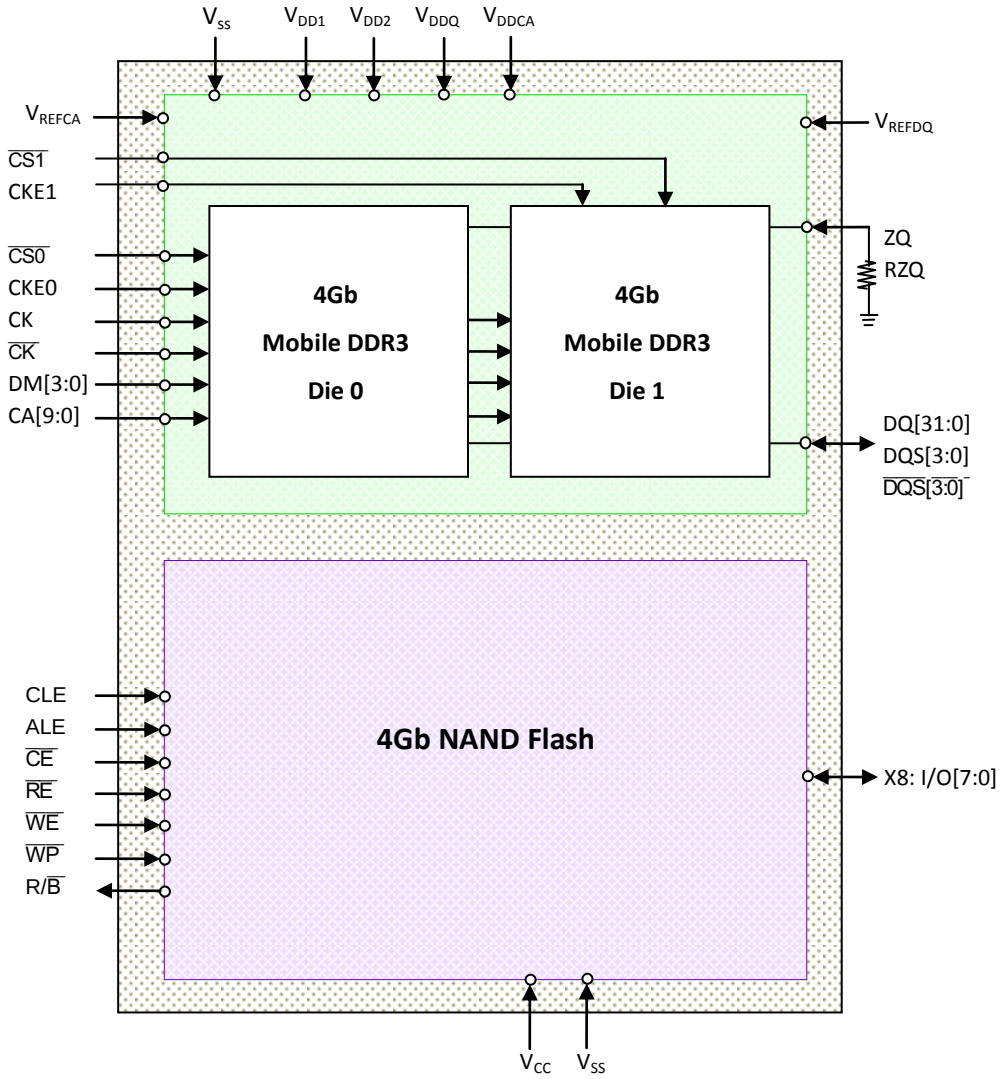
Symbol	Type	Function
V_{DD1}	Supply	**Core Power Supply 1:** Core power supply
V_{DD2}	Supply	**Core Power Supply 2:** Core power supply
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, $\overline{CS}$, CK, and $\overline{CK}$ input buffers.
V_{REFCA}	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9 CKE, $\overline{CS}$, CK, and $\overline{CK}$ input buffers.
V_{REFDQ}	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all data input buffers.
V_{SS}	Supply	**Ground**
NC	-	**No Connect: No internal electrical connection is present.**

NOTE 1: The signal may show up in a different symbol but it indicates to the same thing. e.g., /CK = CK# = $\overline{CK}$ = CKb = CK_n = CK_c, /DQS = DQS# = $\overline{DQS}$ = DQSb = DQS_n = DQS_c, /CS = CS# = $\overline{CS}$ = CSb = CS_n.

Functional Block Diagram (4Gb SLC NAND + 4Gb LPDDR3)



Functional Block Diagram (4Gb SLC NAND + 8Gb LPDDR3)



4Gb(X8) SLC NAND Flash

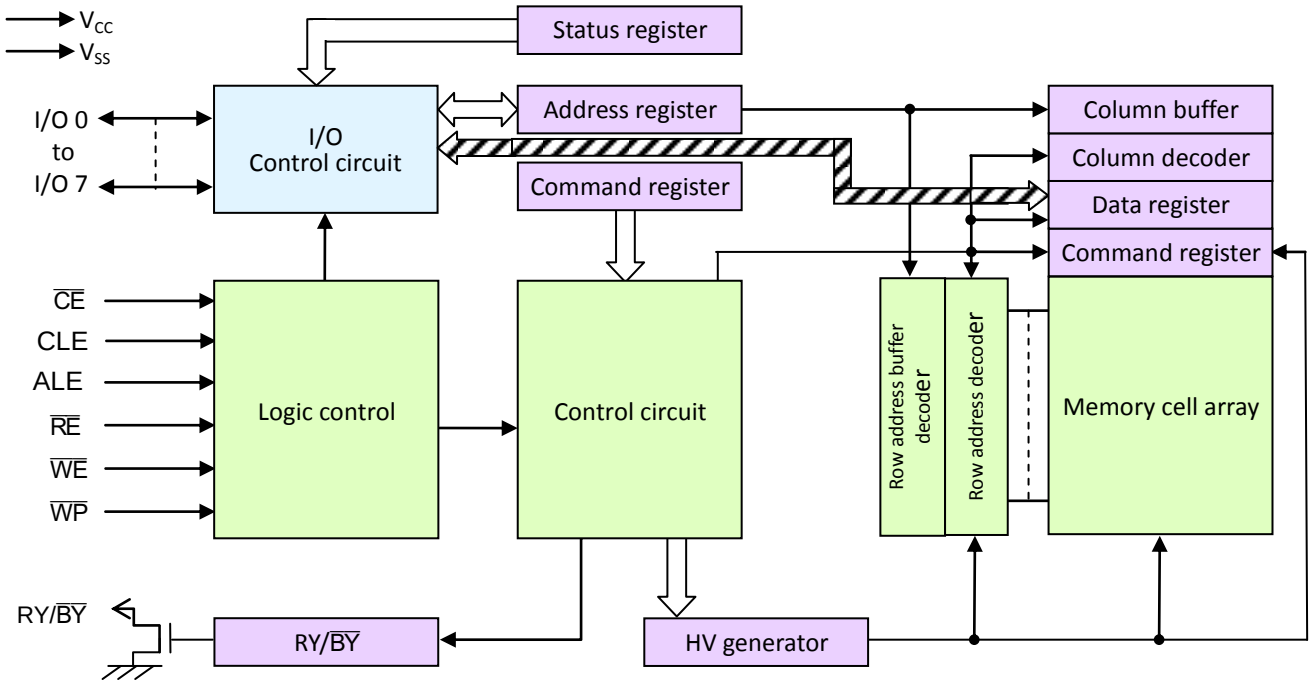
Descriptions

The device is a single 1.8V 4Gbit (4,563,402,752 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^2PROM) organized as X8: (4096 +256) bytes x 64 pages x 2048 blocks.

The device has 4352-bytes static registers which allow program and read data to be transferred between the register ad the memory cell array in 4352-bytes increments. The Erase operation is implemented in a single block unit (X8=256 Kbytes + 16 Kbytes: 4352 bytes x 64 pages).

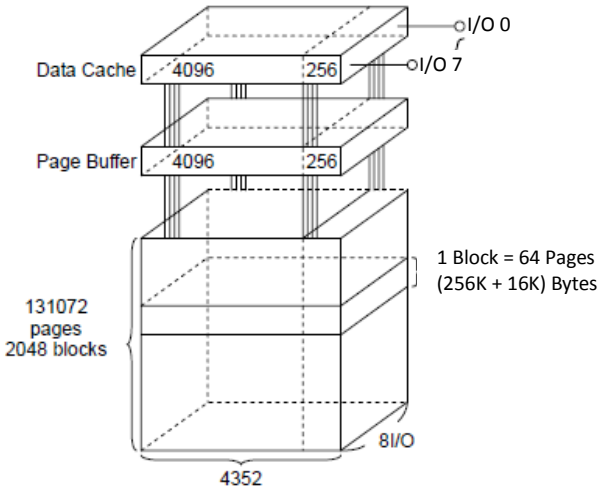
The device is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

Function Block Diagram (X8)



Array Organization (X8)

The Program operation works on page units while the Erase operation works on block units



A page consists of 4352 bytes in which 4096 bytes are used for main memory storage and 256 bytes are for redundancy or for other uses.
1 Page = 4352 Bytes
1 Block = 4352 Bytes x 64 Pages = (256K + 16K) Bytes
Capacity = 4352 Bytes x 64 Pages x 2048 Blocks

Array Address (X8)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1st cycle	CA_0	CA_1	CA_2	CA_3	CA_4	CA_5	CA_6	CA_7	Column Address
2nd cycle	CA_8	CA_9	CA_{10}	CA_{11}	CA_{12}	L	L	L	Column Address
3rd cycle	PA_0	PA_1	PA_2	PA_3	PA_4	PA_5	PA_6	PA_7	Page Address
4th cycle	PA_8	PA_9	PA_{10}	PA_{11}	PA_{12}	PA_{13}	PA_{14}	PA_{15}	Page Address
5th cycle	PA_{16}	L	L	L	L	L	L	L	Page Address

PA6 to PA16: Block address
PA0 to PA5: NAND address in block

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	-0.6 to +2.5	V
V_{IN}	Input Voltage	-0.6 to +2.5	
$V_{I/O}$	Input / Output Voltage	-0.6 to Vcc + 0.3 (≤2.5V)	
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	-55 to +125	°C

Capacitance[1]

(T_A=25℃, f=1.0MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input	V_{IN}=0V	–	10	pF
C_{OUT}	Output	V_{OUT}=0V	–	10	pF

NOTE 1 This parameter is periodically sampled and is not tested for every device.

Valid Blocks

Symbol	Parameter	Min	Typ.	Max	Unit
N_{VB}	Number of Valid Blocks	2,008	–	2,048	Blocks

NOTE 1 The device occasionally contains unusable blocks.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime.
The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
V_{CC}	Power Supply Voltage	1.70	–	1.95	V
V_{IH}	High Level Input Voltage	V_{CC} x 0.8	–	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	-0.3[1]	–	V_{CC} x 0.2	V

Note 1 -2V (pulse width lower than 20 ns)

DC and Operation Characteristics

(Ta= -25 to 85℃, V_{CC}=1.70 to 1.95V)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_{IL}	Input Leakage Current	V_{IN}=0 to V_{CC}	–	–	±10	µA
I_{LO}	Output Leakage Current	V_{OUT}=0 to V_{CC}	–	–	±10	µA
I_{CCO1}	Serial Read Current	$\overline{CE}$=V_{IL},I_{OUT}= 0 mA, tcycle=25ns	–	–	30	mA
I_{CCO2}	Programming Current	–	–	–	30	mA
I_{CCO3}	Erasing Current	–	–	–	30	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} - 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	–	–	50	µA
V_{OH}	High Level Output Voltage	I_{OH} = -0.1mA	V_{CC} - 0.2	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1mA	–	–	0.2	V
I_{OL} (RY/$\overline{BY}$)	Output Current of (RY/$\overline{BY}$) pin	V_{OL}=0.2V	–	4	–	mA

AC Timing Characteristics for Command / Address / Data Input

(Ta= -25 to 85℃, V_{CC}=1.70 to 1.95V)

Symbol	Parameter	Min	Max	Unit
tCLS	CLE Setup Time	12	–	ns
tCLH	CLE Hold Time	5	–	ns
tCS	$\overline{CE}$ Setup Time	20	–	ns
tCH	$\overline{CE}$ Hold Time	5	–	ns
tWP	Write Pulse Width	12	–	ns
tALS	ALE Setup Time	12	–	ns
tALH	ALE Hold Time	5	–	ns
tDS	Data Setup Time	12	–	ns
tDH	Data Hold Time	5	–	ns
tWC	Write Cycle Time	25	–	ns
tWH	$\overline{WE}$ High Hold Time	10	–	ns

AC Characteristics for Operation

Symbol	Parameter	Min	Max	Unit
tWW	$\overline{WP}$ High to $\overline{WE}$ Low	100	–	ns
tRR	Ready to $\overline{RE}$ Falling Edge	20	–	ns
tRW	Ready to $\overline{WE}$ Falling Edge	20	–	ns
tRP	Read Pulse Width	12	–	ns
tRC	Read Cycle Time	25	–	ns
tREA	$\overline{RE}$ Access Time	–	20	ns
tCEA	$\overline{CE}$ Access Time	–	25	ns
tCLR	CLE Low to $\overline{RE}$ Low	10	–	ns
tAR	ALE Low to $\overline{RE}$ Low	10	–	ns
tRHOH	$\overline{RE}$ High to Output Hold Time	25	–	ns
tRLOH	$\overline{RE}$ Low to Output Hold Time	5	–	ns
tRHZ	$\overline{RE}$ High to Output High Impedance	–	60	ns
tCHZ	$\overline{CE}$ High to Output High Impedance	–	20	ns
tCSD	$\overline{CE}$ High to ALE or CLE Don't care	0	–	ns
tREH	$\overline{RE}$ High Hold Time	10	–	ns
tIR	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	–	ns
tRHW	$\overline{RE}$ High to $\overline{WE}$ Low	30	–	ns
tWHC	$\overline{WE}$ High to $\overline{CE}$ Low	30	–	ns
tWHR	$\overline{WE}$ High to $\overline{RE}$ Low	60	–	ns
tR	Memory Cell Array to Starting Address	–	25	µs
tDCBSYR1	Data Cache Busy in Read Cache (following 31h and 3Fh)	–	25	µs
tDCBSYR2	Data Cache Busy in Page Copy (following 3Ah)	–	30	µs
tWB	$\overline{WE}$ High to Busy	–	100	ns
tRST	Device Reset Time (Ready/Read/Program/Erase)	–	5/5/10/500	µs

NOTE 1 tCLS and tALS cannot be shorter than tWP.

NOTE 2 tCS should be longer than tWP + 8ns.

AC Test Condition

Parameter	Condition
	VCC : 1.70 to 1.95V
Input level	VCC – 0.2 V, 0.2 V
Input pulse rise and fall time	3ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output Load	CL (30 pF) + 1 TTL

NOTE 1 Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.

Programming / Erasing Characteristics

(Ta= -25 to 85℃, V_{CC}=1.70 to 1.95V)

Symbol	Parameter	Min	Typ.	Max	Unit
tPROG	Average Programming Time	–	300	700	µs
tDCBSYW1	Data Cache Busy Time in Write Cache (following 11h)	–	–	10	µs
tDCBSYW2[1]	Data Cache Busy Time in Write Cache (following 15h)	–	–	700	µs
N	Number of Partial Program Cycles in the Same Page	–	–	4	cycle
tBERASE	Block Erase Time	–	3.5	10	ms

NOTE 1 $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by operations shown in command table. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Mode Selection Table.

Mode Selection

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode
H	L	L		H	*	Command Input
L	L	L		H	H	Data Input
L	H	L		H	*	Address Input
L	L	L	H		*	Serial Data Output
*	*	*	*	*	H	During Program (Busy)
*	*	*	*	*	H	During Erase (Busy)
*	*	H	*	*	*	During Read (Busy)
*	*	L	H[1]	H[1]	*	
*	*	*	*	*	L	Program, Erase Inhibit
*	*	H	*	*	0V/V_{CC}	Stand-by

H: V_{IH}, L=V_{IL} *: V_{IH} or V_{IL}.

Note 1: If $\overline{CE}$ is low during read busy. $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to device or read to device. Reset or Status Read command can be input during Read Busy.

Command Table

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Serial Data Input	80_H	—	
Read	00_H	30_H	
Column Address Change in Serial Data Output	05_H	$E0_H$	
Read with Data Cache	31_H	—	
Read Start for Last Page in Read Cycle with Data Cache	$3F_H$	—	
Auto Page Program	80_H	10_H	
Column Address Change in Serial Data Input	85_H	—	
Auto Program with Data Cache	80_H	15_H	
Multi Page Program	80_H	11_H	
	81_H	15_H	
	81_H	10_H	
Read for Page Copy (2) with Data Out	00_H	$3A_H$	
Auto Program with Data Cache during Page Copy (2)	$8C_H$	15_H	
Auto Program for last page during Page Copy (2)	$8C_H$	10_H	
Auto Block Erase	60_H	$D0_H$	
ID Read	90_H	—	
Status Read	70_H	—	O
Status Read for Multi-Page Program or Multi Block Erase	71_H	—	O
Reset	FF_H	—	O

Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O0 to I/O7	Power
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: V_{IH}, L=V_{IL}

ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

ID Definition Table (X8)

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98_H
2nd Data	Device Code	1	0	1	0	1	1	0	0	AC_H
3rd Data	Chip Number, Cell Type	1	0	0	1	0	0	0	0	90_H
4th Data	Page Size, Block Size, I/O Width	0	0	1	0	0	1	1	0	26_H
5th Data	Plane Number	0	1	1	1	0	1	1	0	76_H

3rd ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Reserved		1	0	0	1				

4th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (without redundant area)	1 KB							0	0
	2 KB							0	1
	4 KB							1	0
	8 KB							1	1
Block Size (without redundant area)	64 KB			0	0				
	128 KB			0	1				
	256 KB			1	0				
	512 KB			1	1				
I/O Width	X8		0						
	X16		1						
Reserved		0				0	1		

5th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1 Plane					0	0		
	2 Plane					0	1		
	4 Plane					1	0		
	8 Plane					1	1		
Reserved		0	1	1	1			1	0

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using $\overline{RE}$ after a “70h” command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

Status Register Definition for 70_H Command

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program	Definition
I/O 0	Pass / Fail	Pass / Fail	Invalid	Invalid	Pass / Fail	Chip Status1 Pass : 0 / Fail : 1
I/O 1	Invalid	Invalid	Invalid	Invalid	Pass / Fail	Chip Status2 Pass : 0 / Fail : 1
I/O 2	0	0	0	0	0	Not Used
I/O 3	0	0	0	0	0	Not Used
I/O 4	0	0	0	0	0	Not Used
I/O 5	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Page Buffer Busy : 0 / Ready : 1
I/O 6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Busy : 0 / Ready : 1
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect Protected : 0 / Not Protected : 1

NOTE The Pass/Fail status on I/O0 and I/O1 is only valid during a Program/Erase operation when the device is in the Ready state.

Chip Status 1:

During a Auto Page Program or Auto Block Erase operation this bit indicates the pass/fail result.

During a Auto Page Programming with Data Cache operation, this bit shows the pass/fail results of the current page program operation, and therefore this bit is only valid when I/O5 shows the Ready state.

Chip Status 2:

This bit shows the pass/fail result of the previous page program operation during Auto Page Programming with Data Cache. This status is valid when I/O6 shows the Ready State.

The status output on the I/O5 is the same as that of I/O6 if the command input just before the 70h is not 15h or 31h.

The 71_H Command Status Description

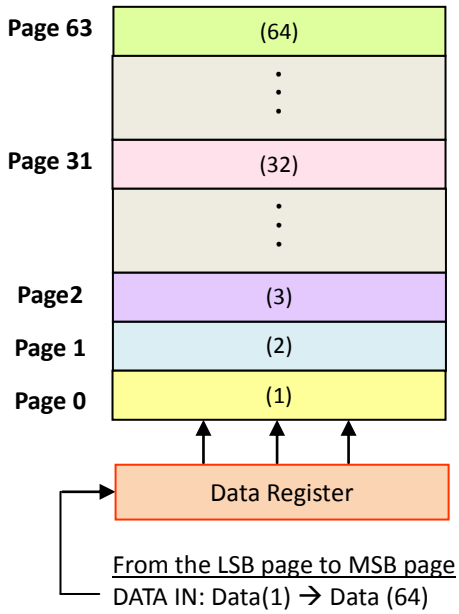
I/O	Status	Output
I/O 0	Chip Status1 : Pass / Fail	Pass : 0 / Fail : 1
I/O 1	District 0 Chip Status1 : Pass / Fail	Pass : 0 / Fail : 1
I/O 2	District 1 Chip Status2 : Pass / Fail	Pass : 0 / Fail : 1
I/O 3	District 0 Chip Status1 : Pass / Fail	Pass : 0 / Fail : 1
I/O 4	District 1 Chip Status2 : Pass / Fail	Pass : 0 / Fail : 1
I/O 5	Ready / Busy	Busy : 0 / Ready : 1
I/O 6	Data Cache Ready / Busy	Busy : 0 / Ready : 1
I/O 7	Write Protect	Protected : 0 / Not Protected : 1

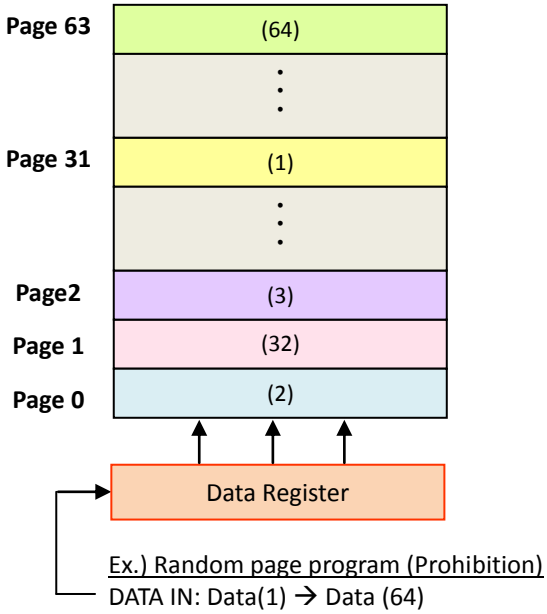
I/O0 describes Pass/Fail condition of district 0 and 1 (OR data of I/O1 and I/O2). If one of the districts fails during multi page program operation, it shows “Fail”.

I/O1 to I/O4 shows the Pass/Fail condition of each district. For details on “Chip Status 1” and “Chip Status2” refer to section “Status Read”.

Addressing for Program Operation

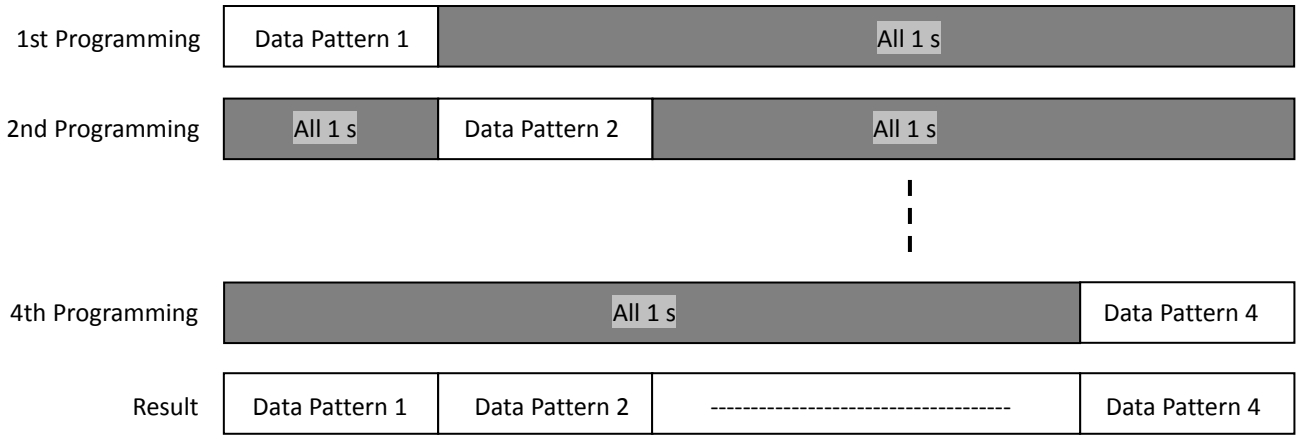
Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.





Several programming cycles on the same page (Partial Page Program)

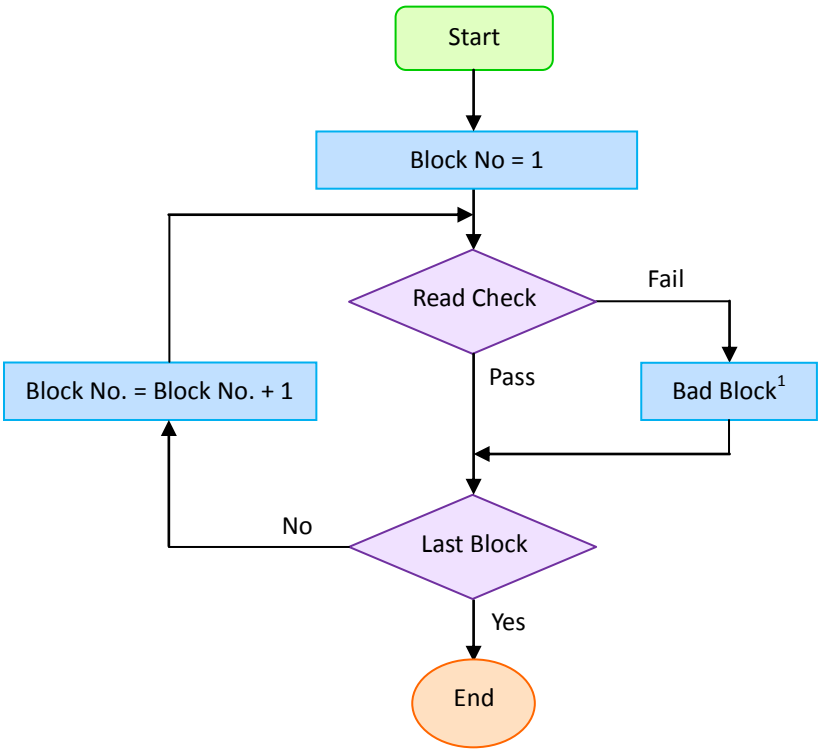
Each segment can be programmed individually as follows:



Bad Block Test Flow

Regarding invalid blocks, bad block mark is in whole pages.

Please read one column of any page in each block. It makes sure that every invalid block has Marjority “0” data at this column. If the data of the column is Marjority “0”, define the block as a bad block.



Note1: No erase operation is allowed to detected bad blocks.

Failure phenomena for Program and Erase Operations

The device may fail during a Program or Erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

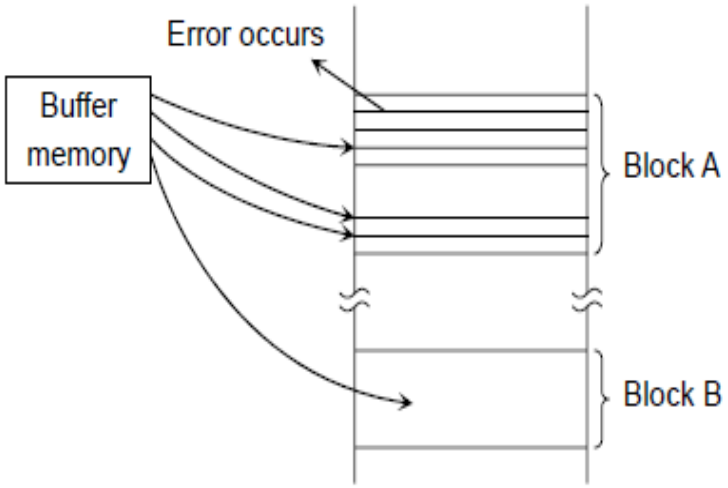
Failure Mode		Detection and Countermeasure Sequence
Block	Erase Failure	Read Status after Erase → Block Replacement
Page	Programming Failure	Read Status after Program → Block Replacement
Read	Bit Error	ECC Correction / Block Refresh

NOTE 1 ECC: Error Correction Code. 8 bit correction per 512 Bytes is necessary.

Block Replacement

Program

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using anther appropriate scheme).



Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

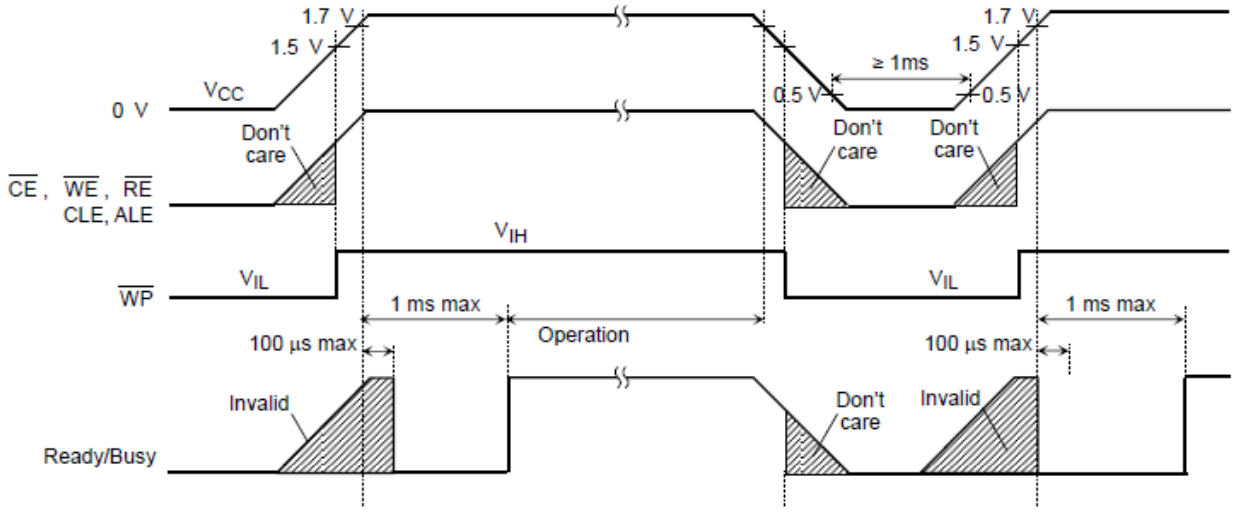
Power-on/off sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence.

During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.

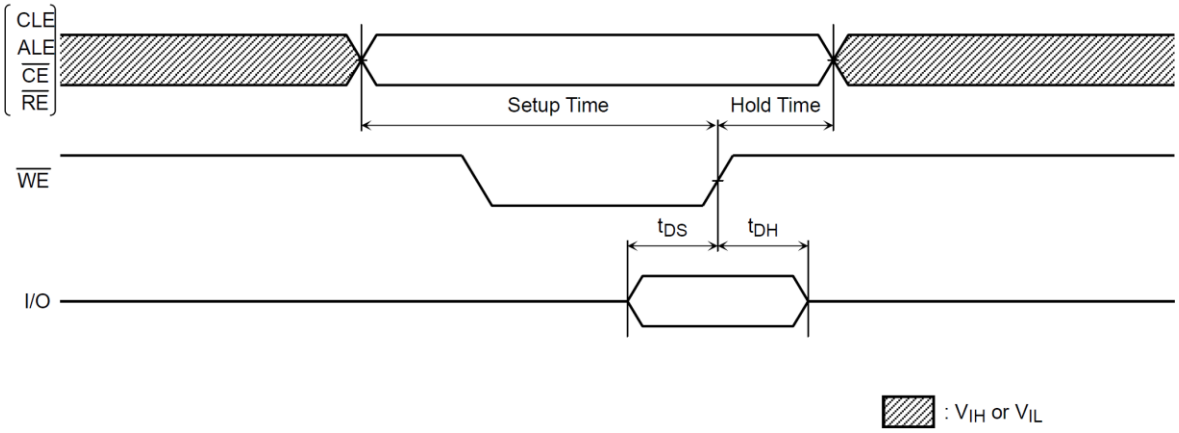
The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.



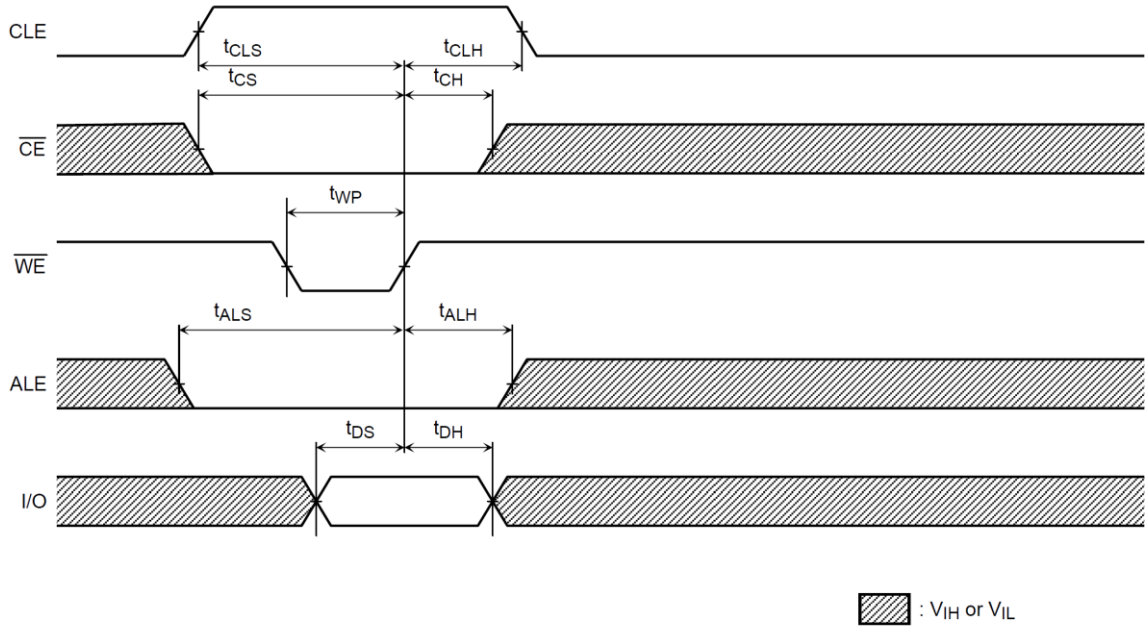
Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

TIMING DIAGRAMS

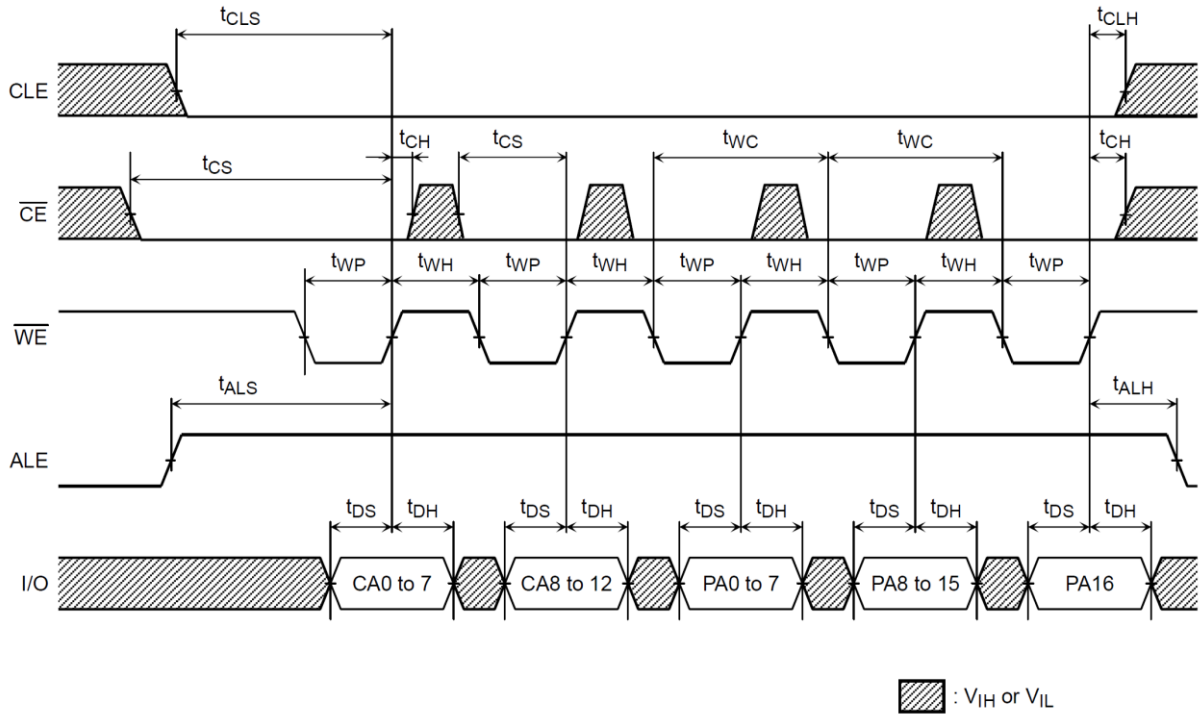
Latch Timing Diagram for Command/Address/Data



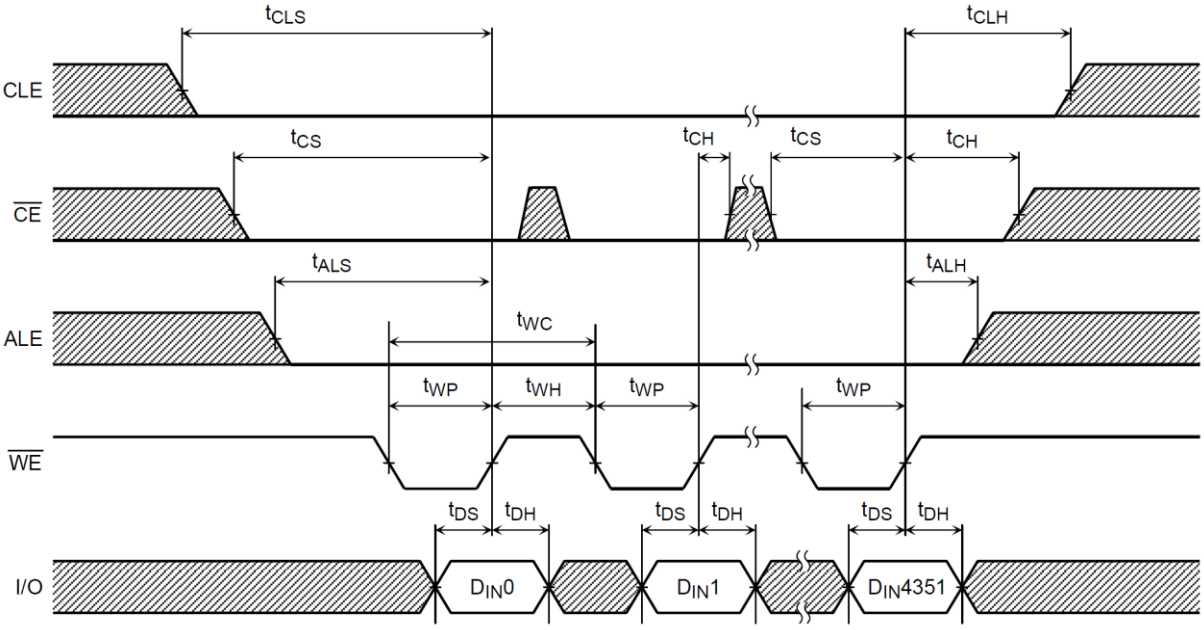
Command Input Cycle Timing Diagram



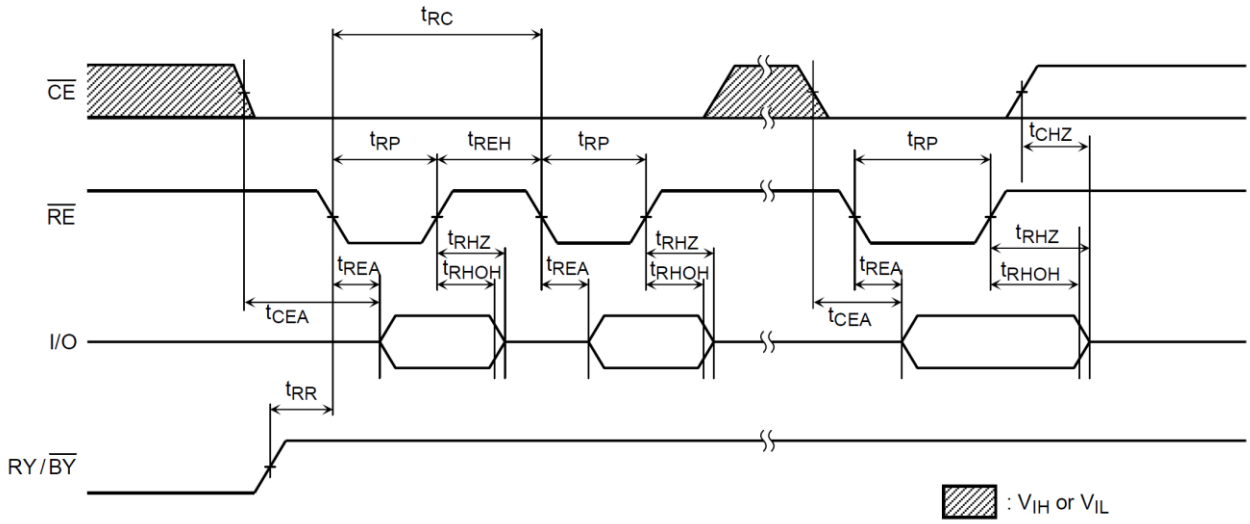
Address Input Cycle Timing Diagram



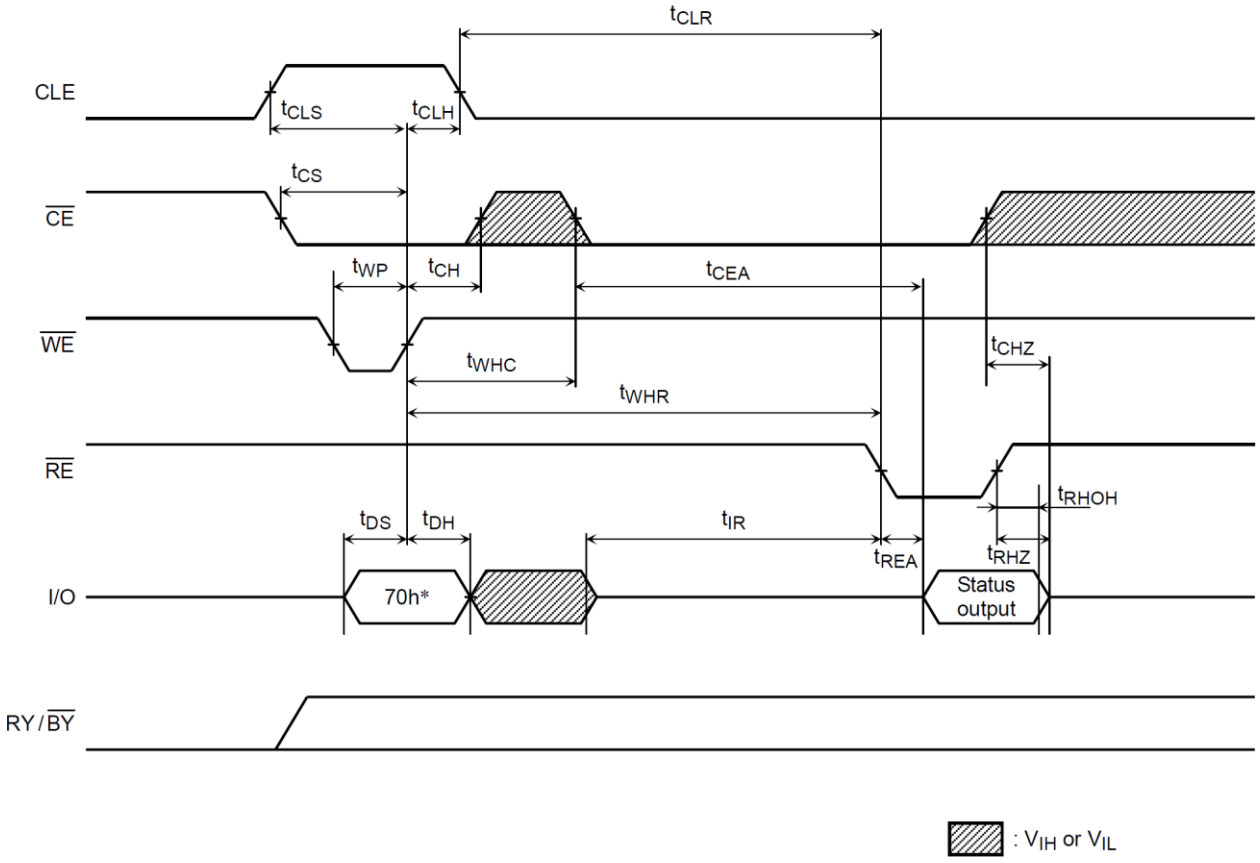
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram

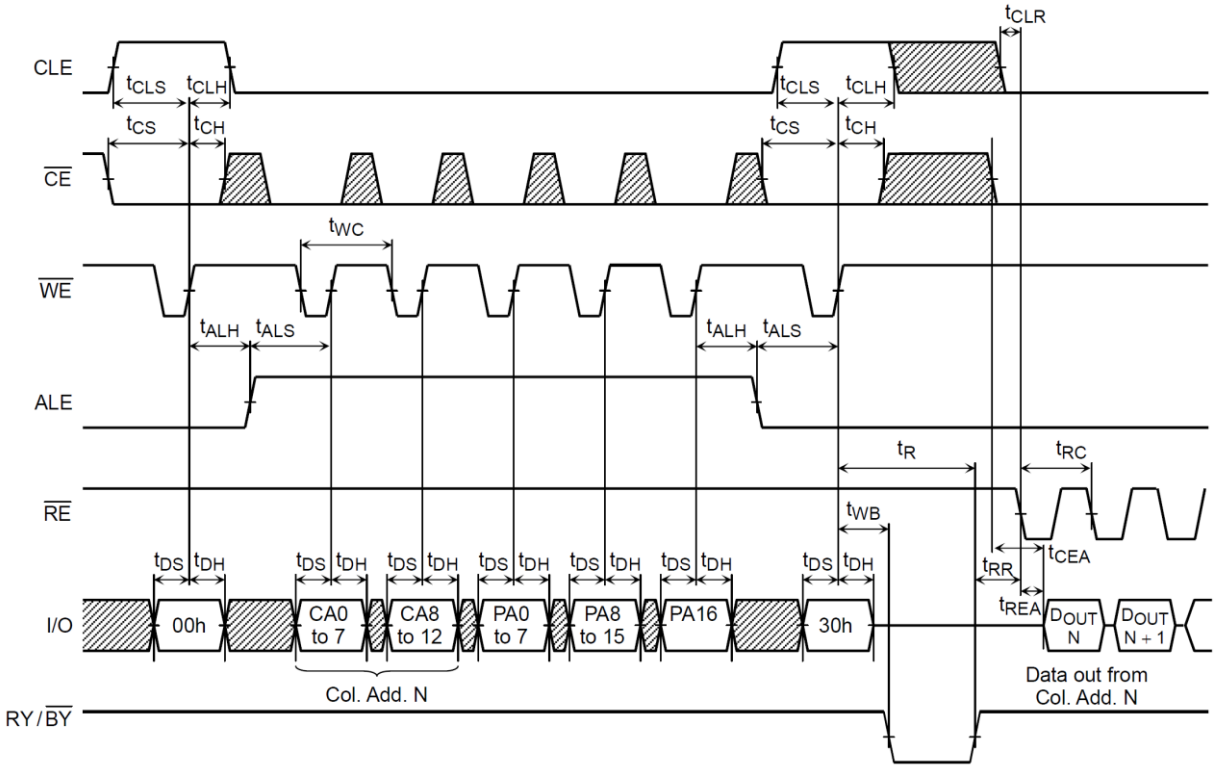


Status Read Cycle Timing Diagram

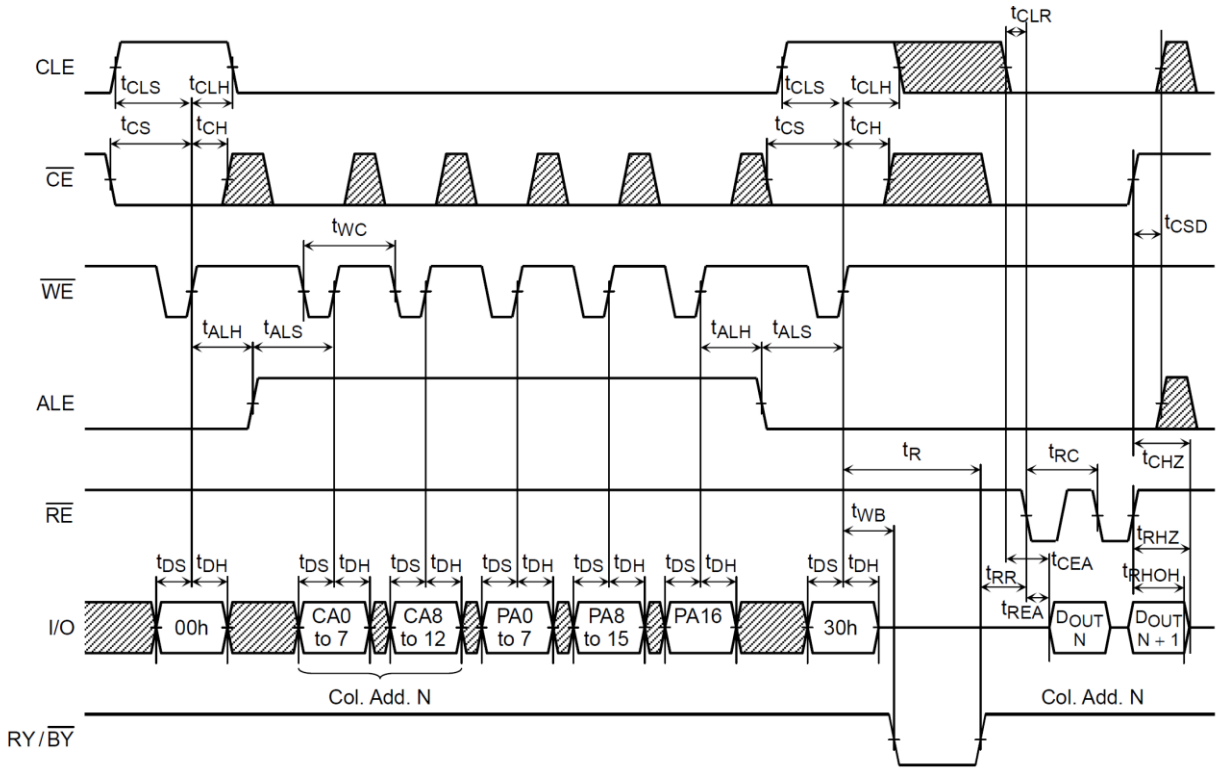


*: 70h represents the hexadecimal number

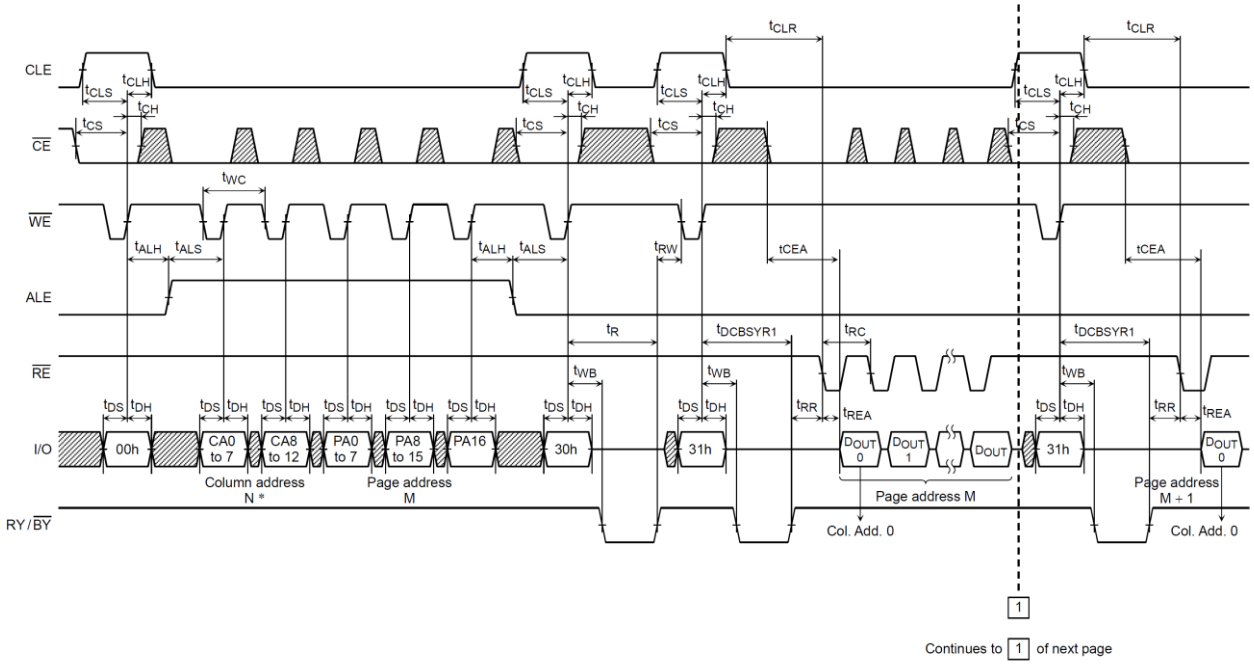
Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by $\overline{CE}$

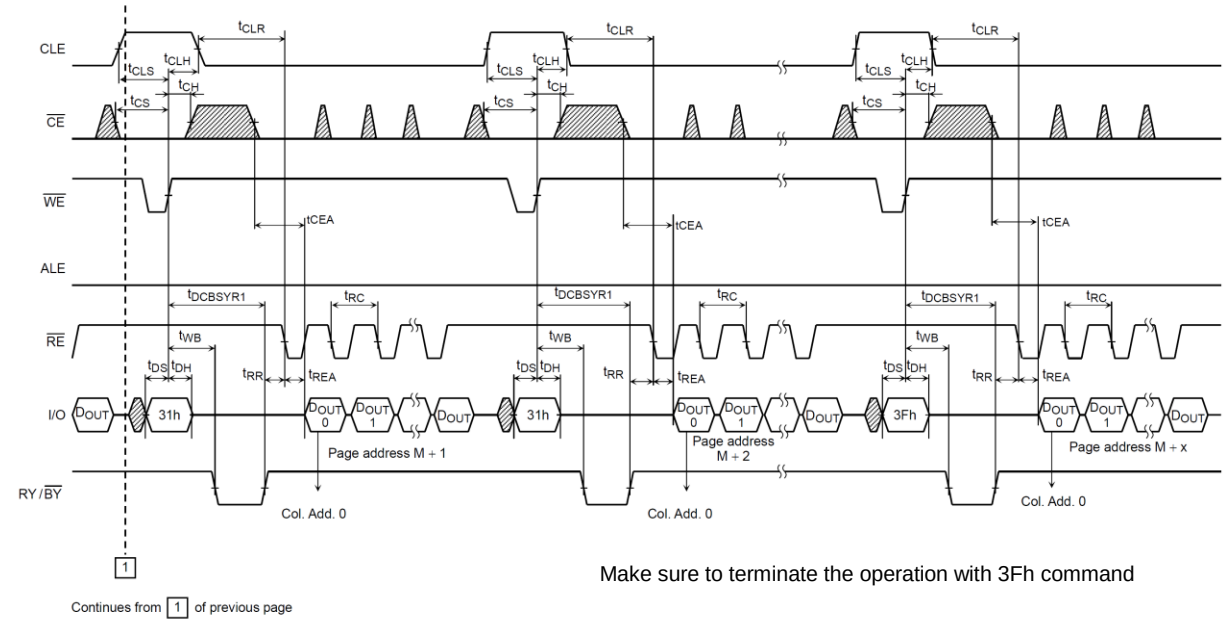


Read Cycle with Data Cache Timing Diagram (1/2)



*: The column address will be reset to 0 by the 31h command input.

Read Cycle with Data Cache Timing Diagram (2/2)



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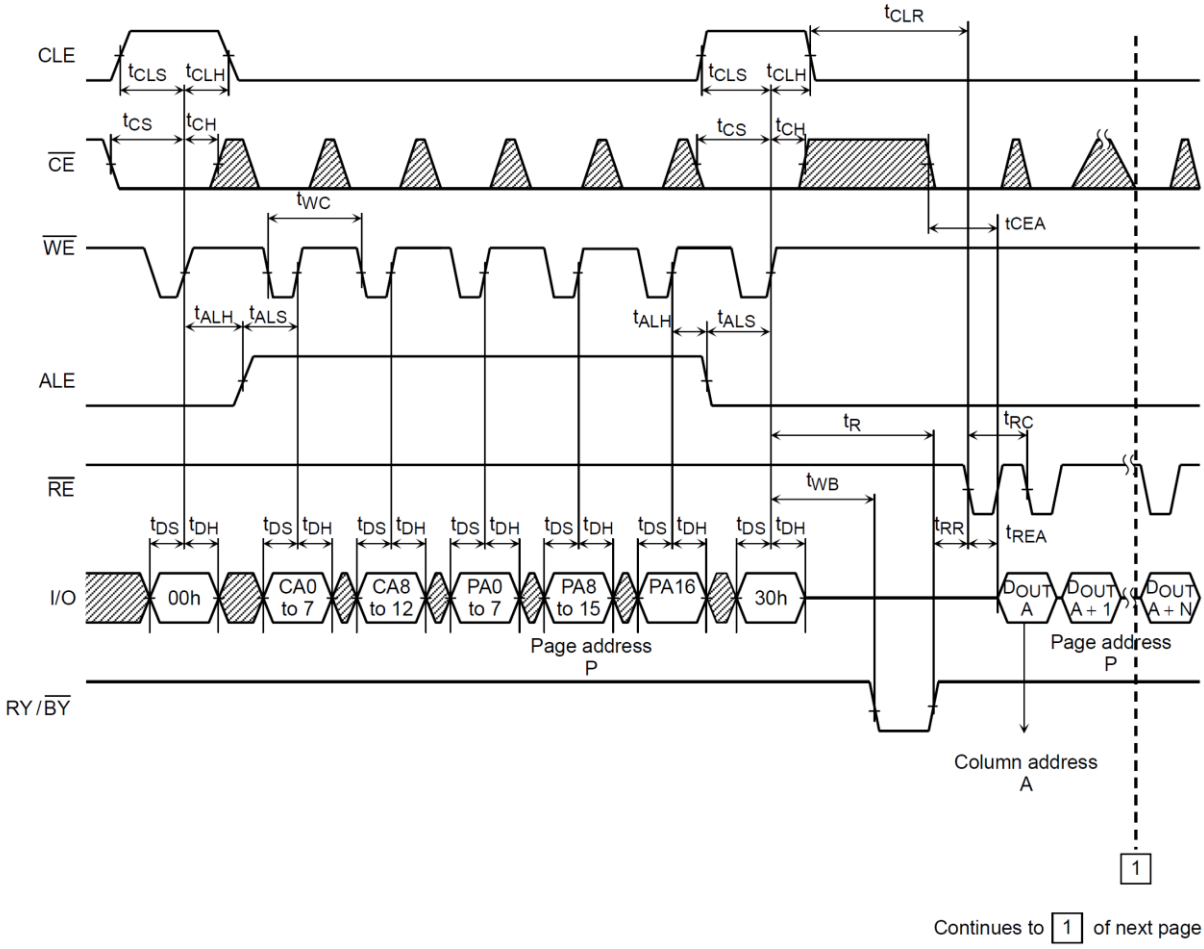
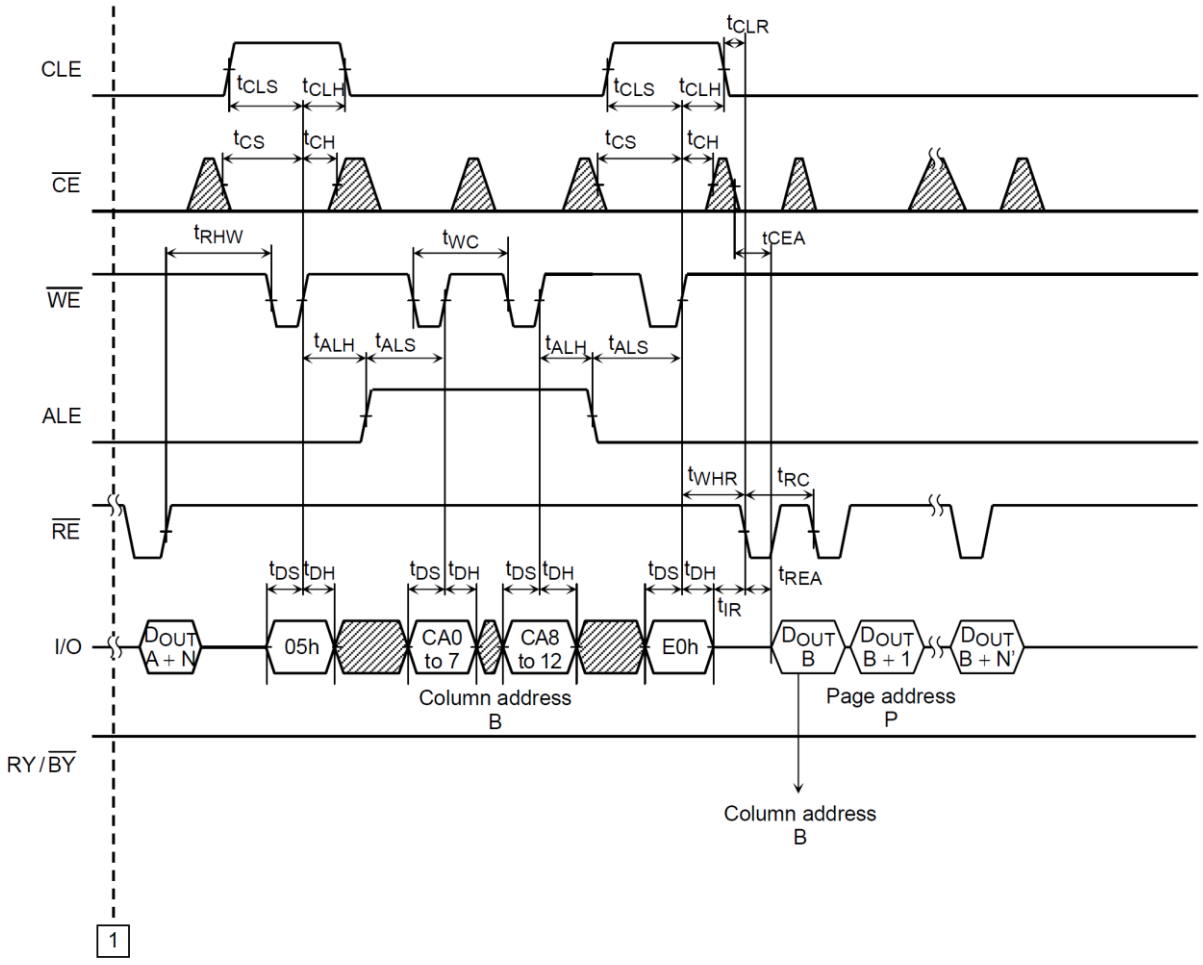
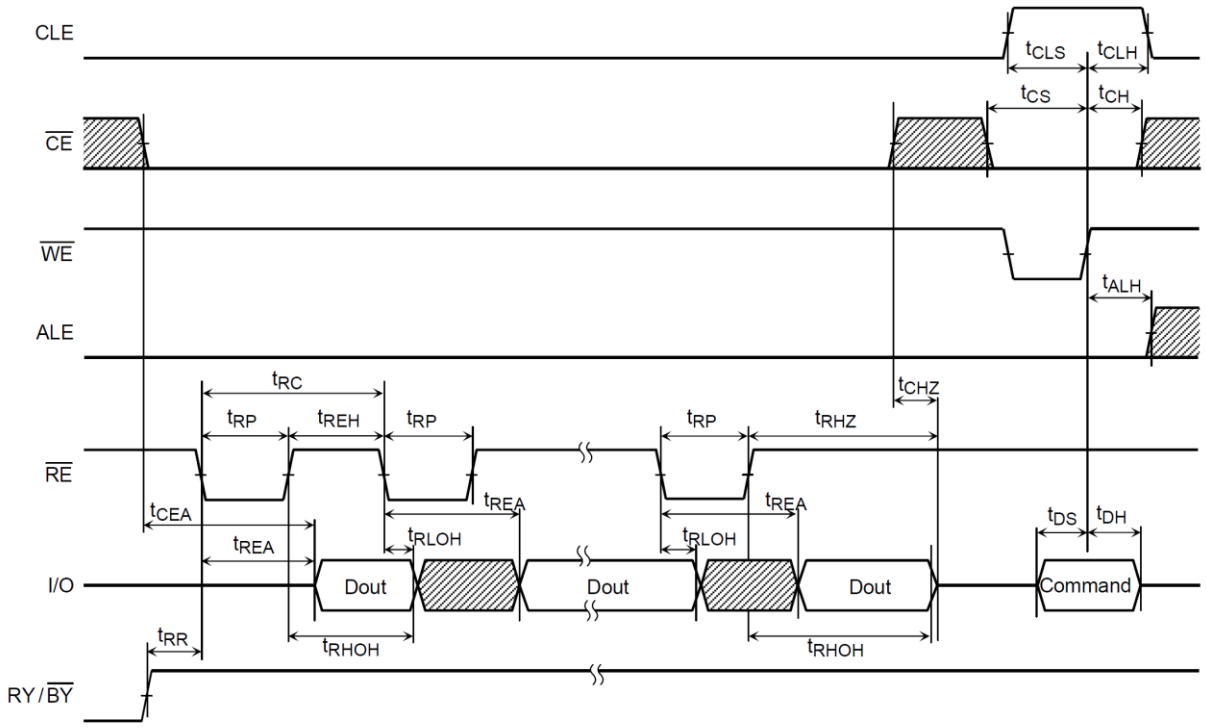
Column Address Change in Read Cycle Timing Diagram (1/2)



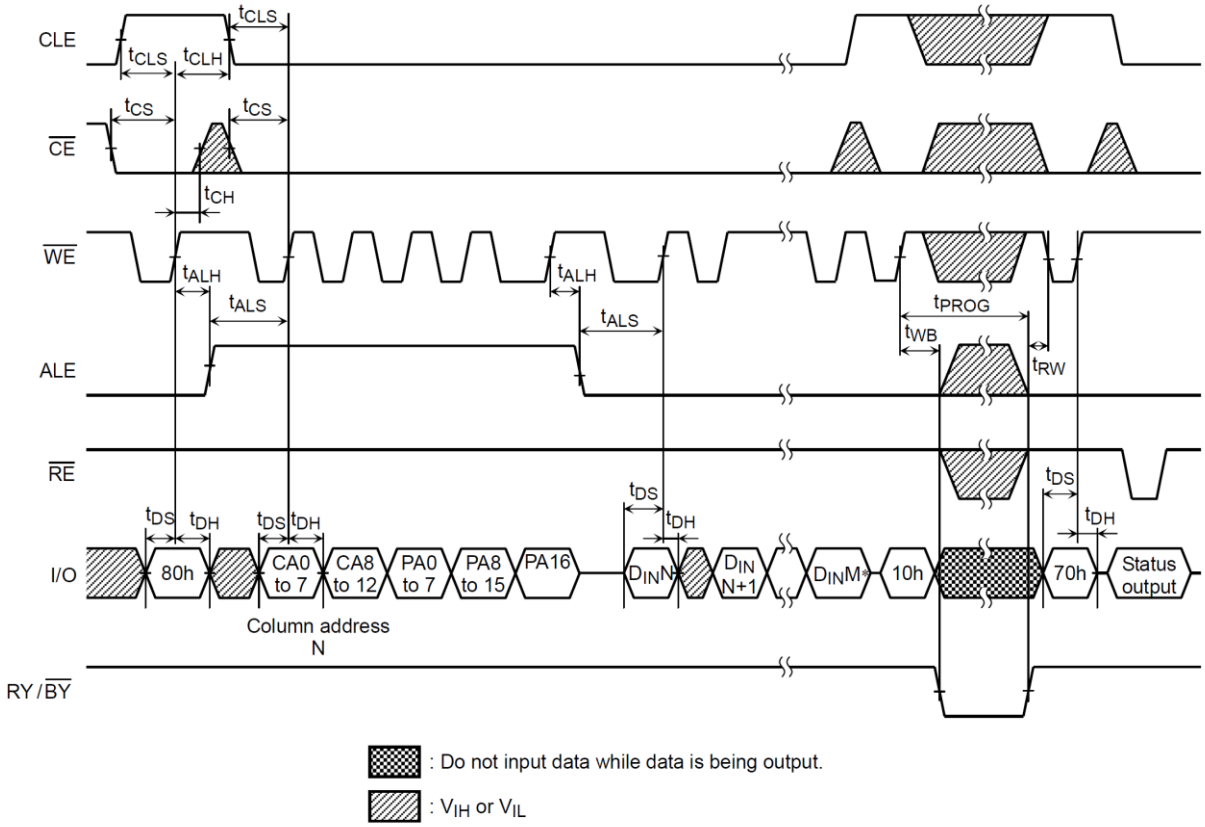
Column Address Change in Read Cycle Timing Diagram (2/2)



Data Output Timing Diagram

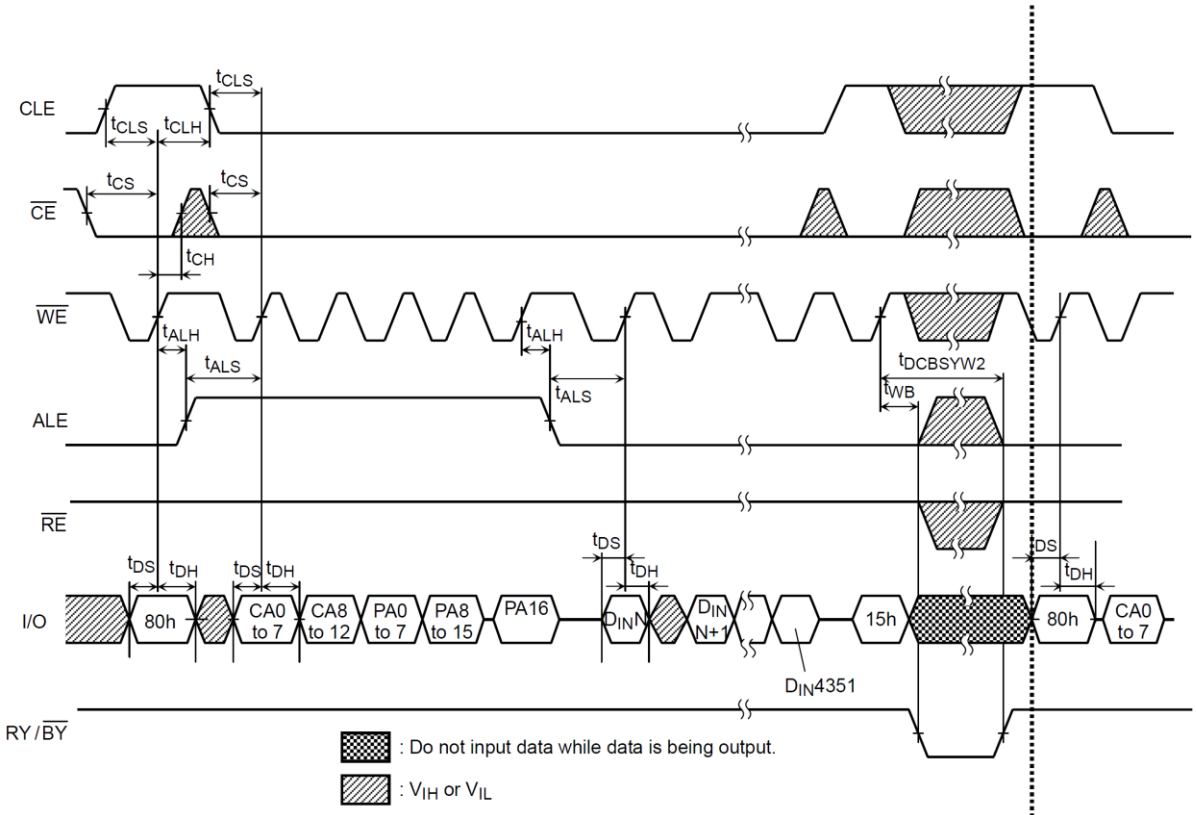


Auto-Program Operation Timing Diagram



*: M: up to 4351 (byte input data for ×8 device).

Auto-Program Operation with Data Cache Timing Diagram (1/3)

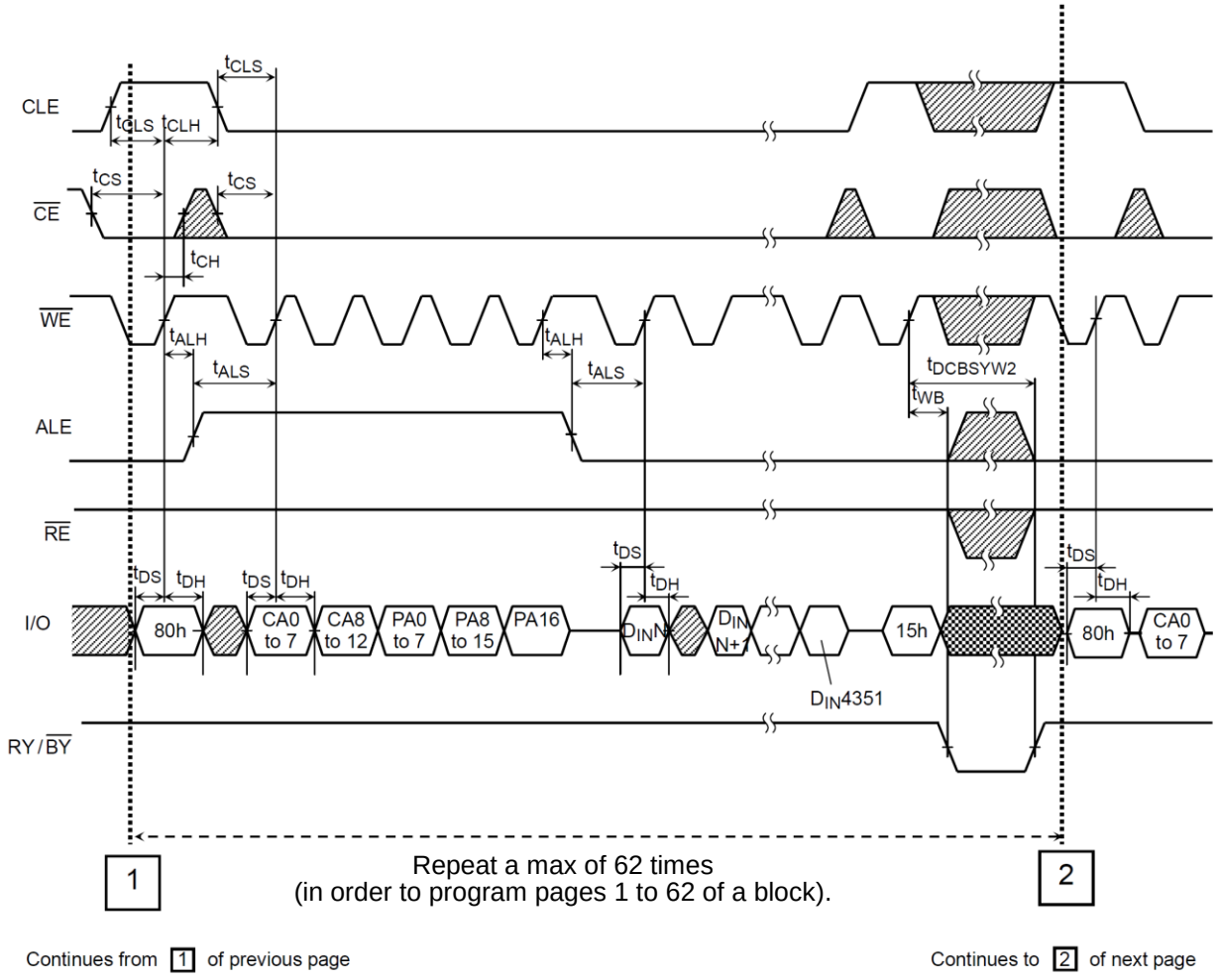


CA0 to CA12 is 0 in this diagram.

1

Continues to 1 of next page

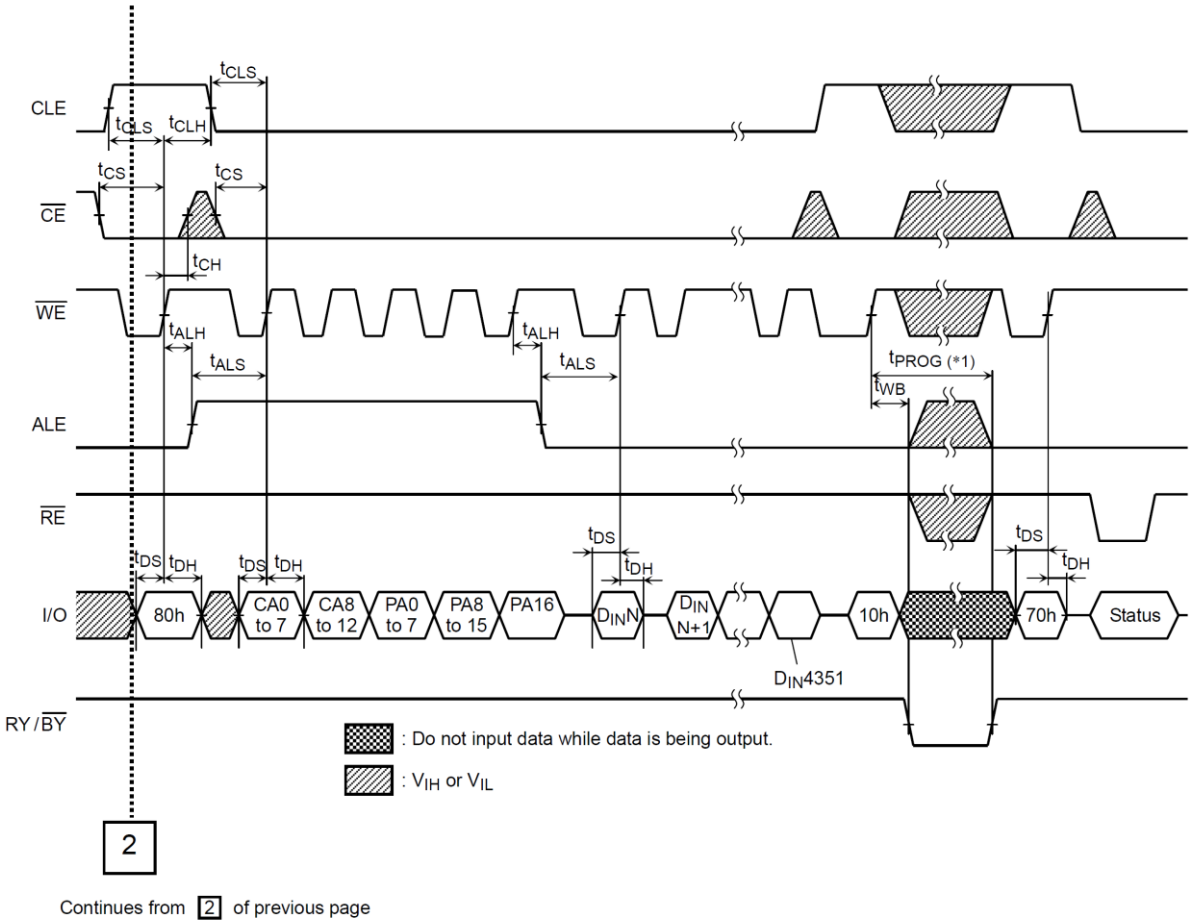
Auto-Program Operation with Data Cache Timing Diagram (2/3)



: Do not input data while data is being output.

: V_{IH} or V_{IL}

Auto-Program Operation with Data Cache Timing Diagram (3/3)



(*1)

tPROG: Since the last page programming by 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following equation.

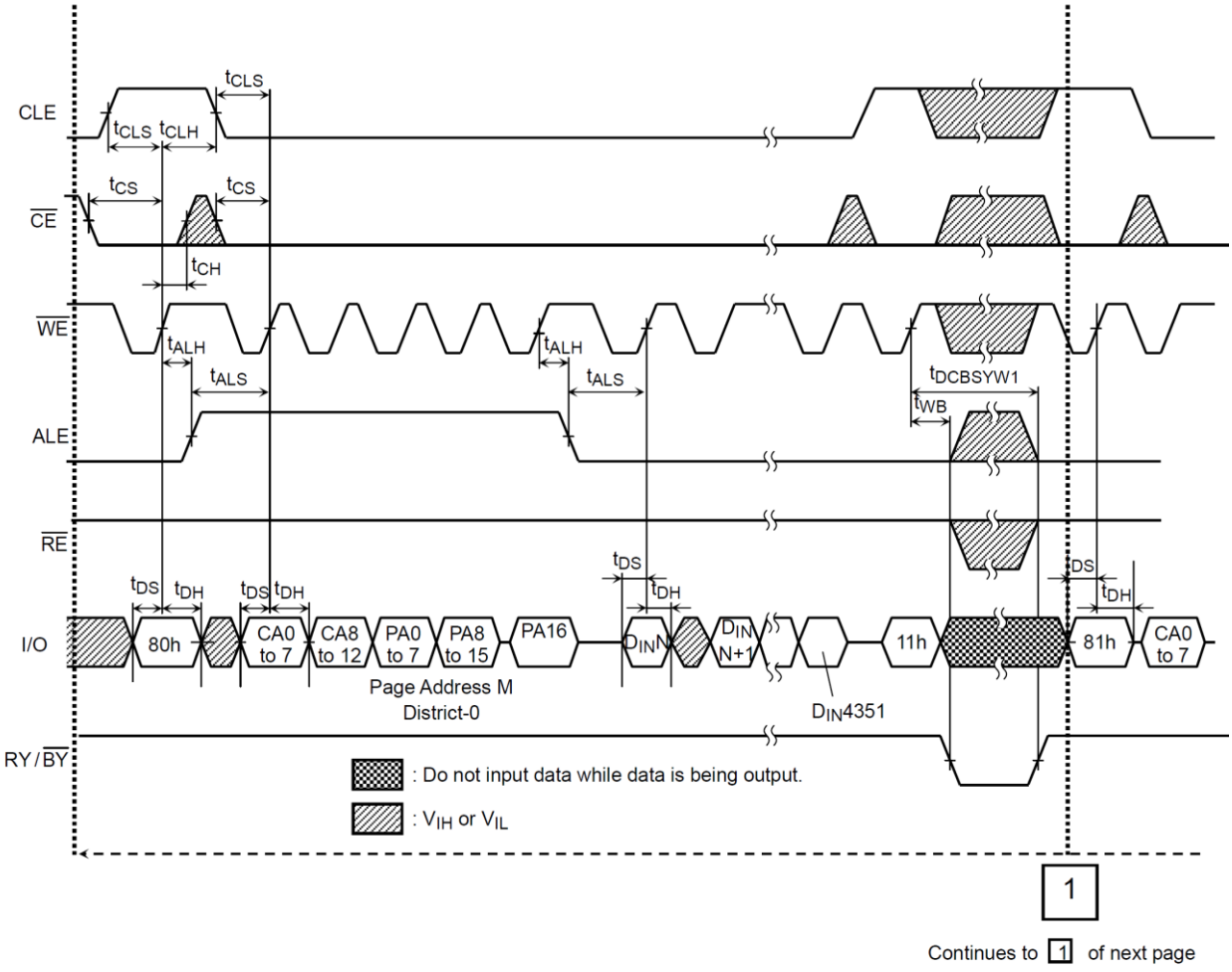
tPROG = tPROG of the last page + tPROG of the previous page − A

A = (command input cycle + address input cycle + data input cycle time of the last page)

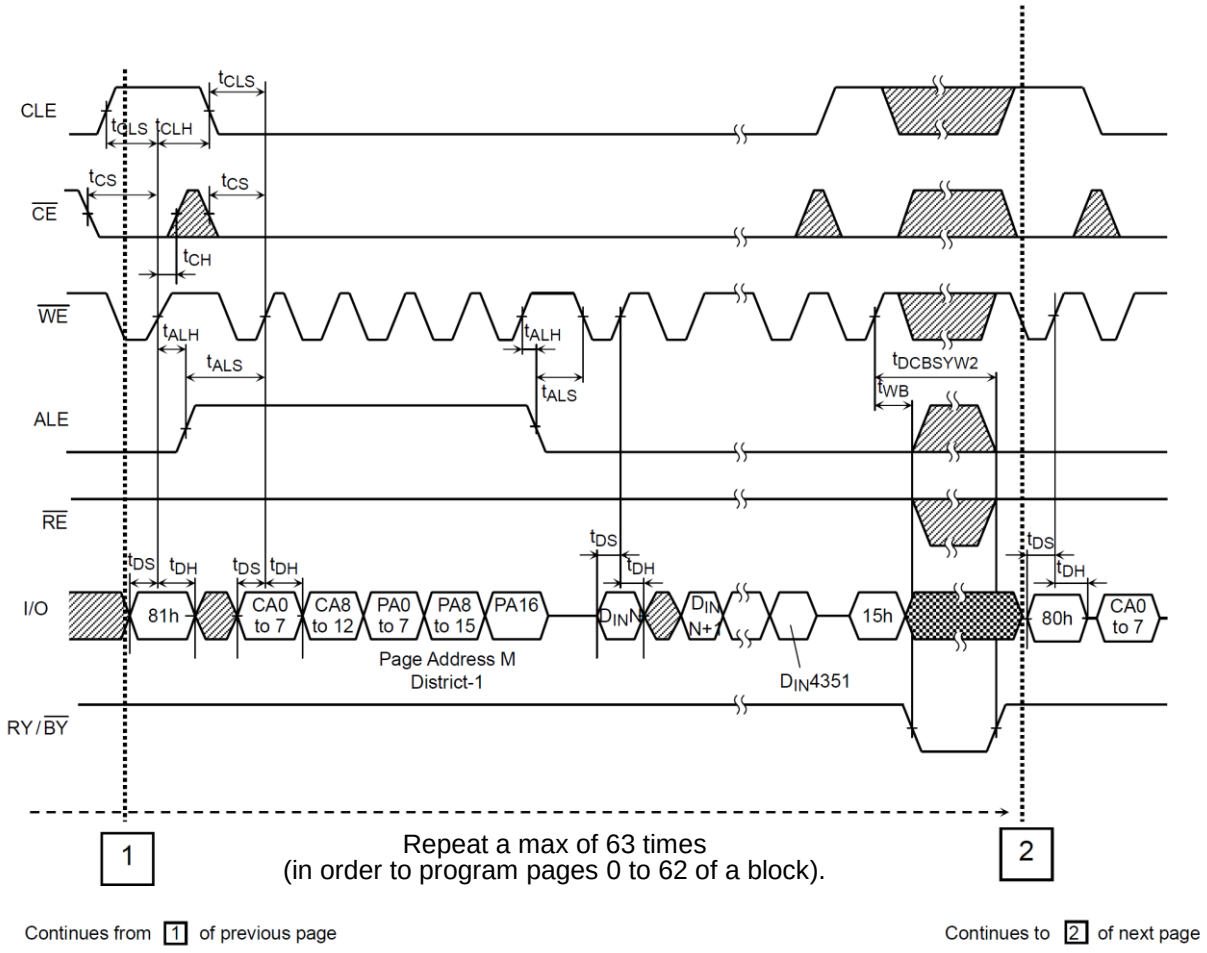
If “A” exceeds the tPROG of previous page, tPROG of the last page is tPROG max.

NOTE : Make sure to terminate the operation with 80h-10h- command sequence.
If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

Multi-Page Program Operation with Data Cache Timing Diagram (1/4)



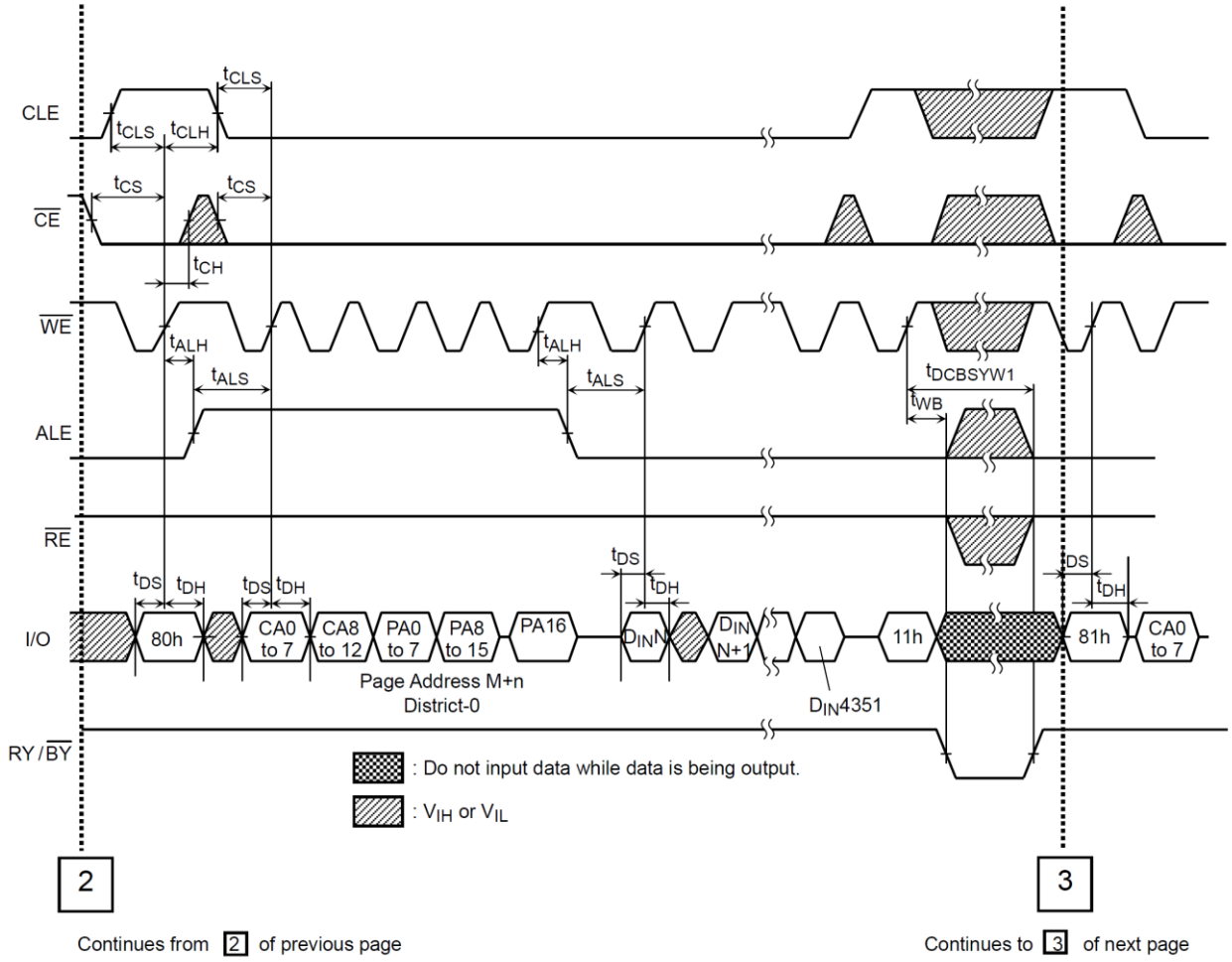
Multi-Page Program Operation with Data Cache Timing Diagram (2/4)



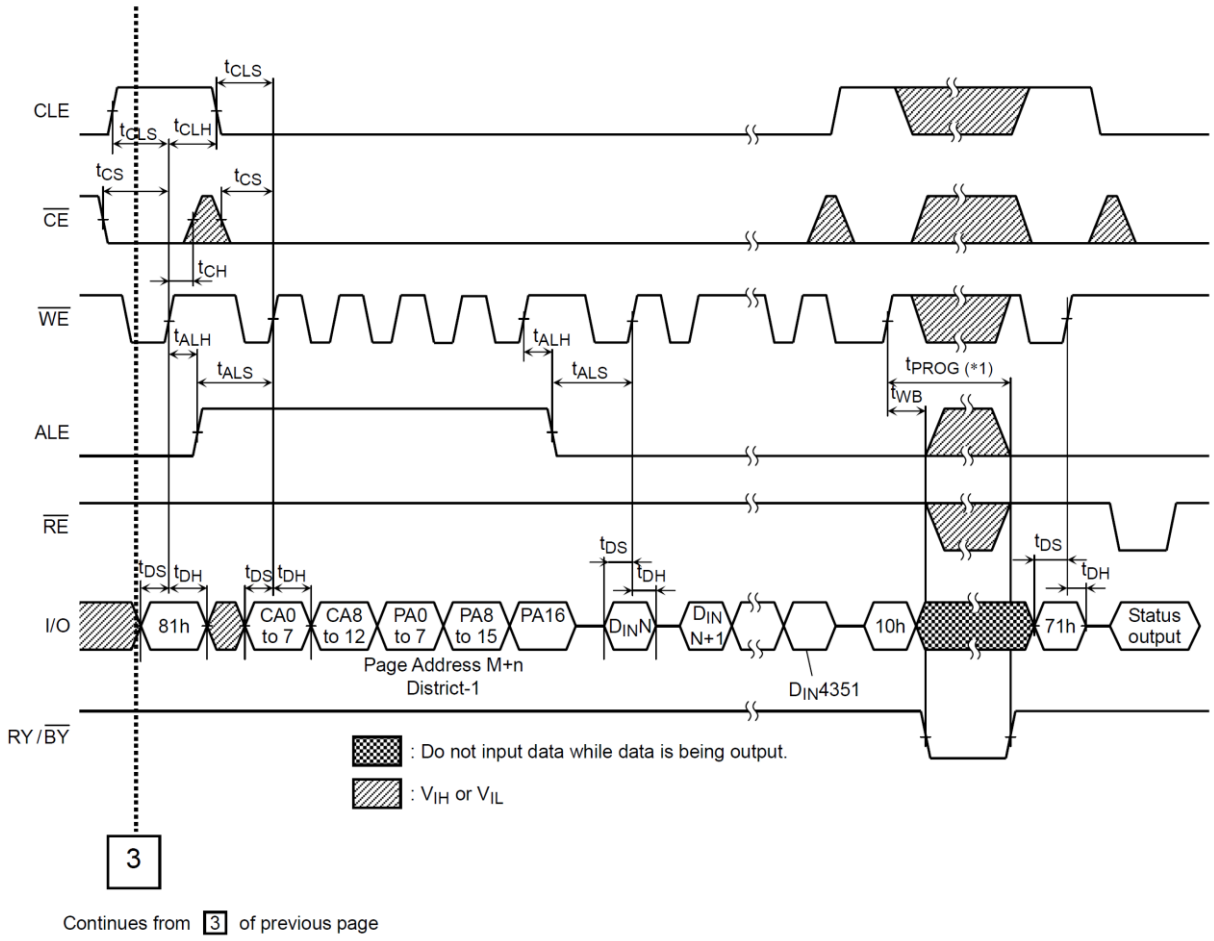
: Do not input data while data is being output.

: V_{IH} or V_{IL}

Multi-Page Program Operation with Data Cache Timing Diagram (3/4)



Multi-Page Program Operation with Data Cache Timing Diagram (4/4)



(*1)

tPROG: Since the last page programming by 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following equation.

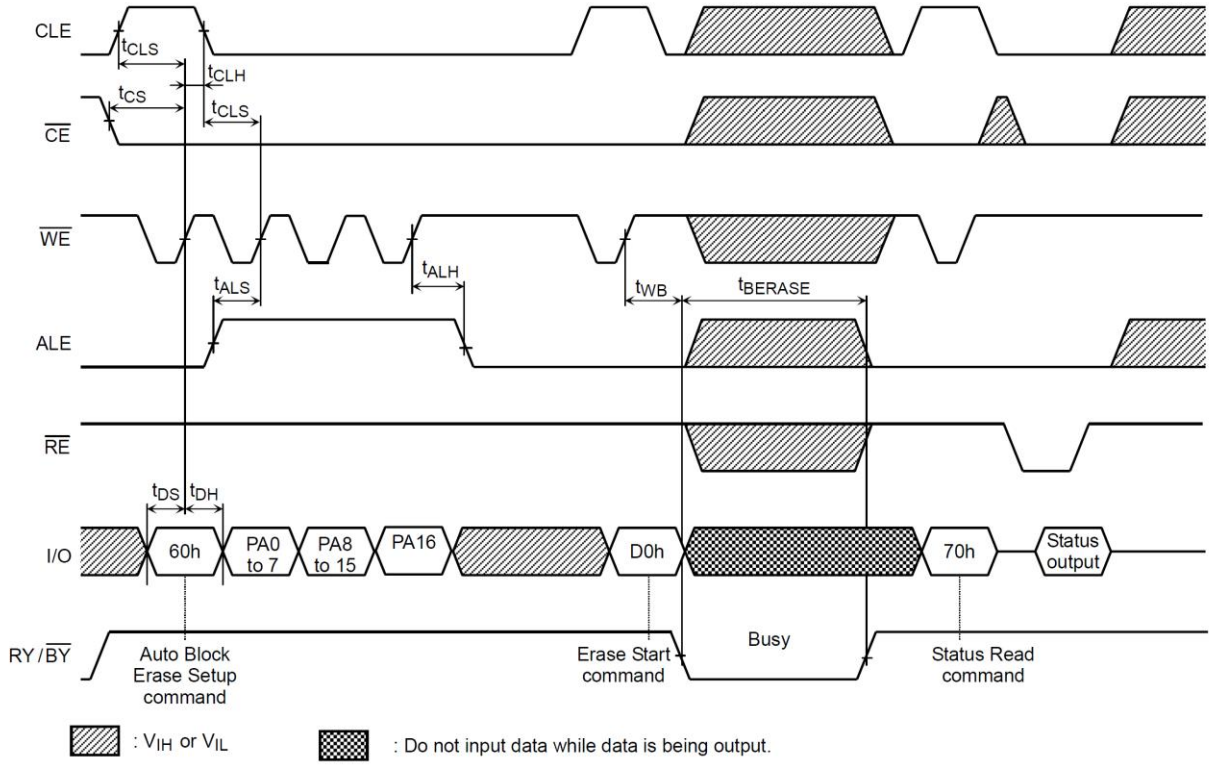
tPROG = tPROG of the last page + tPROG of the previous page − A

A = (command input cycle + address input cycle + data input cycle time of the last page)

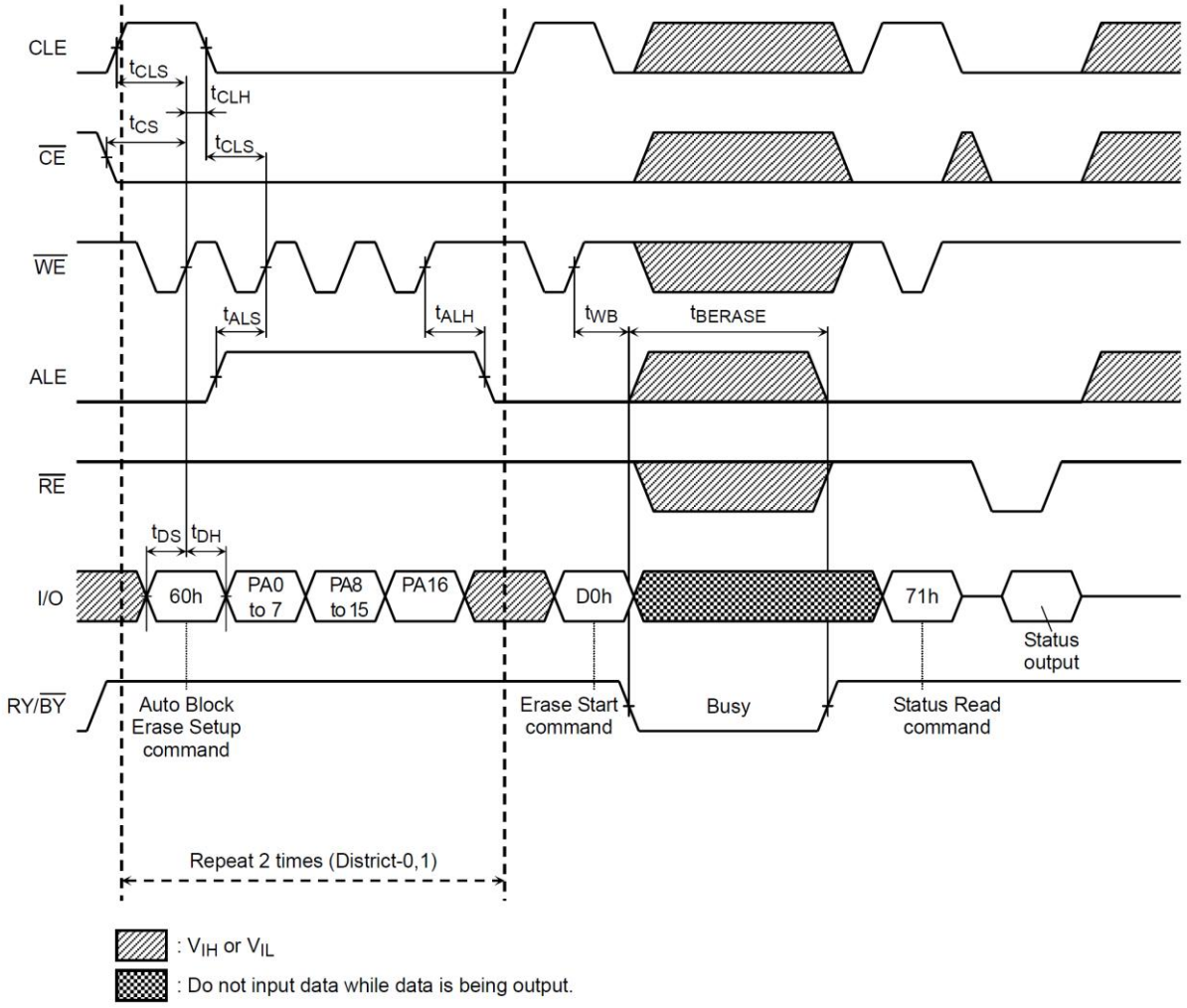
If “A” exceeds the tPROG of previous page, tPROG of the last page is tPROG max.

NOTE : Make sure to terminate the operation with 81h-10h- command sequence.
If the operation is terminated by 81h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status
Read command (70h) and make sure the previous page program operation is completed.
If the page program operation is completed issue FFh reset before next operation.

Auto Block Erase Timing Diagram



Multi Block Erase Timing Diagram



ID Read Operation Timing Diagram

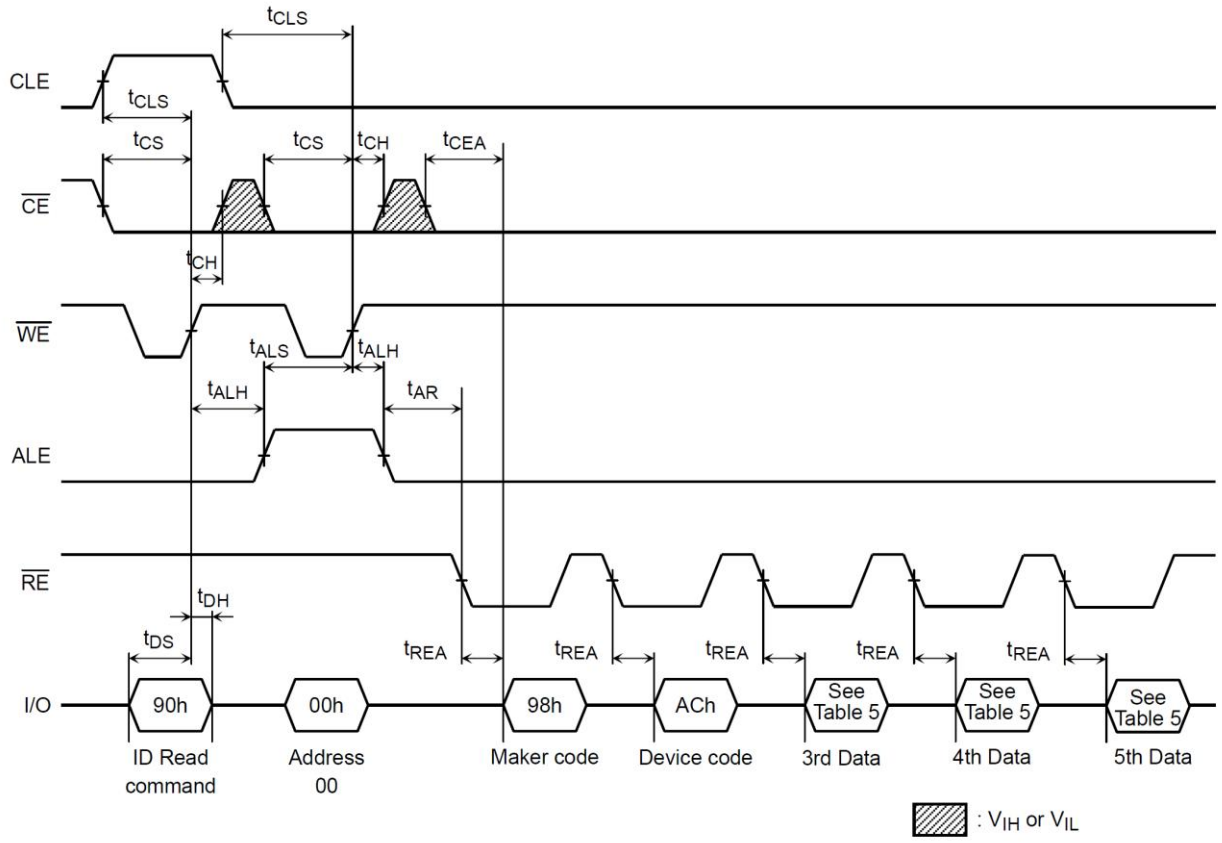


Table 5: ID Definition Table

4Gb(X32, SDP)/8Gb (X32, DDP) LPDDR3

LPDDR3 Descriptions

4Gb LPDDR3-SDRAM has 4,294,967,296 bits. These devices are high-speed synchronous DRAM devices internally configured as an 8-bank memory and use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the device effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the device must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	-0.4	2.3	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	1.6	V	1
V_{DDCA} supply voltage relative to V_{SS}	V_{DDCA}	-0.4	1.6	V	1,2
V_{DDQ} supply voltage relative to V_{SS}	V_{DDQ}	-0.4	1.6	V	1,3
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.6	V	
Storage Temperature	T_{STG}	-55	125	°C	4

NOTE 1 See "Power-Ramp" section for relationships between power supplies.

NOTE 2 $V_{REFCA} \leq 0.6 \times V_{DDCA}$; however, V_{REFCA} may be $\geq V_{DDCA}$ provided that $V_{REFCA} \leq 300mV$.

NOTE 3 $V_{REFDQ} \leq 0.7 \times V_{DDQ}$; however, V_{REFDQ} may be $\geq V_{DDQ}$ provided that $V_{REFDQ} \leq 300mV$.

NOTE 4 Storage Temperature is the case surface temperature on the center/top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

AC/DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Voltage			DRAM	Unit
	Min	Typ	Max		
V_{DD1}	1.70	1.80	1.95	Core Power1	V
V_{DD2}	1.14	1.20	1.30	Core Power2	V
V_{DDCA}	1.14	1.20	1.30	Input Buffer Power	V
V_{DDQ}	1.14	1.20	1.30	I/O Buffer Power	V

NOTE 1 V_{DD1} uses significantly less current than V_{DD2}.

NOTE 2 The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1MHz at the DRAM package ball.

Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current	I_L	-2	2	uA	1, 2
V_{REF} supply leakage current	I_{VREF}	-1	1	uA	3, 4

NOTE 1 For CA, CKE, $\overline{CS}$, CK, $\overline{CK}$. Any input 0V ≤ V_{IN} ≤ V_{DDCA} (All other pins not under test = 0V)

NOTE 2 Although DM is for input only, the DM leakage shall match the DQ and DQS/$\overline{DQS}$ output leakage specification.

NOTE 3 The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

NOTE 4 V_{REFDQ} = V_{DDQ}/2 or V_{REFCA} = V_{DDCA}/2. (All other pins not under test = 0V)

AC/DC Input Measurement Level

AC and DC Logic Input Levels for Single-Ended Signals

Single-Ended AC and DC Input Levels for CA and $\overline{CS}$ Inputs

Symbol	Parameter	1600		Unit	Notes
		Min	Max		
V_{IHCA}(AC)	AC input logic high	V_{Ref} + 0.150	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	V_{Ref} - 0.150	V	1, 2
V_{IHCA}(DC)	DC input logic high	V_{Ref} + 0.100	V_{DDCA}	V	1
V_{ILCA}(DC)	DC input logic low	V_{SS}	V_{Ref} - 0.100	V	1
V_{RefCA}(DC)	Reference Voltage for CA and $\overline{CS}$ inputs	0.49 * V_{DDCA}	0.51 * V_{DDCA}	V	3, 4

NOTE 1 For CA and $\overline{CS}$ input only pins. $V_{Ref} = V_{RefCA(DC)}$.

NOTE 2 Overshoot and Undershoot Specifications.

NOTE 3 The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from $V_{RefCA(DC)}$ by more than ± 1% V_{DDCA} (for reference: approx. ± 12 mV).

NOTE 4 For reference: approx. $V_{DDCA}/2$ ± 12 mV.

Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.65 * V_{DDCA}	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.35 * V_{DDCA}	V	1

NOTE 1 Overshoot and Undershoot Specifications.

Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	1600		Unit	Notes
		Min	Max		
V_{IHDQ}(AC)	AC input logic high	V_{Ref} + 0.150	Note 2	V	1, 2, 5
V_{ILDQ}(AC)	AC input logic low	Note 2	V_{Ref} - 0.150	V	1, 2, 5
V_{IHDQ}(DC)	DC input logic high	V_{Ref} + 0.100	V_{DDQ}	V	1
V_{ILDQ}(DC)	DC input logic low	V_{SS}	V_{Ref} - 0.100	V	1
V_{RefDQ}(DC) (DQ ODT disabled)	Reference Voltage for DQ, DM inputs	0.49 * V_{DDQ}	0.51 * V_{DDQ}	V	3, 4
V_{RefDQ}(DC) (DQ ODT enabled)	Reference Voltage for DQ, DM inputs	V_{ODTR}/2 - 0.01 * V_{DDQ}	V_{ODTR}/2 + 0.01 * V_{DDQ}	V	3, 5, 6

NOTE 1 For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

NOTE 2 Overshoot and Undershoot Specifications.

NOTE 3 The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from $V_{RefDQ(DC)}$ by more than ± 1% V_{DDQ} (for reference: approx. ± 12 mV).

NOTE 4 For reference: approx. $V_{DDQ}/2$ ± 12 mV.

NOTE 5 For reference: approx. $V_{ODTR}/2$ ± 12 mV.

NOTE 6 R_{ON} and R_{ODT} nominal mode register programmed values are used for the calculation of V_{ODTR}. For testing purposes a controller RON value of 50 Ω is used.

$$VODTR = \frac{2RON + RTT}{RON + RTT} \times VDDQ$$

Differential AC and DC Input Levels

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
$V_{IHdiff(dc)}$	Differential input high	2 x (V_{IH}(dc) - V_{Ref})	Note 3	V	1
$V_{ILdiff(dc)}$	Differential input low	Note 3	2 x (V_{IL}(dc) - V_{Ref})	V	1
$V_{IHdiff(ac)}$	Differential input high ac	2 x (V_{IH}(ac) - V_{Ref})	Note 3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	Note 3	2 x (V_{IL}(ac) - V_{Ref})	V	2

NOTE 1 Used to define a differential signal slew-rate. For CK - $\overline{CK}$ use $V_{IH}/V_{IL(dc)}$ of CA and V_{REFCA}; for DQS - $\overline{DQS}$, use $V_{IH}/V_{IL(dc)}$ of DQs and V_{REFDQ}; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

NOTE 2 For CK - $\overline{CK}$ use $V_{IH}/V_{IL(ac)}$ of CA and V_{REFCA}; for DQS - $\overline{DQS}$, use $V_{IH}/V_{IL(ac)}$ of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

NOTE 3 These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, and $\overline{DQS}$ need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Overshoot and Undershoot Specifications.

NOTE 4 For CK and $\overline{CK}$, $V_{Ref} = V_{RefCA(DC)}$. For DQS and $\overline{DQS}$, $V_{Ref} = V_{RefDQ(DC)}$.

Allowed time before ringback tDVAC for Strobe (DQS - $\overline{DQS}$)

Slew Rate [V/ns]	t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff(ac)}\rvert$ = 300mV 1600Mbps	
	min	max
> 8.0	48	—
8.0	48	—
7.0	46	—
6.0	43	—
5.0	40	—
4.0	35	—
3.0	27	—
< 3.0	27	—

Allowed time before ringback tDVAC for Clock (CK - $\overline{CK}$)

Slew Rate [V/ns]	t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff(ac)}\rvert$ = 300mV 1600Mbps	
	min	max
> 8.0	48	—
8.0	48	—
7.0	46	—
6.0	43	—
5.0	40	—
4.0	35	—
3.0	27	—
< 3.0	27	—

Single-ended requirements for differential signals

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
*V*SEH(AC150)	Single-ended high-level for strobes	(V_{DDQ} / 2) + 0.150	Note 3	V	1, 2
	Single-ended high-level for CK, $\overline{CK}$	(V_{DDCA} / 2) + 0.150	Note 3	V	1, 2
*V*SEL(AC150)	Single-ended low-level for strobes	Note 3	(V_{DDQ} / 2) - 0.150	V	1, 2
	Single-ended low-level for CK, $\overline{CK}$	Note 3	(V_{DDCA} / 2) - 0.150	V	1, 2

NOTE 1 For CK, $\overline{CK}$ use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0, $\overline{DQS0}$, DQS1, $\overline{DQS1}$, DQS2, $\overline{DQS2}$, DQS3, $\overline{DQS3}$) use $V_{IH}/V_{IL(ac)}$ of DQs.

NOTE 2 $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

NOTE 3 These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS0, $\overline{DQS0}$, DQS1, $\overline{DQS1}$, DQS2, $\overline{DQS2}$, DQS3, $\overline{DQS3}$ need to be within the respective limits ($V_{IH(dc)\ max}$, $V_{IL(dc)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Overshoot and Undershoot Specifications.

Differential Input Cross Point Voltage

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
*V*IXCA	Differential Input Cross Point Voltage relative to V_{DDCA}/2 for CK, $\overline{CK}$	- 120	120	mV	1,2
*V*IXDQ	Differential Input Cross Point Voltage relative to V_{DDQ}/2 for DQS, $\overline{DQS}$	- 120	120	mV	1,2

NOTE 1 The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

NOTE 2 For CK and $\overline{CK}$, $V_{Ref} = V_{RefCA(DC)}$. For DQS and $\overline{DQS}$, $V_{Ref} = V_{RefDQ(DC)}$.

Slew Rate Definitions for Differential Input Signals

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK - $\overline{CK}$ and DQS - $\overline{DQS}$).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff
Differential input slew rate for falling edge (CK - $\overline{CK}$ and DQS - $\overline{DQS}$).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff

NOTE 1 The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds.

AC and DC Output Measurement Levels

Single Ended AC and DC Output Levels

Symbol	Parameter			Value	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)			0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$	ODT disabled	DC output low measurement level (for IV curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OL(DC)}$	ODT enabled			V_{DDQ} x [0.1 + 0.9 x (R_{ON} / (R_{TT} + R_{ON}))]	V	3
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)			V_{REFDQ} + 0.12	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)			V_{REFDQ} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS, $\overline{DQS}$) (DQ, DQS, $\overline{DQS}$ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}		Min	-5	uA	
			Max	5	uA	

NOTE 1 I_{OH} = -0.1mA.
NOTE 2 I_{OL} = 0.1mA.
NOTE 3 The minimum value is derived when using RTT,min and RON,max (±30% uncalibrated, ±15% calibrated).

Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.20 x V_{DDQ}	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.20 x V_{DDQ}	V	2

NOTE 1 I_{OH} = -0.1mA.
NOTE 2 I_{OL} = 0.1mA

Single-ended Output Slew Rate

Parameter	Symbol	Value		Units
		Min[1]	Max[2]	
Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	SRQse	1.5	4.0	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	

Description: SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output); se: Single-ended Signals

NOTE 1 Measured with output reference load.

NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

NOTE 3 The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.

NOTE 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate (R_{ON} = 40Ω +/- 30%)	SRQdiff	3.0	8.0	V/ns

Description: SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output); diff: Differential Signals

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.

NOTE 3 Slew rates are measured under normal SSO conditions, with 50% of DQ signals per data byte switching.

AC Overshoot/Undershoot Specification

Parameter		1600	Units
Maximum peak amplitude allowed for overshoot area.	Max	0.35	V
Maximum peak amplitude allowed for undershoot area.	Max	0.35	V
Maximum area above VDD.	Max	0.10	V-ns
Maximum area below VSS.	Max	0.10	V-ns

NOTE 1 V_{DD} stands for V_{DDCA} for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, ODT, DQS, and $\overline{DQS}$.

NOTE 2 V_{SS} stands for V_{SS} for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. V_{SS} stands for V_{SS} for DQ, DM, ODT, DQS, and $\overline{DQS}$.

NOTE 3 Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.

NOTE 4 Maximum area values are referenced from maximm operating V_{DD} and V_{SS} values.

Input/output capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance, CK and $\overline{CK}$	C_{CK}	0.5	1.2	pF	1,2
Input capacitance delta, CK and $\overline{CK}$	C_{DCK}	0	0.15	pF	1,2,3
Input capacitance, all other input-only pins	C_I	0.5	1.1	pF	1,2,4
Input capacitance delta, all other input-only pins	C_{DI}	-0.20	0.20	pF	1,2,5
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	C_{IO}	1.0	1.8	pF	1,2,6,7
Input/output capacitance delta, DQS, $\overline{DQS}$	C_{DDQS}	0	0.2	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	C_{DIO}	-0.25	0.25	pF	1,2,7,9
Input/output capacitance ZQ Pin	C_{ZQ}	0	2.0	pF	1,2

(T_{OPER} ;V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V, V_{DD2} = 1.14-1.3V)

NOTE 1 This parameter applies to die device only (does not include package capacitance).

NOTE 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SS}, V_{SS} applied and all other pins floating.

NOTE 3 Absolute value of C_{CK} - $C_{\overline{CK}}$.

NOTE 4 C_I applies to $\overline{CS}$, CKE, CA0-CA9, ODT.

NOTE 5 $C_{DI} = C_I - 0.5 * (C_{CK} + C_{\overline{CK}})$

NOTE 6 DM loading matches DQ and DQS.

NOTE 7 MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ω typical)

NOTE 8 Absolute value of C_{DQS} and $C_{\overline{DQS}}$.

NOTE 9 $C_{DIO} = C_{IO} - 0.5 * (C_{DQS} + C_{\overline{DQS}})$ in byte-lane.

IDD Specifications

Parameter Condition	Symbol	Power Supply	1600 (X32)		Unit
			SDP	DDP	
Operating one bank active-precharge current	I_{DD01}	V_{DD1}	15	30	mA
	I_{DD02}	V_{DD2}	70	140	
	I_{DD0in}	V_{DDCA}, V_{DDQ}	12	24	
Idle power-down standby current	I_{DD2P1}	V_{DD1}	600	1200	µA
	I_{DD2P2}	V_{DD2}	800	1600	
	$I_{DD2P,in}$	V_{DDCA}, V_{DDQ}	120	240	
Idle power-down standby current with clock stop	I_{DD2PS1}	V_{DD1}	600	1200	µA
	I_{DD2PS2}	V_{DD2}	800	1600	
	$I_{DD2PS,in}$	V_{DDCA}, V_{DDQ}	120	240	
Idle non-power-down standby current	I_{DD2N1}	V_{DD1}	2	4	mA
	I_{DD2N2}	V_{DD2}	24	48	
	$I_{DD2N,in}$	V_{DDCA}, V_{DDQ}	12	24	
Idle non-power-down standby current with clock stopped	I_{DD2NS1}	V_{DD1}	1.7	3.4	mA
	I_{DD2NS2}	V_{DD2}	10	20	
	$I_{DD2NS,in}$	V_{DDCA}, V_{DDQ}	6	12	
Active power-down standby current	I_{DD3P1}	V_{DD1}	1000	2000	µA
	I_{DD3P2}	V_{DD2}	7.5	15	mA
	$I_{DD3P,in}$	V_{DDCA}, V_{DDQ}	150	300	µA
Active power-down standby current with clock stop	I_{DD3PS1}	V_{DD1}	1300	2600	µA
	I_{DD3PS2}	V_{DD2}	7.5	15	mA
	$I_{DD3PS,in}$	V_{DDCA}, V_{DDQ}	150	300	µA
Active non-power-down standby current	I_{DD3N1}	V_{DD1}	2	4	mA
	I_{DD3N2}	V_{DD2}	25	50	
	$I_{DD3N,in}$	V_{DDCA}, V_{DDQ}	12	24	
Active non-power-down standby current with clock stopped	I_{DD3NS1}	V_{DD1}	2	4	mA
	I_{DD3NS2}	V_{DD2}	20	40	
	$I_{DD3NS,in}$	V_{DDCA}, V_{DDQ}	6	12	
Operating burst READ current	I_{DD4R1}	V_{DD1}	3	6	mA
	I_{DD4R2}	V_{DD2}	300	600	
	$I_{DD4R,in}$	V_{DDCA}	12	24	
Operating burst WRITE current	I_{DD4W1}	V_{DD1}	3	6	mA
	I_{DD4W2}	V_{DD2}	300	600	
	$I_{DD4W,in}$	V_{DDCA}, V_{DDQ}	45	90	

Parameter Condition	Symbol	Power Supply	1600 (X32)		Unit
			SDP	DDP	
All-bank REFRESH burst current	I_{DD51}	V_{DD1}	20	40	mA
	I_{DD52}	V_{DD2}	150	300	
	I_{DD5IN}	V_{DDCA}, V_{DDQ}	12	24	
All-bank REFRESH average current	I_{DD5AB1}	V_{DD1}	5	10	mA
	I_{DD5AB2}	V_{DD2}	25	50	
	$I_{DD5AB,in}$	V_{DDCA}, V_{DDQ}	12	24	
Per-bank REFRESH average current	I_{DD5PB1}	V_{DD1}	5	10	mA
	I_{DD5PB2}	V_{DD2}	25	50	
	$I_{DD5PB,in}$	V_{DDCA}, V_{DDQ}	12	24	
Self refresh current (Full Array; TC ≦ +85˚C)	I_{DD61} (full Array)	V_{DD1}	1000	2000	µA
	I_{DD62} (full Array)	V_{DD2}	4000	8000	
	I_{DD6IN} (full Array)	V_{DDCA}, V_{DDQ}	120	240	
Self refresh current (1/2 Array; TC ≦ +85˚C)	I_{DD61} (1/2 Array)	V_{DD1}	950	1900	
	I_{DD62} (1/2 Array)	V_{DD2}	2300	4600	
	I_{DD6IN} (1/2 Array)	V_{DDCA}, V_{DDQ}	120	240	
Self refresh current (1/4 Array; TC ≦ +85˚C)	I_{DD61} (1/4 Array)	V_{DD1}	900	1800	
	I_{DD62} (1/4 Array)	V_{DD2}	1500	3000	
	I_{DD6IN} (1/4 Array)	V_{DDCA}, V_{DDQ}	120	240	
Self refresh current (1/8 Array; TC ≦ +85˚C)	I_{DD61} (1/8 Array)	V_{DD1}	850	1700	
	I_{DD62} (1/8 Array)	V_{DD2}	1060	2120	
	I_{DD6IN} (1/8 Array)	V_{DDCA}, V_{DDQ}	120	240	

REFRESH Requirements

LPDDR3 Refresh Requirement Parameters

Parameter		Symbol	4 Gb (SDP)	Unit
Number of Banks			8	-
Refresh Window: Tcase ≦ 85°C		**tREFW**	32	ms
Refresh Window: 1/2-Rate Refresh		**tREFW**	16	ms
Refresh Window: 1/4-Rate Refresh		**tREFW**	8	ms
Required number of REFRESH commands (min)		**R**	8,192	-
average time between REFRESH commands (for reference only) Tcase ≦ 85°C	REFab	**tREFI**	3.9	µs
	REFpb	**tREFIpb**	0.4875	µs
Refresh Cycle time		**tRFCab**	130	ns
Per Bank Refresh Cycle time		**tRFCpb**	60	ns

AC Timing

Notes 1–4 apply to all parameters. Notes begin below table.

Parameter	Symbol	Min/ Max	Data Rate 1600	Unit
Maximum clock frequency	***f*CK**	–	800	MHz
Clock Timing				
Average clock period	**tCK(avg)**	MIN	1.25	ns
		MAX	100	
Average HIGH pulse width	**tCH(avg)**	MIN	0.45	tCK(avg)
		MAX	0.55	
Average LOW pulse width	**tCL(avg)**	MIN	0.45	tCK(avg)
		MAX	0.55	
Absolute clock period	**tCK(abs)**	MIN	*tCK(avg) MIN + tJIT(per) MIN*	ns
Absolute clock HIGH pulse width	**tCH(abs)**	MIN	0.43	tCK(avg)
		MAX	0.57	
Absolute clock LOW pulse width	**tCL(abs)**	MIN	0.43	tCK(avg)
		MAX	0.57	
Clock period jitter (with supported jitter)	**tJIT(per)**, allowed	MIN	-70	ps
		MAX	70	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	**tJIT(cc)**, allowed	MAX	140	ps
Duty cycle jitter (with supported jitter)	**tJIT(duty)**, allowed	MIN	*min((tCH(abs),min - tCH(avg),min),(tCL(abs),min - tCL(avg),min)) × tCK(avg)*	ps
		MAX	*max((tCH(abs),max - tCH(avg),max)(tCL(abs),max - tCL(avg),max)) × tCK(avg)*	
Cumulative errors across 2 cycles	**tERR(2per)**, allowed	MIN	-103	ps
		MAX	103	
Cumulative errors across 3 cycles	**tERR(3per)**, allowed	MIN	-122	ps
		MAX	122	
Cumulative errors across 4 cycles	**tERR(4per)**, allowed	MIN	-136	ps
		MAX	136	
Cumulative errors across 5 cycles	**tERR(5per)**, allowed	MIN	-147	ps
		MAX	147	
Cumulative errors across 6 cycles	**tERR(6per)**, allowed	MIN	-155	ps
		MAX	155	
Cumulative errors across 7 cycles	**tERR(7per)**, allowed	MIN	-163	ps
		MAX	163	
Cumulative errors across 8 cycles	**tERR(8per)**, allowed	MIN	-169	ps
		MAX	169	
Cumulative errors across 9 cycles	**tERR(9per)**, allowed	MIN	-175	ps
		MAX	175	
Cumulative errors across 10 cycles	**tERR(10per)**, allowed	MIN	-180	ps
		MAX	180	
Cumulative errors across 11 cycles	**tERR(11per)**, allowed	MIN	-184	ps
		MAX	184	
Cumulative errors across 12 cycles	**tERR(12per)**, allowed	MIN	-188	ps
		MAX	188	

Parameter	Symbol	Min/ Max	Data Rate 1600	Unit
Clock Timing				
Cumulative errors across n = 13, 14, 15…, 19, 20 cycles	**tERR(nper)**, allowed	MIN	*tERR(nper),allowed MIN = (1 + 0.68ln(n)) ×tJIT(per), allowed MIN*	ps
		MAX	*tERR (nper), allowed MAX = (1 + 0.68ln(n)) ×tJIT(per), allowed MAX*	
ZQ Calibration Parameters				
Initialization calibration time	**tZQINIT**	MIN	1	µs
Long calibration time	**tZQCL**	MIN	360	ns
Short calibration time	**tZQCS**	MIN	90	ns
Calibration RESET time	**tZQRESET**	MIN	max(50ns,3*n*CK)	ns
READ Parameters[5]				
DQS output access time from CK/$\overline{CK}$	**tDQSCK**	MIN	2500	ps
		MAX	5500	
DQSCK delta short	**tDQSCKDS**	MAX	220	ps
DQSCK delta medium	**tDQSCKDM**	MAX	511	ps
DQSCK delta long	**tDQSCKDL**	MAX	614	ps
DQS-DQ skew	**tDQSQ**	MAX	135	ps
DQS output HIGH pulse width	**tQSH**	MIN	*tCH(abs)* - 0.05	tCK(avg)
DQS output LOW pulse width	**tQSL**	MIN	*tCL(abs)* - 0.05	tCK(avg)
DQ/DQS output hold time from DQS	**tQH**	MIN	min(*t*QSH, *t*QSL)	ps
READ preamble	**tRPRE**	MIN	0.9	tCK(avg)
READ postamble	**tRPST**	MIN	0.3	tCK(avg)
DQS Low-Z from clock	**tLZ(DQS)**	MIN	*t*DQSCK (MIN) - 300	ps
DQ Low-Z from clock	**tLZ(DQ)**	MIN	*t*DQSCK,(MIN) - 300	ps
DQS High-Z from clock	**tHZ(DQS)**	MAX	*t*DQSCK,(MAX) - 100	ps
DQ High-Z from clock	**tHZ(DQ)**	MAX	*t*DQSCK,(MAX) + (1.4 × *t*DQSQ,(MAX))	ps
WRITE Parameters[5]				
DQ and DM input hold time (VREF based)	**tDH**	MIN	150	ps
DQ and DM input setup time (VREF based)	**tDS**	MIN	150	ps
DQ and DM input pulse width	**tDIPW**	MIN	0.35	tCK(avg)
Write command to 1st DQS latching transition	**tDQSS**	MIN	0.75	tCK(avg)
		MAX	1.25	
DQS input high-level width	**tDQSH**	MIN	0.4	tCK(avg)
DQS input low-level width	**tDQSL**	MIN	0.4	tCK(avg)
DQS falling edge to CK setup time	**tDSS**	MIN	0.2	tCK(avg)
DQS falling edge hold time from CK	**tDSH**	MIN	0.2	tCK(avg)
Write postamble	**tWPST**	MIN	0.4	tCK(avg)
Write preamble	**tWPRE**	MIN	0.8	tCK(avg)
CKE Input Parameters				
CKE minimum pulse width (HIGH and LOW pulse width)	**tCKE**	MIN	max(7.5ns,3*n*CK)	ns
CKE input setup time	**tISCKE**	MIN	0.25	tCK(avg)
CKE input hold time	**tIHCKE**	MIN	0.25	tCK(avg)
Command path disable delay	**tCPDED**	MIN	2	tCK(avg)
Command Address Input Parameters[5]				
Address and control input setup time	**tISCA**	MIN	150	ps
Address and control input hold time	**tIHCA**	MIN	150	ps
$\overline{CS}$ input setup time	**tISCS**	MIN	270	ps
$\overline{CS}$ input hold time	**tIHCS**	MIN	270	ps

Parameter	Symbol	Min/ Max	Data Rate 1600	Unit
Command Address Input Parameters[5]				
Address and control input pulse width	**tIPWCA**	MIN	0.35	tCK(avg)
$\overline{CS}$ input pulse width	**tIPWCS**	MIN	0.7	tCK(avg)
Boot Parameters (10 MHz–55 MHz) [16, 17, 18]				
Clock cycle time	**tCK**b	MAX	100	ns
		MIN	18	
CKE input setup time	**tISCKE**b	MIN	2.5	ns
CKE input hold time	**tIHCKE**b	MIN	2.5	ns
Address and control input setup time	**tIS**b	MIN	1150	ps
Address and control input hold time	**tIH**b	MIN	1150	ps
DQS output data access time from CK/$\overline{CK}$	**tDQSCK**b	MIN	2	ns
		MAX	10	
Data strobe edge to output data edge	**tDQSQ**b	MAX	1.2	ns
Mode Register Parameters				
MODE REGISTER WRITE command period	**tMRW**	MIN	10	tCK(avg)
MODE REGISTER READ command period	**tMRR**	MIN	4	tCK(avg)
Additional time after tXP has expired until the MRR command may be issued	**tMRRI**	MIN	*t*RCD(min)	ns
Core Parameters [19]				
READ latency	**RL**	MIN	12	tCK(avg)
WRITE latency(Set A)	**WL**	MIN	6	tCK(avg)
WRITE latency(Set B)	**WL**	MIN	9	tCK(avg)
ACTIVATE-to- ACTIVATE command period	**tRC**	MIN	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)	ns
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	**tCKESR**	MIN	max(15ns,3*n*CK)	ns
SELF REFRESH exit to next valid command delay	**tXSR**	MIN	max(*t*RFCab + 10ns,2*n*CK)	ns
Exit power- down to next valid command delay	**tXP**	MIN	max(7.5ns,3*n*CK)	ns
CAS-to-CAS delay	**tCCD**	MIN	4	tCK(avg)
Internal READ to PRECHARGE command delay	**tRTP**	MIN	max(7.5ns,4*n*CK)	ns
RAS-to-CAS delay	**tRCD** (fast)	MIN	max(15ns,3*n*CK)	ns
	tRCD (typ)		max(18ns,3*n*CK)	
	tRCD (slow)		max(24ns,3*n*CK)	
Row precharge time (single bank)	**tRP**pb (fast)	MIN	max(15ns,3*n*CK)	ns
	tRPpb (typ)		max(18ns,3*n*CK)	
	tRPpb (slow)		max(24ns,3*n*CK)	
Row precharge time (all banks)	**tRP**pab (fast)	MIN	max(18ns,3*n*CK)	ns
	tRPpab (typ)		max(21ns,3*n*CK)	
	tRPpab (slow)		max(27ns,3*n*CK)	
Row active time	**tRAS**	MIN	max(42ns,3*n*CK)	ns
		MAX	70	µs
WRITE recovery time	**tWR**	MIN	max(15ns,4*n*CK)	ns
Internal WRITE-to- READ command delay	**tWTR**	MIN	max(7.5ns,4*n*CK)	ns
Active bank A to active bank B	**tRRD**	MIN	max(10ns,2*n*CK)	ns
Four-bank ACTIVATE window	**tFAW**	MIN	max(50ns,8*n*CK)	ns
Minimum deep power- down time	**tDPD**	MIN	500	µs

Parameter	Symbol	Min/ Max	Data Rate 1600	Unit
ODT Parameters				
Asynchronous R_{TT} turn-on dely from ODT input	**tODT**on	MIN	1.75	ns
		MAX	3.5	
Asynchronous R_{TT} turn-off delay from ODT input	**tODT**off	MIN	1.75	ns
		MAX	3.5	
Automatic R_{TT} turn-on delay after READ data	**tAODT**on	MAX	*t*DQSCK + 1.4 × *t*DQSQ,max + *t*CK(avg,min)	ps
Automatic R_{TT} turn-off delay after READ data	**tAODT**off	MIN	*t*DQSCK,min - 300	ps
R_{TT} disable delay from power down, self-refresh, and deep power down entry	**tODT**d	MIN	12	ns
R_{TT} enable delay from power down and self refresh exit	**tODT**e	MAX	12	ns
CA Training Parameters				
First CA calibration command after CA calibration mode is programmed	**tCAMRD**	MIN	20	tCK(avg)
First CA calibration command after CKE is LOW	**tCAENT**	MIN	10	tCK(avg)
CA caibration exit command after CKE is HIGH	**tCAEXT**	MIN	10	tCK(avg)
CKE LOW after CA calibration mode is programmed	**tCACKEL**	MIN	10	tCK(avg)
CKE HIGH after the last CA calibration results are driven.	**tCACKEH**	MIN	10	tCK(avg)
Data out delay after CA training calibration command is programmed	**tADR**	MAX	20	ns
MRW CA exit command to DQ tri-state	**tMRZ**	MIN	3	ns
CA calibration command to CA calibration command delay	**tCACD**	MIN	RU(*t*ADR+2 × *t*CK)	tCK(avg)
Write Leveling Parameters				
DQS/$\overline{\text{DQS}}$ delay after write leveling mode is programmed	**tWLDQSEN**	MIN	25	ns
		MAX	—	
First DQS/$\overline{\text{DQS}}$ edge after write leveling mode is programmed	**tWLMRD**	MIN	40	ns
		MAX	—	
Write leveling output delay	**tWLO**	MIN	0	ns
		MAX	20	
Write leveling hold time	**tWLH**	MIN	175	ps
Write leveling setup time	**tWLS**	MIN	175	ps
Mode register set command delay	**tMRD**	MIN	MAX (14ns, 10nCK)	ns
		MAX	—	
Temperature Derating				
DQS output access time from CK/$\overline{\text{CK}}$ (derated)	**tDQSCK**	MAX	5620	ps
RAS-to-CAS delay (derated)	**tRCD**	MIN	*t*RCD + 1.875	ns
ACTIVATE-to-ACTIVATE command period (derated)	**tRC**	MIN	*t*RC + 1.875	ns
Row active time (derated)	**tRAS**	MIN	*t*RAS + 1.875	ns
Row precharge time (derated)	**tRP**	MIN	*t*RP + 1.875	ns
Active bank A to active bank B (derated)	**tRRD**	MIN	*t*RRD + 1.875	ns

NOTE 1 Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.

NOTE 2 All AC timings assume an input slew rate of 2V/ns for single-ended signals.

NOTE 3 Measured with 4 V/ns differential CK/$\overline{\text{CK}}$ slew rate and nominal VIX.

NOTE 4 All timing and voltage measurements are defined at the ball.

NOTE 5 READ, WRITE, and input setup and hold values are referenced to VREF.

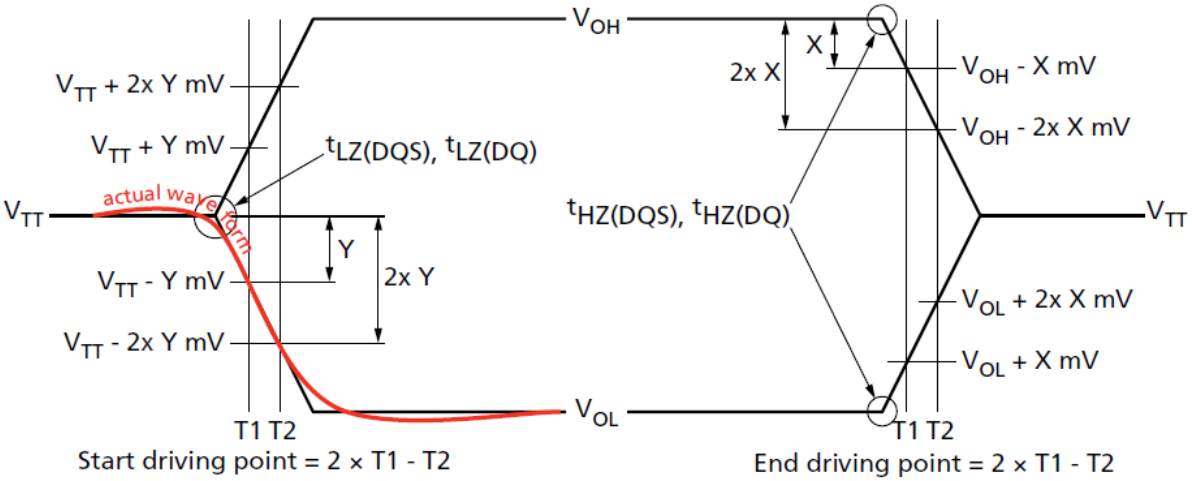
NOTE 6 tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.

NOTE 7 tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.

NOTE 8 tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.

NOTE 9 For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS) and tLZ(DQ)). The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ) or begins driving tLZ(DQS) and tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

NOTE 10 Output Transition Timing



NOTE 11 The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS/$\overline{\text{DQS}}$.

NOTE 12 Measured from the point when DQS/$\overline{\text{DQS}}$ begins driving the signal, to the point when DQS/$\overline{\text{DQS}}$ begins driving the first rising strobe edge.

NOTE 13 Measured from the last falling strobe edge of DQS/$\overline{\text{DQS}}$ to the point when DQS/$\overline{\text{DQS}}$ finishes driving the signal.

NOTE 14 CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK/$\overline{\text{CK}}$ crossing.

NOTE 15 CKE input hold time is measured from CK/$\overline{\text{CK}}$ crossing to CKE reaching a HIGH/LOW voltage level.

NOTE 16 Input setup/hold time for signal (CA[9:0], $\overline{\text{CS}}$).

NOTE 17 To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).

NOTE 18 Mobile LPDDR3 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.

NOTE 19 The output skew parameters are measured with default output impedance settings using the reference load.

NOTE 20 The minimum tCK column applies only when tCK is greater than 6ns.

CA Setup and Hold Base-Values

unit [ps]	Data Rate	reference
	1600	
*t*ISCA(base)	75	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-150mV
*t*IHCA(base)	100	$V_{IH/L(dc)} = V_{REF(dc)}$ +/-100mV

NOTE 1 AC/DC referenced for 2V/ns CA slew rate and 4V/ns differential CK-$\overline{CK}$ slew rate.

$\overline{CS}$ Setup and Hold Base-Values

unit [ps]	Data Rate	reference
	1600	
*t*ISCS(base)	195	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-150mV
*t*IHCS(base)	220	$V_{IH/L(dc)} = V_{REF(dc)}$ +/-100mV

NOTE 1 AC/DC referenced for 2V/ns $\overline{CS}$ slew rate and 4V/ns differential CK-$\overline{CK}$ slew rate.

Derating values tIS/tIH - ac/dc based AC150

ΔtISCA, ΔtIHCA, ΔtISCS, ΔtIHCS derating in [ps] AC/DC based AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV													
		CK, $\overline{CK}$ Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA,$\overline{CS}$ Slew rate (V/ns)	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1 Cell contents shaded in pink are defined as 'not supported'.

Required time *t*VAC above *V*IH(ac) {below *V*IL(ac)} for valid transition for CA

Slew Rate (V/ns)	tVAC at 150mV (ps) 1600Mb/s	
	Min	Max
>4.0	48	—
4.0	48	—
3.5	46	—
3.0	43	—
2.5	40	—
2.0	35	—
1.5	27	—
<1.5	27	—

Data Setup and Hold Base-Values (>400MHz, 1V/ns Slew Rate)

unit [ps]	Data Rate	reference
	1600	
tDS(base)	75	$V_{IH/L(ac)} = V_{REF(dc)}$ +/- 150mV
tDH(base)	100	$V_{IH/L(dc)} = V_{REF(dc)}$ +/- 100mV

NOTE 1 AC/DC referenced for 2V/ns DQ, DM slew rate and 4V/ns differential DQS-$\overline{DQS}$ slew rate and nominal V_{IX}.

Derating values tDS/tDH - ac/dc based AC150

ΔtDS, ΔtDH derating in [ps] AC/DC based AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV													
		DQS, $\overline{DQS}$ Differential Slew Rate											
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew rate (V/ns)	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1 Cell contents shaded in pink are defined as 'not supported'.

Required time *t*VAC above *V*IH(ac) {below *V*IL(ac)} for valid transition for DQ, DM

Slew Rate (V/ns)	tVAC at 150mV (ps) 1600Mb/s	
	Min	Max
>4.0	48	—
4.0	48	—
3.5	46	—
3.0	43	—
2.5	40	—
2.0	35	—
1.5	27	—
<1.5	27	—

Initialization Timing Parameters

Symbol	Parameter	Value		Unit
		min	max	
^{t}INIT0	Maximum Power Ramp Time	-	20	ms
^{t}INIT1	Minimum CKE low time after completion of power ramp	100	-	ns
^{t}INIT2	Minimum stable clock before first CKE high	5	-	tCK
^{t}INIT3	Minimum idle time after first CKE assertion	200	-	us
^{t}INIT4	Minimum idle time after Reset command	1	-	us
^{t}INIT5[1]	Maximum duration of Device Auto-Initialization	-	10	us
^{t}ZQINIT	ZQ Initial Calibration	1	-	us
^{t}CKb	Clock cycle time during boot	18	100	ns

NOTE 1 If DAI bit is not read via MRR, SDRAM will be in idle state after tINIT5(max) has expired.

Power-Off Timing

Symbol	Parameter	Min	Max	Unit
tPOFF	Maximum power-off ramp time	-	2	s

Mode Register Assignment

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info	R	RL3	WL-B	(RFU)	RZQI		(RFU)		DAI
1	01_H	Device Feature1	W	nWR (for AP)			(RFU)		BL		
2	02_H	Device Feature2	W	WRLev	WL Sel	(RFU)	nWRE		RL & WL		
3	03_H	I/O Config-1	W	(RFU)					DS		
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11	$0B_H$	ODT	W	(RFU)					PD ctl	DQ ODT	
12-15	$0C_H$-$0F_H$	(Reserved)	—	(RFU)							
16	10_H	PASR_BANK	W	PASR Bank Mask							
17	11_H	PASR_Seg	W	PASR Segment Mask							
18-31	12_H-$1F_H$	(Reserved)	—	(RFU)							
32	20_H	DQ calibration pattern A	R	See Data Calibration Pattern Description							
33-39	21_H-27_H	(Do Not Use)	—	(DNU)							
40	28_H	DQ calibration pattern B	R	See Data Calibration Pattern Description							
41	29_H	CA Training 1	W	See MRW – CA Training Mode							
42	$2A_H$	CA Training 2	W	See MRW – CA Training Mode							
43-47	$2B_H$-$2F_H$	(Do Not Use)	—	(DNU)							
48	30_H	CA Training 3	W	See MRW – CA Training Mode							
49-62	31_H-$3E_H$	(Reserved)	—	(RFU)							
63	$3F_H$	RESET	W	X or 0xFCh							
64-255	40_H-FF_H	(Reserved)	—	(RFU)							

NOTE 1 RFU bits shall be set to '0' during mode register writes.

NOTE 2 RFU bits shall be read as '0' during mode register reads.

NOTE 3 All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS, $\overline{DQS}$ shall be toggled.

NOTE 4 All mode registers that are specified as RFU shall not be written.

NOTE 5 See vendor device datasheets for details on vendor-specific mode registers.

NOTE 6 Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA[7:0] = 00_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info	R	RL3	WL-B	(RFU)	RZQI		(RFU)		DAI

Feature	Register Information	Type	OP	Definition
DAI	Device Auto-Initialization Status	Read-only	OP<0>	**0_B:** DAI complete **1_B:** DAI still in progress
RZQI[1-4]	RZQI (Built in Self Test for RZQ Information)	Read-only	OP<4:3>	**00_B:** RZQ self test not supported **01_B:** ZQ-pin may connect to V_{DDCA} or float **10_B:** ZQ-pin may short to GND **11_B:** ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to V_{DDCA} or float nor short to GND)
WL-B	WL (Set B) Support	Read-only	OP<6>	**0B**: DRAM does not support WL (Set B) **1B**: DRAM supports WL (SetB)
RL3	RL3 Option Support	Read-only	OP<7>	**0_B**: DRAM does not support RL=3, nWR=3, WL=1 **1_B**: DRAM supports RL=3, nWR=3, WL=1 for frequencies ≤ 166

NOTE 1 RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.

NOTE 2 If ZQ is connected to V_{DDCA} to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to V_{DDCA}, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 3 In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for R_{ON}, and will ignore ZQ calibration commands. In either case, the system may not function as intended.

NOTE 4 In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-Ω ±1%).

MR1_Device Feature 1 (MA[7:0] = 01_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
1	01_H	Device Feature1	W	nWR (for AP)			(RFU)		BL		

Feature	Type	OP	Definition
BL	Write-only	OP<2:0>	**011_B:** BL8 (default) All others: reserved
nWR (for AP)	Write -only	OP<7:5>	If *n*WRE (MR2 OP<4>) = 0: **001_B**: *n*WR=3 (default) **100_B**: *n*WR=6 **110_B**: *n*WR=8 **111_B**: *n*WR=9 If *n*WRE (MR2 OP<4> = 1: **000_B**: *n*WR=10 **001_B**: *n*WR=11 **010_B**: *n*WR=12 All others: reserved

NOTE 1 Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Burst Sequence

C2	C1	C0	BL	Burst Cycle Number and Burst Address Sequence							
				1	2	3	4	5	6	7	8
0_B	0_B	0_B	8	0	1	2	3	4	5	6	7
0_B	1_B	0_B		2	3	4	5	6	7	0	1
1_B	0_B	0_B		4	5	6	7	0	1	2	3
1_B	1_B	0_B		6	7	0	1	2	3	4	5

1. C0 input is not present on CA bus. It is implied zero.
2. The burst address represents C2 - C0.

MR2_Device Feature 2 (MA[7:0] = 02_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
2	02_H	Device Feature2	W	WRLev	WL Sel	(RFU)	nWRE	RL & WL			

Feature	Type	OP	Definition
RL & WL	Write-only	OP<3:0>	If OP<6> =0 (WL Set A, default) **0001B**: RL = 3 / WL = 1 (≦166 MHz) **0100B**: RL = 6 / WL = 3 (≦400 MHz) **0110B**: RL = 8 / WL = 4 (≦533 MHz) **0111B**: RL = 9 / WL = 5 (≦600 MHz) **1000B**: RL = 10 / WL = 6 (≦667 MHz, default) **1001B**: RL = 11 / WL = 6 (≦733 MHz) **1010B**: RL = 12 / WL = 6 (≦800 MHz) **1100B**: RL = 14 / WL = 8 (≦933 MHz) All others: reserved If OP<6> =1 (WL Set B) **0001B**: RL = 3 / WL = 1 (≦166 MHz) **0100B**: RL = 6 / WL = 3 (≦400 MHz) **0110B**: RL = 8 / WL = 4 (≦533 MHz) **0111B**: RL = 9 / WL = 5 (≦600 MHz) **1000B**: RL = 10 / WL = 8 (≦667 MHz) **1001B**: RL = 11 / WL = 9 (≦733 MHz) **1010B**: RL = 12 / WL = 9 (≦800 MHz) All others: reserved
nWRE	Write-only	OP<4>	**0B:** enable *n*WR programming ≦9 **1B:** enable *n*WR programming > 9 (default)
WL Selection	Write-only	OP<6>	**0B:** Select WL Set A (default) **1B:** Select WL Set B
WR Leveling	Write-only	OP<7>	**0B:** disabled (default) **1B:** enabled

NOTE 1 See MR0, OP<7>

NOTE 2 See MR0, OP<6>

MR3_I/O Configuration 1 (MA[7:0] = 03_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
3	03_H	I/O Config-1	W	(RFU)				DS			

Feature	Type	OP	Definition
Drive Strength	Write-only	OP<3:0>	**0000_B:** reserved **0001_B:** 34.3Ω typical **0010_B:** 40Ω typical (default) **0011_B:** 48Ω typical **0100_B:** 60Ω typical **0110_B:** 80Ω typical **1001_B:** 34.3Ω pull-down, 40Ω pull-up (240Ω termination) **1010_B:** 40Ω pull-down, 48Ω pull-up (240Ω termination) **1011_B:** 34.3Ω pull-down, 48Ω pull-up (120Ω termination) **All others:** reserved

MR4_Device Temperature (MA[7:0] = 04_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		

Feature	Type	OP	Definition
Refresh Rate	Read-only	OP<2:0>	**000B:** SDRAM Low temperature operating limit exceeded **001B:** 4x tREFI, 4x tREFIpb, 4x tREFW **010B:** 2x tREFI, 2x tREFIpb, 2x tREFW **011B:** 1x tREFI, 1x tREFIpb, 1x tREFW (≦85℃) **100B:** reserved **101B:** 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, no AC timing derating **110B:** 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, timing derating required **111B:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0B:** OP<2:0> value has not changed since last read of MR4. **1B:** OP<2:0> value has changed since last read of MR4.

NOTE 1 A mode register read from MR4 will reset OP7 to 0.

NOTE 2 OP7 is reset to 0 at power-up.

NOTE 3 If OP2 = 1, the device temperature is greater than 85˚C.

NOTE 4 OP7 is set to 1 if OP<2:0> has changed at any time since the last MR4 read.

NOTE 5 The device might not operate properly when OP<2:0> = 000b or 111b.

NOTE 6 For the specified operating temperature range and maximum operating temperature, refer to the Operating Temperature Range table.

NOTE 7 LPDDR3 devices must be derated by adding 1.875ns to the following core timing parameters:tRCD, tRC, tRAS, tRP, and tRRD. The tDQSCK parameter must be derated as specified in the AC Timing table. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.

NOTE 8 The recommended frequency for reading MR4 is provided in the Temperature Sensor section.

MR5_Basic Configuration-1 (MA[7:0] = 05_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
5	05_H	Basic Config-1	R	Manufacturer ID							

Feature	Type	OP	Definition
Manufactuer ID	Read-only	OP<7:0>	**0000 0101B:** Nanya **All Others:** Reserved

MR6_Basic Configuration-2 (MA[7:0] = 06_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
6	06_H	Basic Config-2	R	Revision ID1							

Feature	Type	OP	Definition
Revision ID1	Read-only	OP<7:0>	**0000 0000B:** A Version **All Others:** Reserved

MR7_Basic Configuration-3 (MA[7:0] = 07_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
7	07_H	Basic Config-3	R	Revision ID2							

Feature	Type	OP	Definition
Revision ID2	Read-only	OP<7:0>	**0000 0000B:** A Version **All Others:** Reserved

MR8_Basic Configuration-4 (MA[7:0] = 08H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
8	08_H	Basic Config-4	R	I/O width		Density				Type	

Feature	Type	OP	Definition
Type	Read-only	OP<1:0>	**11B:** LPDDR3 S8 **All others:** Reserved
Density	Read-only	OP<5:2>	**0110B:** 4Gb **0111B:** 8Gb **1000B:** 16Gb **1001B:** 32Gb **All others:** Reserved
I/O width	Read-only	OP<7:6>	**00B:** x32 **01B:** x16 **All others:** Reserved

MR9_Test Mode (MA<7:0> = 09H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
9	09_H	Test Mode	W	Vendor-Specific Test Mode							

MR10_Calibration (MA[7:0] = $0A_H$)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
10	$0A_H$	IO Calibration	W	Calibration Code							

Feature	Type	OP	Definition
Calibration Code	Write-only	OP<7:0>	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **All Others:** Reserved

NOTE 1 Host processor shall not write MR10 with "Reserved" values.

NOTE 2 The device ignores calibration commands when a reserved value is written into MR10.

NOTE 3 See AC Timing table for the calibration latency.

NOTE 4 If ZQ is connected to VSS through RZQ, either the ZQ calibration function (see MRW ZQ CALIBRATION Command) or default calibration (through the ZQ RESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration and ZQ CALIBRATION commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.

NOTE 5 Devices that do not support calibration ignore the ZQ CALIBRATION command.

NOTE 6 The MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11_ODT (MA[7:0] = $0B_H$)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
11	$0B_H$	ODT	W	(RFU)					PD ctl	DQ ODT	

Feature	Type	OP	Definition
DQ ODT[1]	Write-only	OP<1:0>	**00B:** Disable (Default) **01B:** Reserved **10B:** *RZQ*/2 **11B:** *RZQ*/1
PD Control	Write-only	OP<2>	**0B:** ODT disabled by DRAM during power down (default) **1B:** ODT enabled by DRAM during power down

NOTE 1 Depending on ballout, ODT pin may be NOT supported so ODT die pad is connected to Vss inside the package.

MR12-15_Reserved (MA[7:0] = $0C_H$-$0F_H$)

MR16_PASR_BANK (MA[7:0] = 10_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_BANK	W	PASR Bank Mask							

Feature	Type	OP	Definition
PASR Bank Mask	Write-only	OP<7:0>	**0B:** refresh enable to the bank (= unmasked, default) **1B:** refresh blocked (= masked)

OP	Bank Mask	LPDDR3 SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	XXX1XXXX	Bank 4
5	XX1XXXXX	Bank 5
6	X1XXXXXX	Bank 6
7	1XXXXXXX	Bank 7

MR17_PASR_Segment (MA[7:0] = 11_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
17	11_H	PASR_Seg	W	PASR Segment Mask							

Feature	Type	OP	Definition
PASR Segment Mask	Write-only	OP<7:0>	**0B:** refresh enable to the segment (=unmasked, default) **1B:** refresh blocked (=masked)

Segment	OP	Segment Mask	4Gb	8Gb	16Gb	32Gb
			R13:11	R14:12	R14:12	TBD
0	0	XXXXXXX1	000_B			
1	1	XXXXXX1X	001_B			
2	2	XXXXX1XX	010_B			
3	3	XXXX1XXX	011_B			
4	4	XXX1XXXX	100_B			
5	5	XX1XXXXX	101_B			
6	6	X1XXXXXX	110_B			
7	7	1XXXXXXX	111_B			

NOTE 1 This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.
NOTE 2 No memory present at addresses with R13=R14=HIGH. Segment masks 6 and 7 are ignored.

MR18-31_Reserved (MA[7:0] = 12_H.$1F_H$)

MR32_DQ Calibration Pattern A (MA[7:0] = 20_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20_H	DQ calibration pattern A	R	See Data Calibration Pattern Description							

NOTE 1 Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration"

MR33-39_Do Not Use (MA[7:0] = 21_H.27_H)

MR40_DQ Calibration Pattern B (MA[7:0] = 28_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
40	28_H	DQ calibration pattern B	R	See Data Calibration Pattern Description							

NOTE 1 Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration"

MR41_CA Training 1 (MA[7:0] = 29_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
41	29_H	CA Training 1	W	See MRW – CA Training Mode							

NOTE 1 Writes to MR41 enables CA Training. See Mode Register Write - CA Training Mode

MR42_CA Training 2 (MA[7:0] = $2A_H$)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
42	$2A_H$	CA Training 2	W	See MRW – CA Training Mode							

NOTE 1 Writes to MR42 enables CA Training. See Mode Register Write - CA Training Mode

MR43-47_Do Not Use (MA[7:0] = $2B_H$.$2F_H$)

MR48_CA Training 3 (MA[7:0] = 30_H)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
48	30_H	CA Training 3	W	See MRW – CA Training Mode							

NOTE 1 Writes to MR48 enables CA Training. See Mode Register Write - CA Training Mode

MR49-62_Do Not Use (MA[7:0] = 31_H.$3E_H$)

MR63_RESET (MA[7:0] = $3F_H$)

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
63	$3F_H$	RESET	W	X or 0xFCh							

MR64-255_Reserved (MA[7:0] = 40_H.FF_H)

Revision History

Rev	Page	Modified	Description	Released
1.0	-	-	Preliminary Release	11/2015
1.1	P26-45	Power-on/off sequence & Timing Diagrams	New	04/2016
1.2	P1-4,6,9,12	-	Add P/N: NM3488KSLAXA7-3D	09/2016
	P4	Package Outline Drawing	Update	
	P26	Partial Page Program	New	

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