

## 74F579

# 8-Bit Bidirectional Binary Counter with 3-STATE Outputs

### General Description

The 74F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-STATE I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

### Features

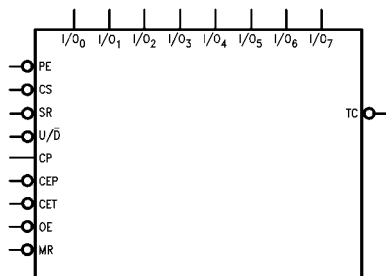
- Multiplexed 3-STATE I/O ports
- Built-in lookahead carry capability
- Count frequency 100 MHz typical
- Supply current 75 mA typical
- Guaranteed 4000V minimum ESD protection

### Ordering Code:

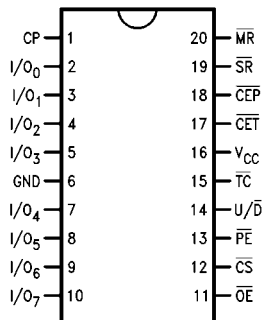
| Order Number | Package Number | Package Description                                                        |
|--------------|----------------|----------------------------------------------------------------------------|
| 74F579SC     | M20B           | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74F579SJ     | M20D           | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide              |
| 74F579PC     | N20A           | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide      |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



74F579 8-Bit Bidirectional Binary Counter with 3-STATE Outputs

## Unit Loading/Fan Out

| Pin Names        | Description                              | U.L.<br>HIGH/LOW   | Input $I_{IH}/I_{IL}$<br>Output $I_{OH}/I_{OL}$ |
|------------------|------------------------------------------|--------------------|-------------------------------------------------|
| $I/O_0-I/O_7$    | Data Inputs or<br>3-STATE Outputs        | 3.5/0.333<br>75/15 | 70 $\mu$ A/-0.2 mA<br>-3 mA/24 mA               |
| $\overline{PE}$  | Parallel Enable Input (Active LOW)       | 0.25/0.333         | 5 $\mu$ A/-0.2 mA                               |
| $U/\overline{D}$ | Up-Down Count Control Input              | 0.25/0.333         | 5 $\mu$ A/-0.2 mA                               |
| $\overline{MR}$  | Master Reset Input (Active LOW)          | 0.25/0.333         | 5 $\mu$ A/-0.2 mA                               |
| $\overline{SR}$  | Synchronous Reset Input (Active LOW)     | 0.25/0.333         | 5 $\mu$ A/-0.2 mA                               |
| $\overline{CEP}$ | Count Enable Parallel Input (Active LOW) | 0.25/0.333         | 5 $\mu$ A/-0.2 mA                               |
| $\overline{CET}$ | Count Enable Trickle Input (Active LOW)  | 0.25/0.333         | 5 $\mu$ A/-0.2 mA                               |
| $\overline{CS}$  | Chip Select Input Active (Active LOW)    | 0.25/0.333         | 5 $\mu$ A/-0.2 mA                               |
| $\overline{OE}$  | Output Enable Input (Active LOW)         | 0.25/0.333         | 5 $\mu$ A/-0.2 mA                               |
| CP               | Clock Pulse Input (Active Rising Edge)   | 0.25/0.333         | 5 $\mu$ A/-0.2 mA                               |
| $\overline{TC}$  | Terminal Count Output (Active LOW)       | 25/12.5            | -1 mA/5 mA                                      |

## Function Table

| $\overline{MR}$ | $\overline{SR}$ | $\overline{CS}$ | $\overline{PE}$ | $\overline{CEP}$ | $\overline{CET}$ | $U/\overline{D}$ | $\overline{OE}$ | CP         | Function                                                 |
|-----------------|-----------------|-----------------|-----------------|------------------|------------------|------------------|-----------------|------------|----------------------------------------------------------|
| X               | X               | H               | X               | X                | X                | X                | X               | X          | $I/O_a$ to $I/O_h$ in High Z ( $\overline{PE}$ Disabled) |
| X               | X               | L               | H               | X                | X                | X                | H               | X          | $I/O_a$ to $I/O_h$ in High Z                             |
| X               | X               | L               | H               | X                | X                | X                | L               | X          | Flip-Flop Outputs Appear on I/O Lines                    |
| L               | X               | X               | X               | X                | X                | X                | X               | X          | Asynchronous Reset for all Flip-Flops                    |
| H               | L               | X               | X               | X                | X                | X                | X               | $\nearrow$ | Synchronous Reset for all Flip-Flops                     |
| H               | H               | L               | L               | X                | X                | X                | X               | $\nearrow$ | Parallel Load all Flip-Flops                             |
| H               | H               | (Not LL)        | H               | X                | X                | X                | X               | $\nearrow$ | Hold                                                     |
| H               | H               | (Not LL)        | X               | H                | X                | X                | X               | $\nearrow$ | Hold ( $\overline{TC}$ Held HIGH)                        |
| H               | H               | (Not LL)        | L               | L                | H                | X                | X               | $\nearrow$ | Count Up                                                 |
| H               | H               | (Not LL)        | L               | L                | L                | X                | X               | $\nearrow$ | Count Down                                               |

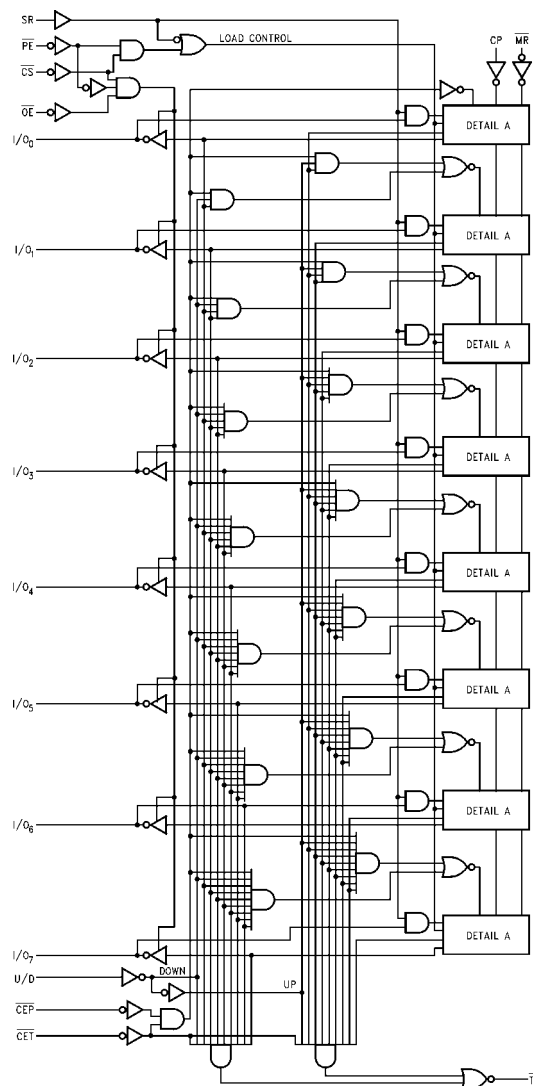
H = HIGH Voltage Level

L = LOW Voltage Level

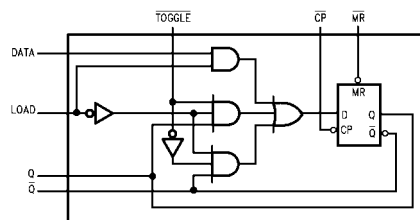
X = Immaterial

 $\nearrow$  = LOW to HIGH Clock TransitionNot LL =  $\overline{CS}$  and  $\overline{PE}$  should never both be LOW voltage level at the same time.

## Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



$V_{CC}$  = Pin 16

GND = Pin 6

() = Pin Numbers

**Detail A**

**Absolute Maximum Ratings**(Note 1)

|                                                                        |                                      |
|------------------------------------------------------------------------|--------------------------------------|
| Storage Temperature                                                    | –65°C to +150°C                      |
| Ambient Temperature under Bias                                         | –55°C to +125°C                      |
| Junction Temperature under Bias                                        | –55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                            | –0.5V to +7.0V                       |
| Input Voltage (Note 2)                                                 | –0.5V to +7.0V                       |
| Input Current (Note 2)                                                 | –30 mA to +5.0 mA                    |
| Voltage Applied to Output<br>in HIGH State (with V <sub>CC</sub> = 0V) |                                      |
| Standard Output                                                        | –0.5V to V <sub>CC</sub>             |
| 3-STATE Output                                                         | –0.5V to +5.5V                       |
| Current Applied to Output<br>in LOW State (Max)                        | twice the rated I <sub>OL</sub> (mA) |
| ESD Last Passing Voltage (Min)                                         | 4000V                                |

**Recommended Operating Conditions**

|                              |                |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C   |
| Supply Voltage               | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

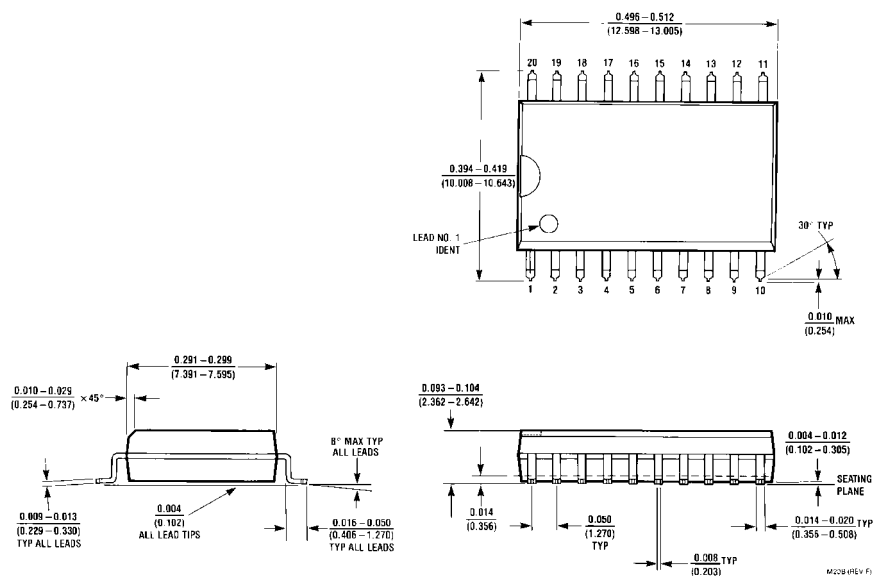
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

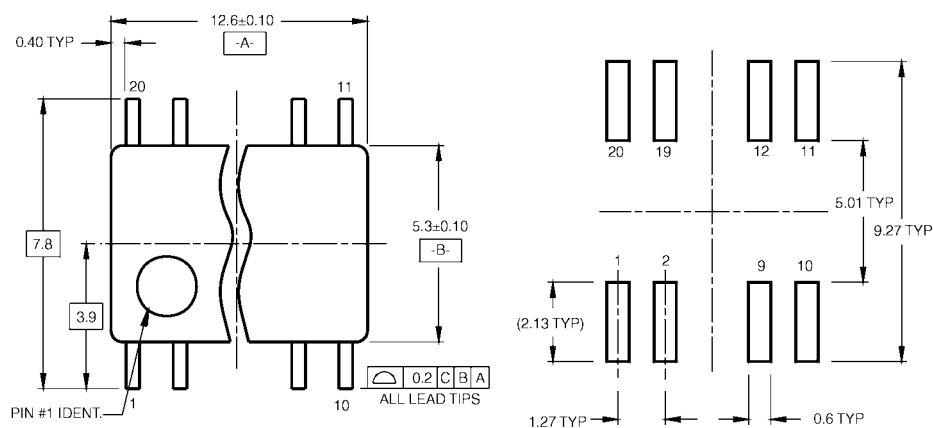
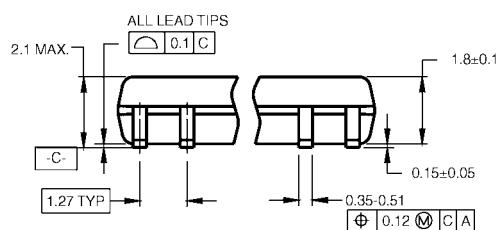
| Symbol                             | Parameter                          | Min                                       | Typ        | Max        | Units | V <sub>CC</sub> | Conditions                                                                                                                                                                       |
|------------------------------------|------------------------------------|-------------------------------------------|------------|------------|-------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>IH</sub>                    | Input HIGH Voltage                 | 2.0                                       |            |            | V     |                 | Recognized as a HIGH Signal                                                                                                                                                      |
| V <sub>IL</sub>                    | Input LOW Voltage                  |                                           |            | 0.8        | V     |                 | Recognized as a LOW Signal                                                                                                                                                       |
| V <sub>CD</sub>                    | Input Clamp Diode Voltage          |                                           |            | –1.2       | V     | Min             | I <sub>IN</sub> = –18 mA                                                                                                                                                         |
| V <sub>OH</sub>                    | Output HIGH Voltage                | 10% V <sub>CC</sub><br>5% V <sub>CC</sub> | 2.4<br>2.7 |            | V     | Min             | I <sub>OH</sub> = –3 mA                                                                                                                                                          |
| V <sub>OL</sub>                    | Output LOW Voltage                 | 10% V <sub>CC</sub><br>5% V <sub>CC</sub> |            | 0.5<br>0.5 | V     | Min             | I <sub>OL</sub> = 20 mA (T <sub>C</sub> ), I <sub>OL</sub> = 24 mA (I/O <sub>n</sub> )<br>I <sub>OL</sub> = 20 mA (T <sub>C</sub> ), I <sub>OL</sub> = 24 mA (I/O <sub>n</sub> ) |
| I <sub>IH</sub>                    | Input HIGH Current                 |                                           |            | 5.0        | μA    | Max             | V <sub>IN</sub> = 2.7V (Non-I/O Pins)                                                                                                                                            |
| I <sub>BVI</sub>                   | Input HIGH Current Breakdown Test  |                                           |            | 7.0        | μA    | Max             | V <sub>IN</sub> = 7.0V (Non-I/O Pins)                                                                                                                                            |
| I <sub>BVIT</sub>                  | Input HIGH Current Breakdown (I/O) |                                           |            | 0.5        | mA    | Max             | V <sub>IN</sub> = 5.5V (I/O <sub>n</sub> )                                                                                                                                       |
| I <sub>CEX</sub>                   | Output HIGH Leakage Current        |                                           |            | 50         | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>                                                                                                                                               |
| V <sub>ID</sub>                    | Input Leakage Test                 | 4.75                                      |            |            | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded                                                                                                                              |
| I <sub>OD</sub>                    | Output Leakage Circuit Control     |                                           |            | 3.75       | μA    | 0.0             | V <sub>IOD</sub> = 150 mV<br>All Other Pins Grounded                                                                                                                             |
| I <sub>ZZ</sub>                    | Bus Drainage Test                  |                                           |            | 500        | μA    | 0.0             | V <sub>OUT</sub> = 5.25V                                                                                                                                                         |
| I <sub>IL</sub>                    | Input LOW Current                  |                                           |            | –0.2       | mA    | Max             | V <sub>IN</sub> = 0.5V (Non-I/O Pins)                                                                                                                                            |
| I <sub>IH</sub> & I <sub>OZH</sub> | Output Leakage Current             |                                           |            | 70         | μA    | Max             | V <sub>OUT</sub> = 2.7V (I/O <sub>n</sub> )                                                                                                                                      |
| I <sub>IL</sub> & I <sub>OZL</sub> | Output Leakage Current             |                                           |            | –200       | μA    | Max             | V <sub>OUT</sub> = 0.5V (I/O <sub>n</sub> )                                                                                                                                      |
| I <sub>OS</sub>                    | Output Short-Circuit Current       | –60                                       |            | –150       | mA    | Max             | V <sub>OUT</sub> = 0V                                                                                                                                                            |
| I <sub>CCH</sub>                   | Power Supply Current               |                                           | 70         | 110        | mA    | Max             | V <sub>O</sub> = HIGH                                                                                                                                                            |
| I <sub>CCL</sub>                   | Power Supply Current               |                                           | 85         | 120        | mA    | Max             | V <sub>O</sub> = LOW                                                                                                                                                             |
| I <sub>CCZ</sub>                   | Power Supply Current               |                                           | 85         | 125        | mA    | Max             | V <sub>O</sub> = HIGH Z                                                                                                                                                          |

| AC Electrical Characteristics |                                                                              |                                                                             |      |      |                                                                                    |      |       |
|-------------------------------|------------------------------------------------------------------------------|-----------------------------------------------------------------------------|------|------|------------------------------------------------------------------------------------|------|-------|
| Symbol                        | Parameter                                                                    | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |      |      | T <sub>A</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |      | Units |
|                               |                                                                              | Min                                                                         | Typ  | Max  | Min                                                                                | Max  |       |
| t <sub>MAX</sub>              | Maximum Clock Frequency                                                      | 70                                                                          | 85   |      | 80                                                                                 |      |       |
| t <sub>PLH</sub>              | Propagation Delay                                                            | 3.0                                                                         | 5.0  | 7.5  | 3.0                                                                                | 8.0  | ns    |
| t <sub>PHL</sub>              | CP to I/O <sub>n</sub>                                                       | 5.0                                                                         | 8.0  | 11.5 | 5.0                                                                                | 11.5 |       |
| t <sub>PLH</sub>              | Propagation Delay                                                            | 5.0                                                                         | 7.5  | 11.5 | 5.0                                                                                | 12.0 | ns    |
| t <sub>PHL</sub>              | CP to $\overline{\text{TC}}$                                                 | 5.0                                                                         | 7.0  | 11.5 | 5.0                                                                                | 12.0 |       |
| t <sub>PLH</sub>              | Propagation Delay                                                            | 4.5                                                                         | 7.0  | 9.0  | 4.5                                                                                | 10.0 | ns    |
| t <sub>PHL</sub>              | U/ $\overline{\text{D}}$ to $\overline{\text{TC}}$                           | 4.5                                                                         | 8.0  | 9.5  | 4.5                                                                                | 10.0 |       |
| t <sub>PLH</sub>              | Propagation Delay                                                            | 2.5                                                                         | 3.8  | 6.0  | 2.5                                                                                | 6.5  | ns    |
| t <sub>PHL</sub>              | $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to $\overline{\text{TC}}$ | 3.5                                                                         | 6.0  | 8.0  | 3.5                                                                                | 8.5  |       |
| t <sub>PHL</sub>              | Propagation Delay                                                            | 5.0                                                                         | 7.5  | 10.0 | 5.0                                                                                | 10.0 | ns    |
|                               | MR to I/O <sub>n</sub>                                                       |                                                                             |      |      |                                                                                    |      |       |
| t <sub>PHL</sub>              | Propagation Delay                                                            | 6.5                                                                         | 10.0 | 13.0 | 6.5                                                                                | 13.5 | ns    |
|                               | MR to TC                                                                     |                                                                             |      |      |                                                                                    |      |       |
| t <sub>PZH</sub>              | Output Enable Time                                                           | 3.0                                                                         | 5.0  | 8.5  | 3.0                                                                                | 9.0  | ns    |
| t <sub>PZL</sub>              | $\overline{\text{CS}}$ or $\overline{\text{PE}}$ to I/O                      | 5.5                                                                         | 8.0  | 10.5 | 5.5                                                                                | 11.5 |       |
| t <sub>PHZ</sub>              | Output Disable Time                                                          | 2.0                                                                         | 5.0  | 8.5  | 2.0                                                                                | 9.0  | ns    |
| t <sub>PLZ</sub>              | $\overline{\text{CS}}$ or $\overline{\text{PE}}$ to I/O                      | 2.0                                                                         | 4.5  | 8.0  | 2.0                                                                                | 8.5  |       |
| t <sub>PZH</sub>              | Output Enable Time                                                           | 3.0                                                                         | 5.0  | 8.0  | 3.0                                                                                | 8.5  | ns    |
| t <sub>PZL</sub>              | $\overline{\text{OE}}$ to I/O <sub>n</sub>                                   | 5.0                                                                         | 8.0  | 11.0 | 5.0                                                                                | 12.0 |       |
| t <sub>PHZ</sub>              | Output Disable Time                                                          | 2.0                                                                         | 4.0  | 6.5  | 2.0                                                                                | 6.5  | ns    |
| t <sub>PLZ</sub>              | $\overline{\text{OE}}$ to I/O <sub>n</sub>                                   | 2.0                                                                         | 4.0  | 6.0  | 2.0                                                                                | 6.5  |       |

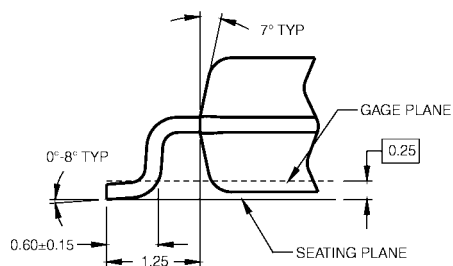
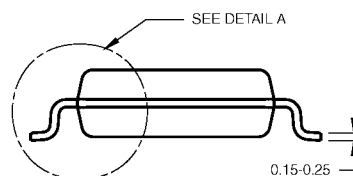
| AC Operating Requirements |                                                                                 |                                                   |     |     |                                                          |     |       |
|---------------------------|---------------------------------------------------------------------------------|---------------------------------------------------|-----|-----|----------------------------------------------------------|-----|-------|
| Symbol                    | Parameter                                                                       | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V |     |     | T <sub>A</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V |     | Units |
|                           |                                                                                 | Min                                               | Typ | Max | Min                                                      | Max |       |
| t <sub>S</sub> (H)        | Setup Time                                                                      | 4.0                                               |     |     | 4.0                                                      |     | ns    |
| t <sub>S</sub> (L)        | I/O <sub>n</sub> to CP                                                          | 4.0                                               |     |     | 4.0                                                      |     |       |
| t <sub>H</sub> (H)        | Hold Time                                                                       | 0.0                                               |     |     | 0.0                                                      |     | ns    |
| t <sub>H</sub> (L)        | I/O <sub>n</sub> to CP                                                          | 0.0                                               |     |     | 0.0                                                      |     |       |
| t <sub>S</sub> (H)        | Setup Time                                                                      | 9.5                                               |     |     | 9.5                                                      |     | ns    |
| t <sub>S</sub> (L)        | $\overline{\text{PE}}$ , $\overline{\text{CS}}$ or $\overline{\text{SR}}$ to CP | 9.5                                               |     |     | 9.5                                                      |     |       |
| t <sub>H</sub> (H)        | Hold Time                                                                       | 0.0                                               |     |     | 0.0                                                      |     | ns    |
| t <sub>H</sub> (L)        | $\overline{\text{PE}}$ , $\overline{\text{CS}}$ or $\overline{\text{SR}}$ to CP | 0.0                                               |     |     | 0.0                                                      |     |       |
| t <sub>S</sub> (H)        | Setup Time                                                                      | 6.5                                               |     |     | 6.5                                                      |     | ns    |
| t <sub>S</sub> (L)        | $\overline{\text{CET}}$ or $\overline{\text{CEP}}$ to CP                        | 9.5                                               |     |     | 9.5                                                      |     |       |
| t <sub>H</sub> (H)        | Hold Time                                                                       | 0.0                                               |     |     | 0.0                                                      |     | ns    |
| t <sub>H</sub> (L)        | $\overline{\text{CET}}$ or $\overline{\text{CEP}}$ to CP                        | 0.0                                               |     |     | 0.0                                                      |     |       |
| t <sub>S</sub> (H)        | Setup Time                                                                      | 9.0                                               |     |     | 9.5                                                      |     | ns    |
| t <sub>S</sub> (L)        | U/ $\overline{\text{D}}$ to CP                                                  | 9.0                                               |     |     | 9.5                                                      |     |       |
| t <sub>H</sub> (H)        | Hold Time                                                                       | 0.0                                               |     |     | 0.0                                                      |     | ns    |
| t <sub>H</sub> (L)        | U/ $\overline{\text{D}}$ to CP                                                  | 0.0                                               |     |     | 0.0                                                      |     |       |
| t <sub>W</sub> (H)        | Clock Pulse Width                                                               | 4.5                                               |     |     | 4.5                                                      |     | ns    |
| t <sub>W</sub> (L)        | HIGH or LOW                                                                     | 4.5                                               |     |     | 4.5                                                      |     |       |
| t <sub>W</sub> (L)        | MR Pulse Width                                                                  | 3.0                                               |     |     | 3.0                                                      |     | ns    |
| t <sub>REC</sub>          | Recovery Time                                                                   | 4.0                                               |     |     | 4.0                                                      |     | ns    |
|                           | $\overline{\text{MR}}$ to CP                                                    |                                                   |     |     |                                                          |     |       |



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

**LAND PATTERN RECOMMENDATION**


DIMENSIONS ARE IN MILLIMETERS

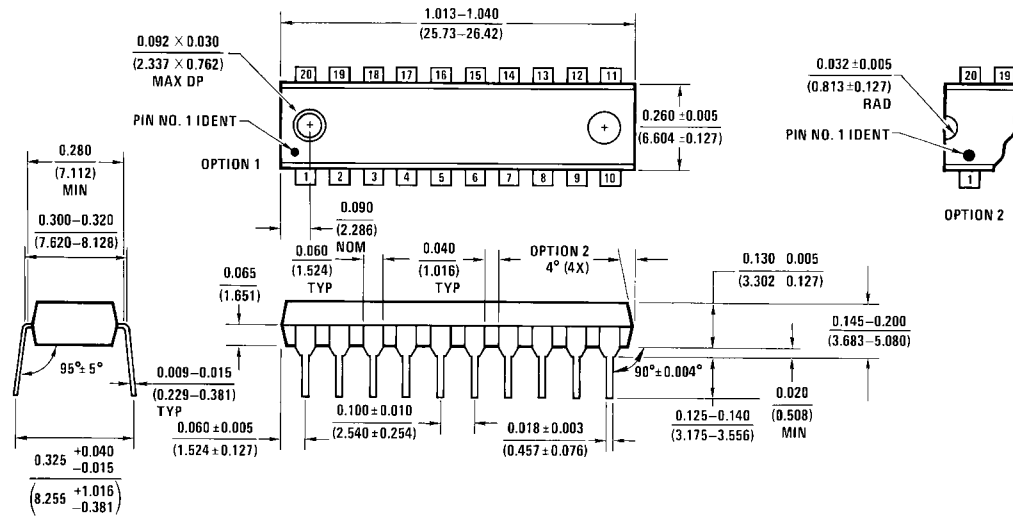

**DETAIL A**
**NOTES:**

- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**  
**Package Number M20D**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N20A

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