SBVS022A – SEPTEMBER 2000 – REVISED NOVEMBER 2003

10V Precision Voltage Reference

FEATURES

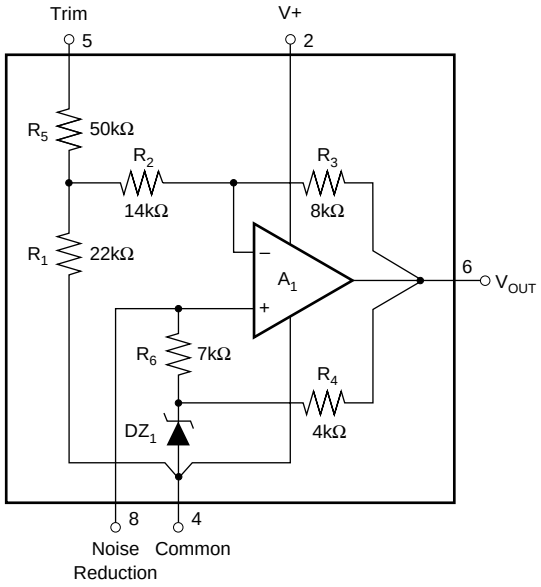
- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μV_{PP} typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: PLASTIC DIP, SO-8

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max C-grade over the industrial temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.



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ABSOLUTE MAXIMUM RATINGS[1]

Input Voltage	+40V
Operating Temperature	
P, U	–25°C to +85°C
Storage Temperature Range	
P, U	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(SO, 3s)	+260°C
Short-Circuit Protection to Common or V+	Continuous

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

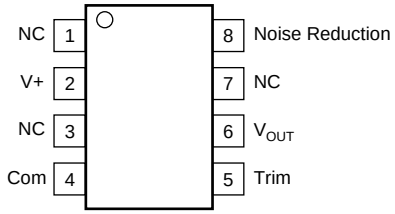
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAX INITIAL ERROR (mV)	MAX DRIFT (PPM/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
REF102AU	±10	±10	SO-8	D	–25°C to +85°C	REF102AU	REF102AU	Tube, 100
"	±10	±10	SO-8	D	"	REF102AU/2K5	REF102AU/2K5	Tape and Reel, 2500
REF102AP	±10	±10	DIP-8	P	"	REF102AP	REF102AP	Tube, 50
REF102BU	±5	±5	SO-8	D	"	REF102BU	REF102BU	Tube, 100
"	±5	±5	SO-8	D	"	REF102BU/2K5	REF102BU/2K5	Tape and Reel, 2500
REF102BP	±5	±5	DIP-8	P	"	REF102BP	REF102BP	Tube, 50
REF102CU	±2.5	±2.5	SO-8	D	"	REF102CU	REF102CU	Tube, 100
"	±2.5	±2.5	SO-8	D	"	REF102CU/2K5	REF102CU/2K5	Tape and Reel, 2500
REF102CP	±2.5	±2.5	DIP-8	P	"	REF102CP	REF102CP	Tube, 50

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

PIN CONFIGURATIONS

Top View **DIP, SO**



NC = Not Connected

ELECTRICAL CHARACTERISTICS

At T_A = +25°C and V_S = +15V power supply, unless otherwise noted.

PARAMETER	CONDITIONS	REF102A			REF102B			REF102C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE											
Initial	T_A = 25°C	9.99		10.01	9.995		10.005	9.9975		10.0025	V
vs Temperature (1)				10			5			2.5	ppm/°C
vs Supply											
(Line Regulation)	V_S = 11.4V to 36V			2			1			1	ppm/V
vs Output Current											
(Load Regulation)	I_L = 0mA to +10mA			20			10			10	ppm/mA
	I_L = 0mA to –5mA			40			20			20	ppm/mA
vs Time	T_A = +25°C										
M Package			5			*			*		ppm/1000hr
P, U Packages (2)			20			*					ppm/1000hr
Trim Range (3)		±3			*			*			%
Capacitive Load, max			1000			*			*		pF
NOISE	0.1Hz to 10Hz		5			*			*		μV_{PP}
OUTPUT CURRENT		+10, –5			*			*			mA
INPUT VOLTAGE RANGE		+11.4		+36	*		*	*		*	V
QUIESCENT CURRENT	I_{OUT} = 0			+1.4			*			*	mA
WARM-UP TIME (4)	To 0.1%		15			*			*		µs
TEMPERATURE RANGE											
Specification											
REF102A, B, C		–25		+85	*		*	*		*	°C

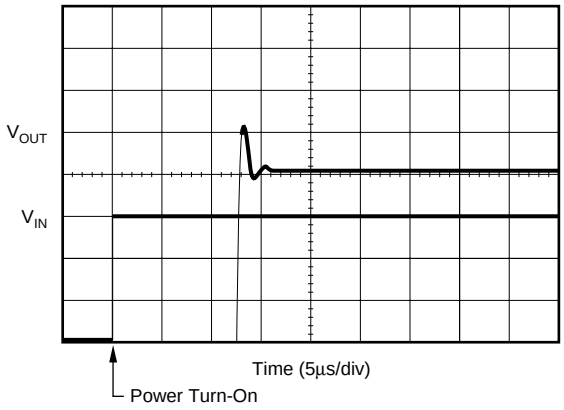
* Specifications same as REF102A.

NOTES: (1) The “box” method is used to specify output voltage drift vs temperature. See the Discussion of Performance section.
(2) Typically 5ppm/1000hrs after 168hr powered stabilization.
(3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details.
(4) With noise reduction pin floating. See Typical Characteristics for details.

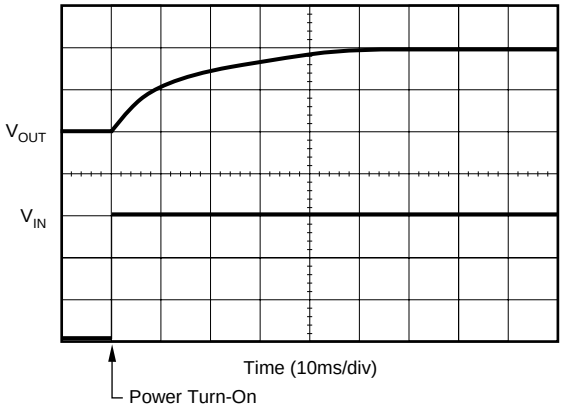
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +15V, unless otherwise noted.

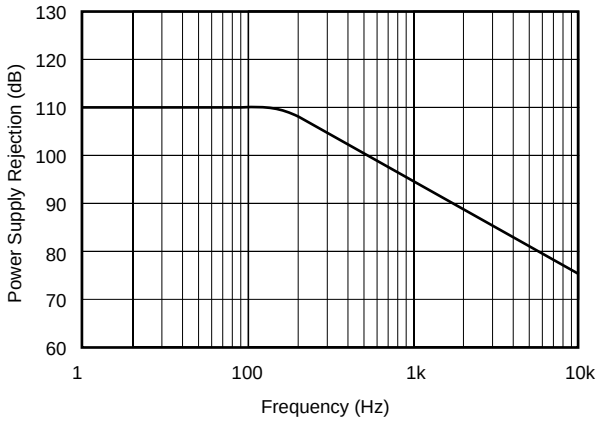
POWER TURN-ON RESPONSE



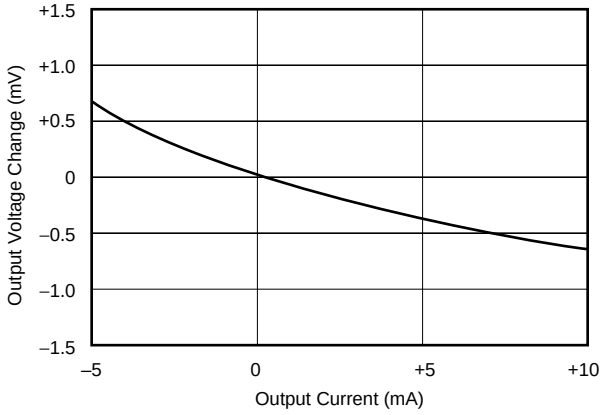
POWER TURN-ON RESPONSE with 1µF C_N



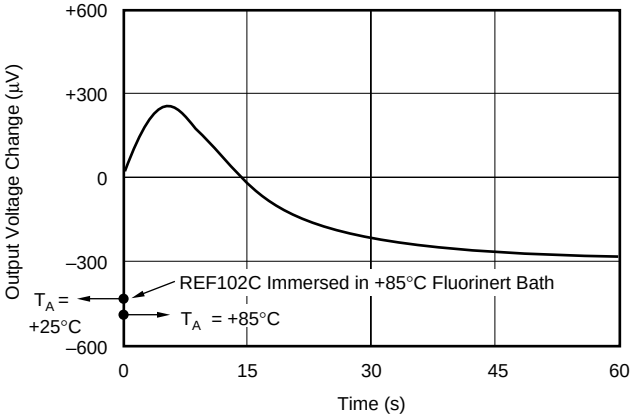
POWER SUPPLY REJECTION vs FREQUENCY



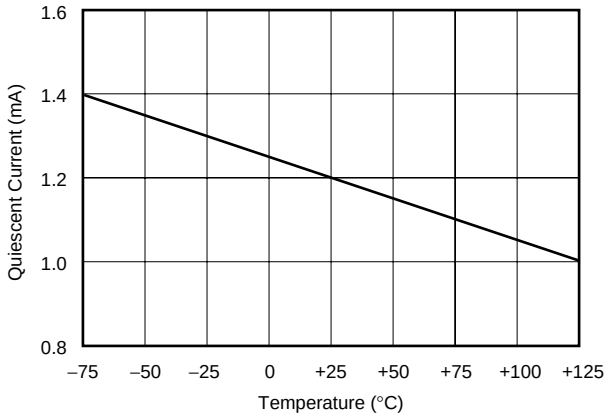
LOAD REGULATION



RESPONSE TO THERMAL SHOCK



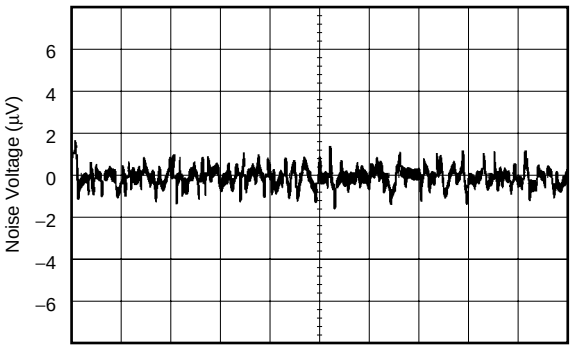
QUIESCENT CURRENT vs TEMPERATURE



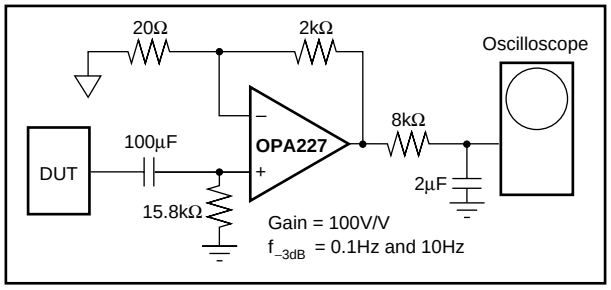
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +15V, unless otherwise noted.

TYPICAL REF102 REFERENCE NOISE



Low Frequency Noise (1s/div)
(See Noise Test Circuit)



Noise Test Circuit.

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1, op amp A_1, and resistor network $R_1 – R_6$.

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1. R_1, R_2, and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4. R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the temperature coefficient (TCR) of of R_5 closely matches the TCR of R_1, R_2 and R_3 , the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the “butterfly method” and the “box method.” The REF102 is specified by the more commonly-used “box method.” The “box” is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not known, either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CU as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of –25°C to +85°C. The “box” height, V_1 to V_2, is 2.75mV.

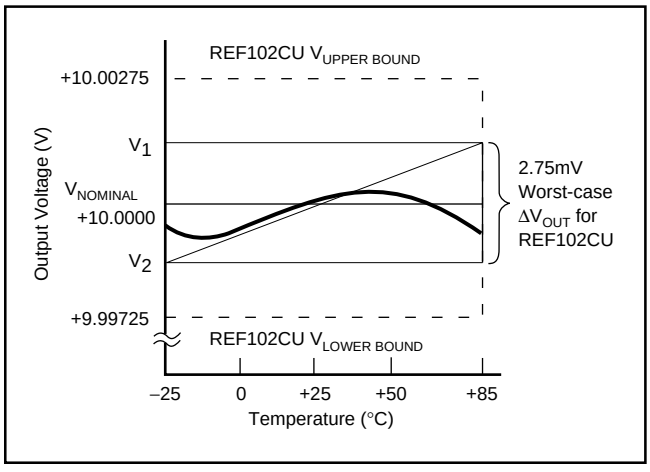
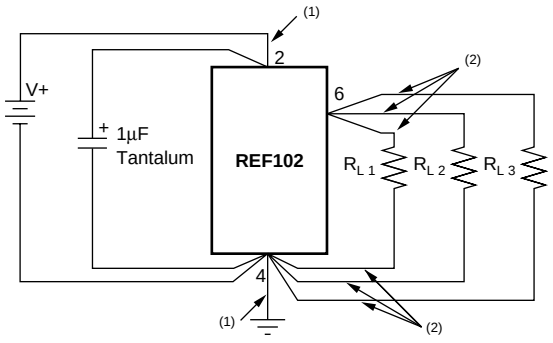


FIGURE 1. REF102CU Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated, being sure to minimize interconnection resistances.



NOTES: (1) Lead resistances here of up to a few ohms have negligible effect on performance. (2) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

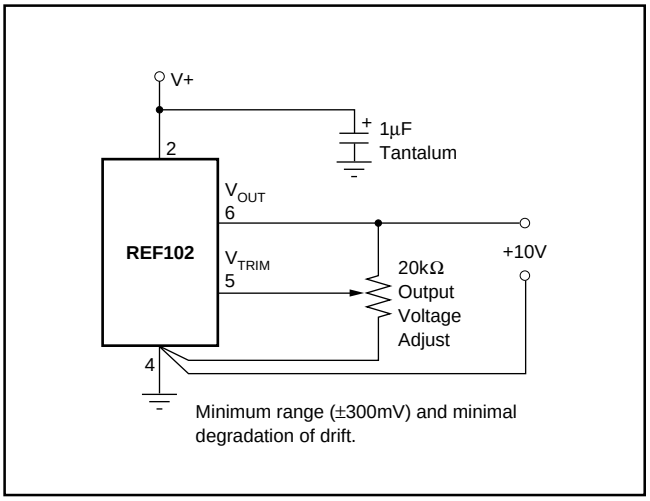


FIGURE 3. REF102 Optional Output Voltage Adjust.

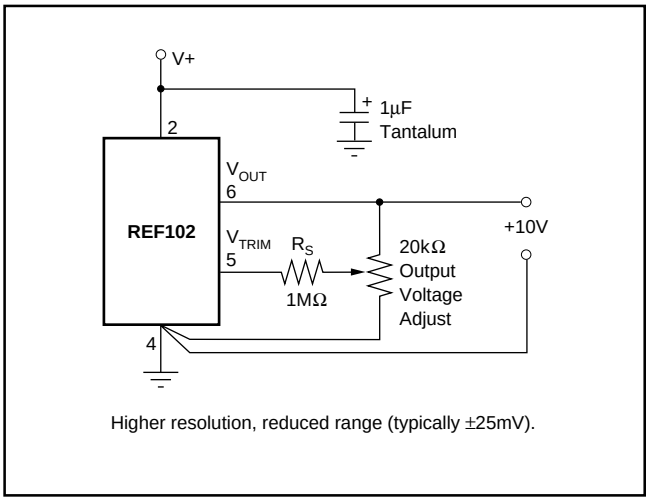


FIGURE 4. REF102 Optional Output Voltage, Fine Adjust.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low-pass filter with R_6 (refer to the figure on page 1) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1µF noise reduction capacitor on the high-frequency noise of the REF102. R_6 is typically 7kΩ so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about $800\mu V_{PP}$ to under $200\mu V_{PP}$. If further noise reduction is required, use the circuit in Figure 14.

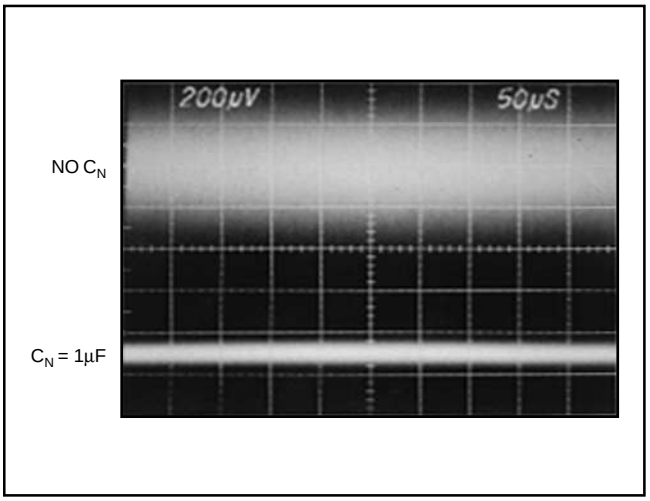


FIGURE 5. Effect of 1µF Noise Reduction Capacitor on Broadband Noise (f_{-3dB} = 1MHz)

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

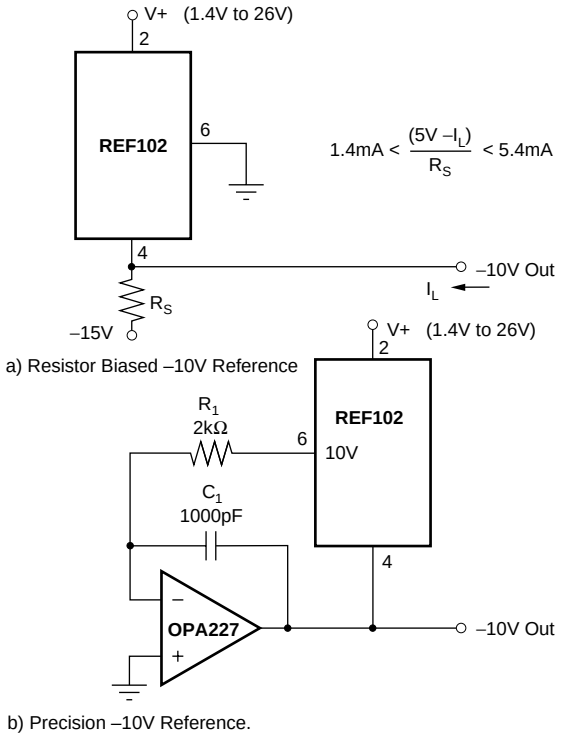


FIGURE 6. –10V Reference Using a) Resistor or b) OPA227.

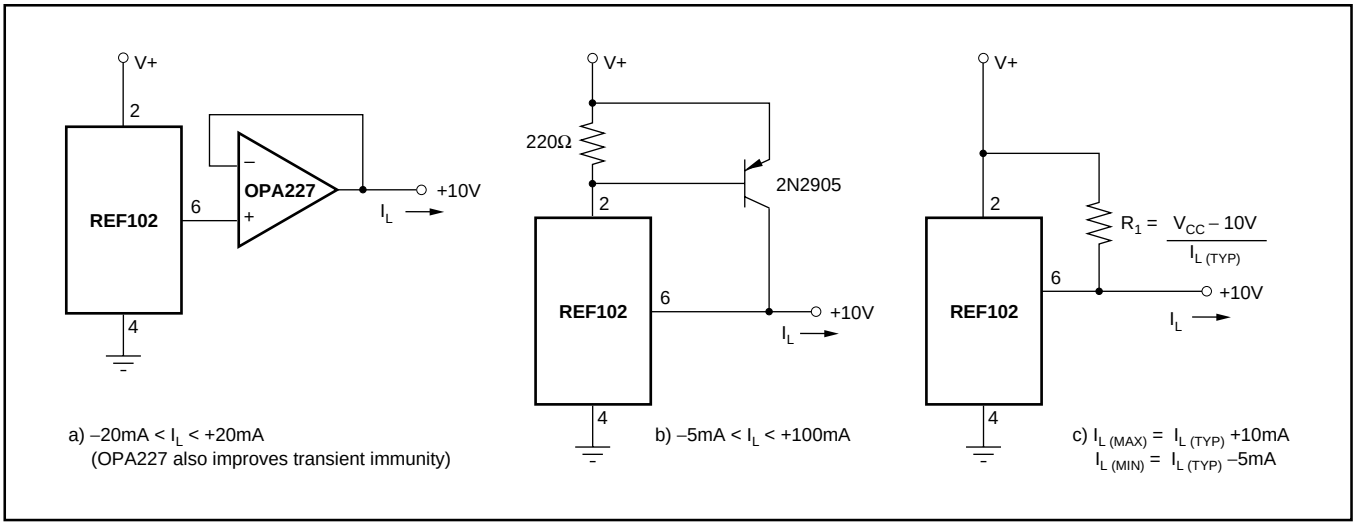


FIGURE 7. +10V Reference With Output Current Boosted to: a) ±20mA, b) +100mA, and c) $I_{L\ (TYP)}$ +10mA, –5A.

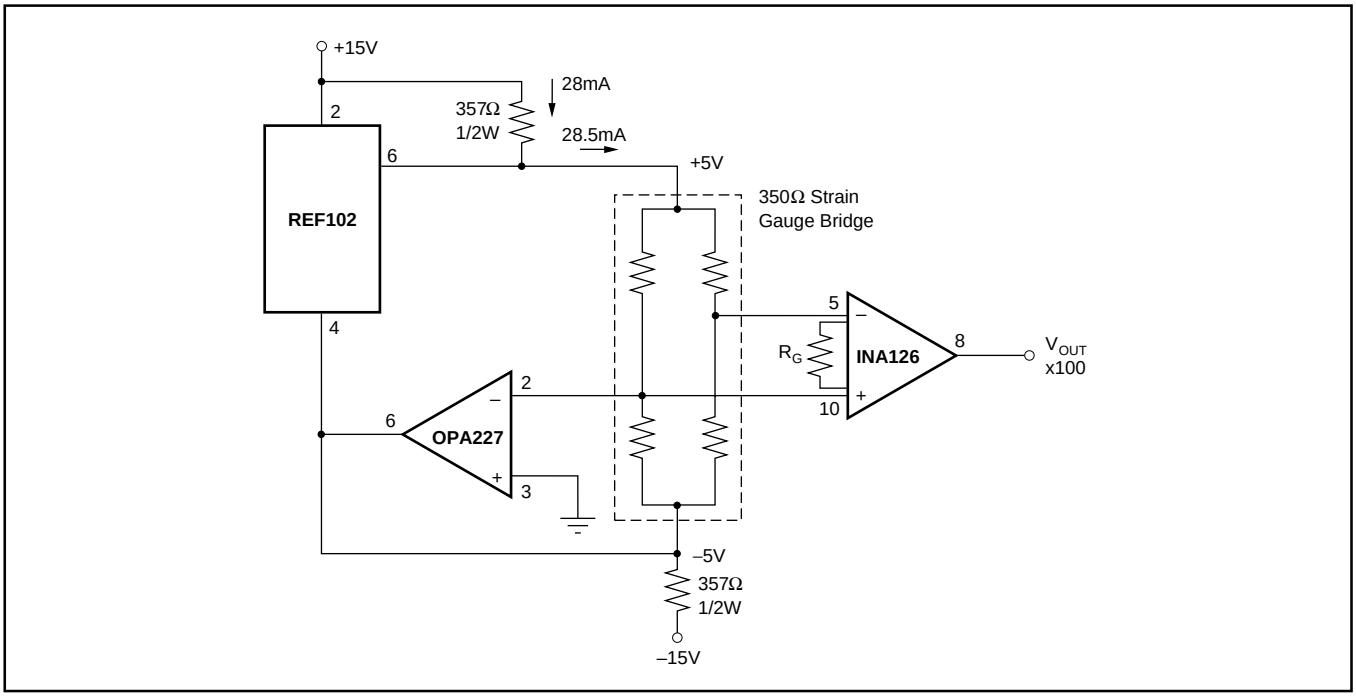


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

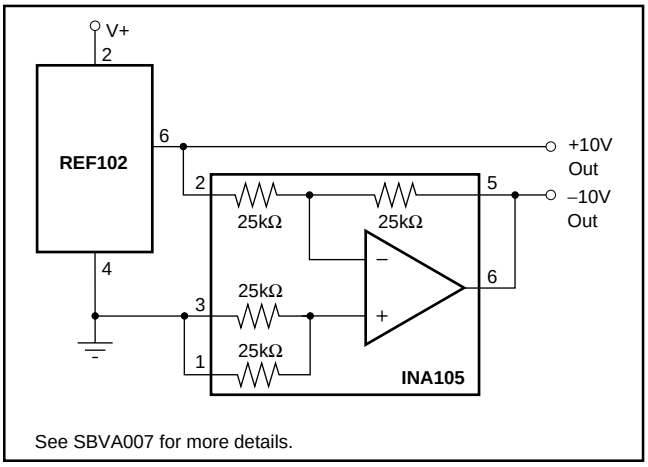


FIGURE 9. ±10V Reference.

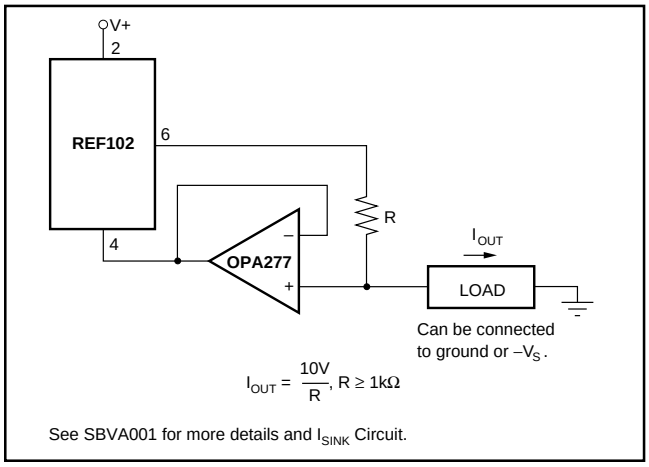
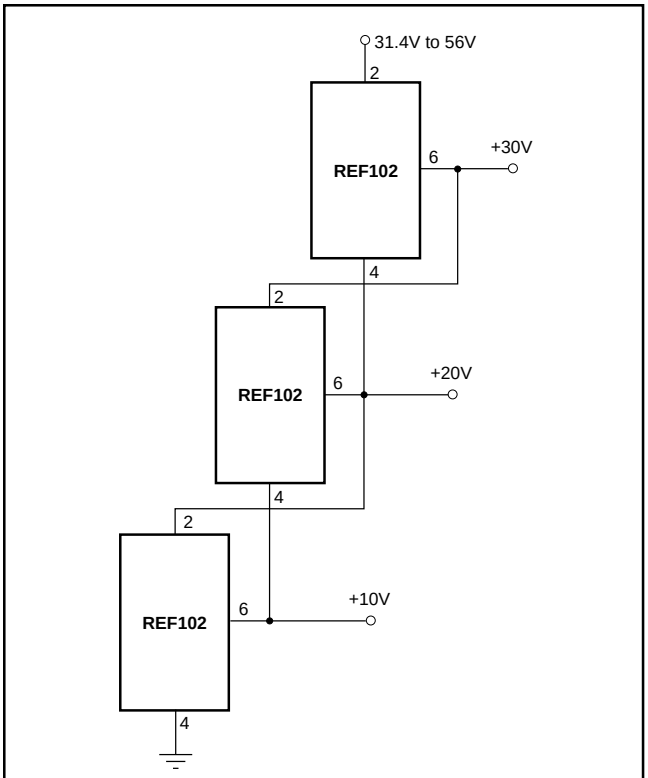


FIGURE 10. Positive Precision Current Source.



NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26, where *n* is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, –5mA. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

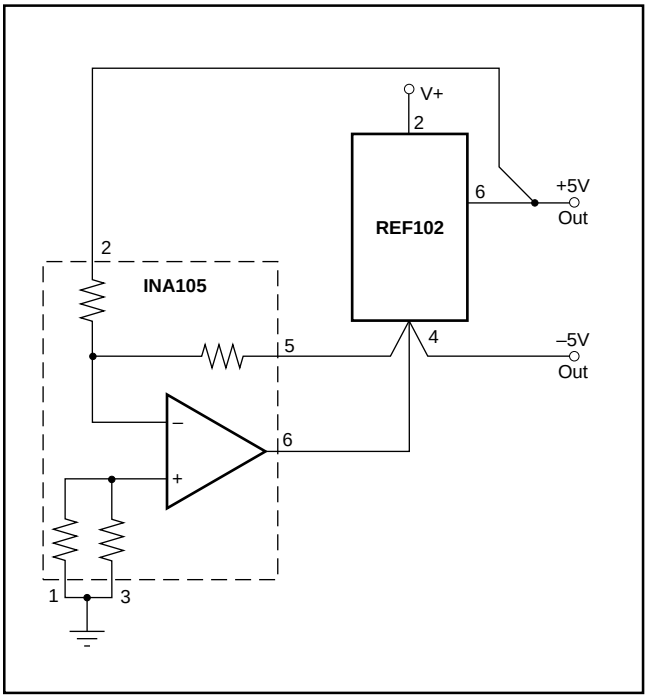


FIGURE 12. ±5V Reference.

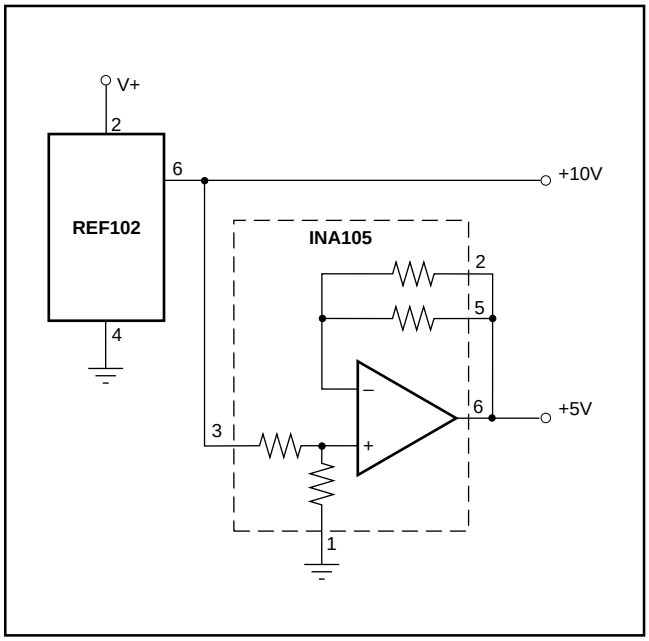


FIGURE 13. +5V and +10V Reference.

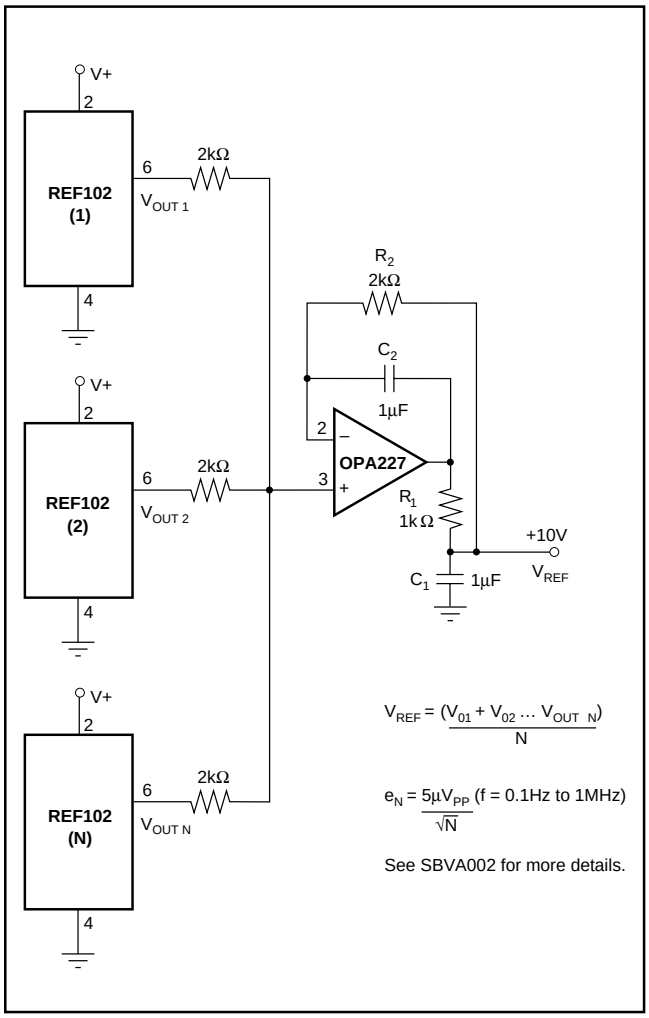


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
REF102AM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
REF102AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102APG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102AU	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102AU/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102AUG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102BM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
REF102BP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102BPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102BU	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102BUG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102CM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
REF102CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102CPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
REF102CU	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102CUG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF102RM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
REF102SM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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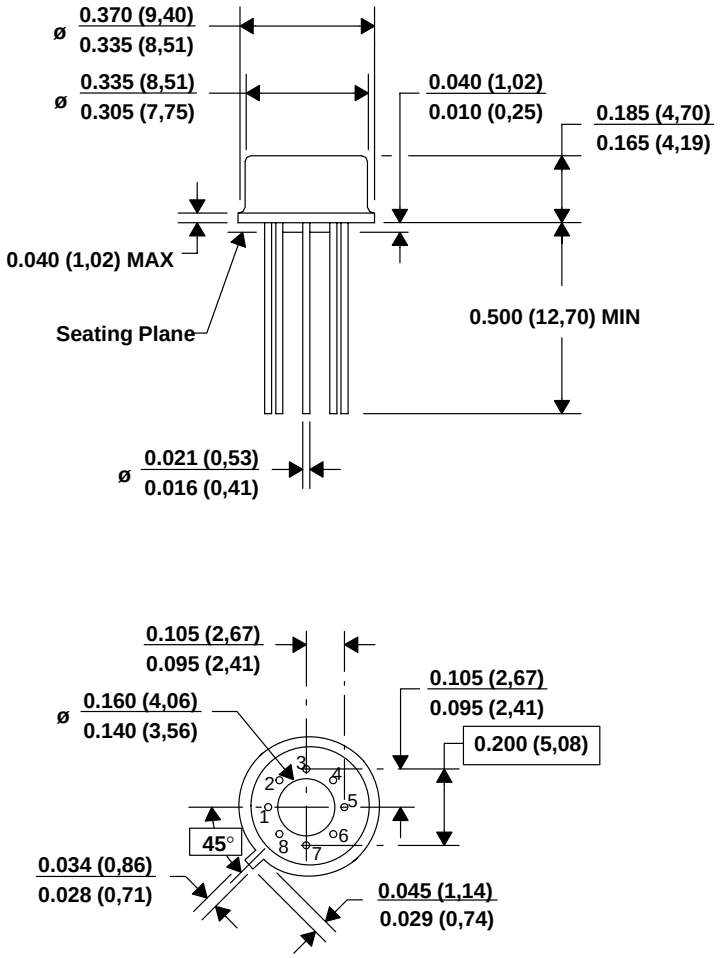
LMC (O–MBCY–W8) **METAL CYLINDRICAL**



4202483/A 03/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO-002/TO-99.

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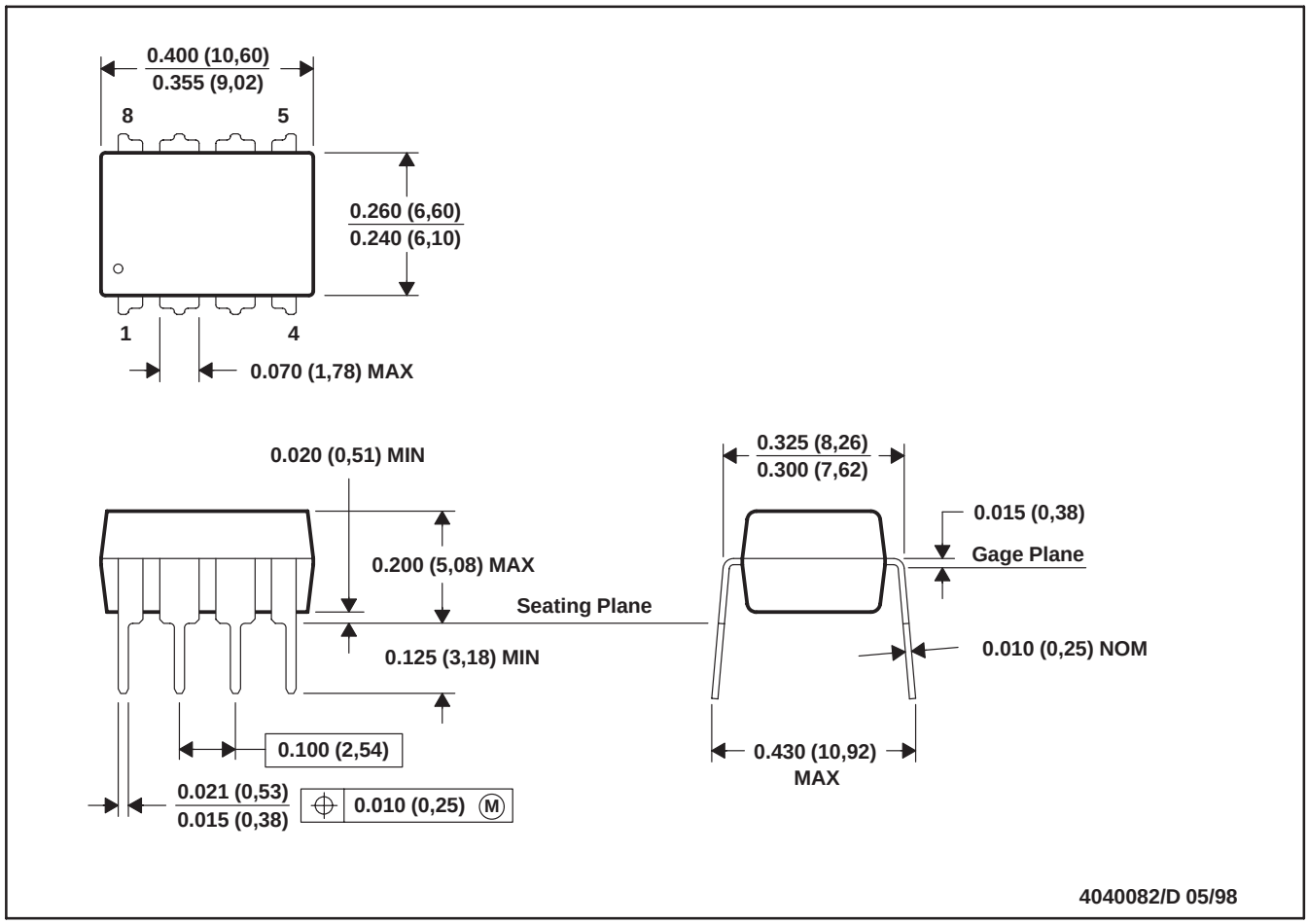
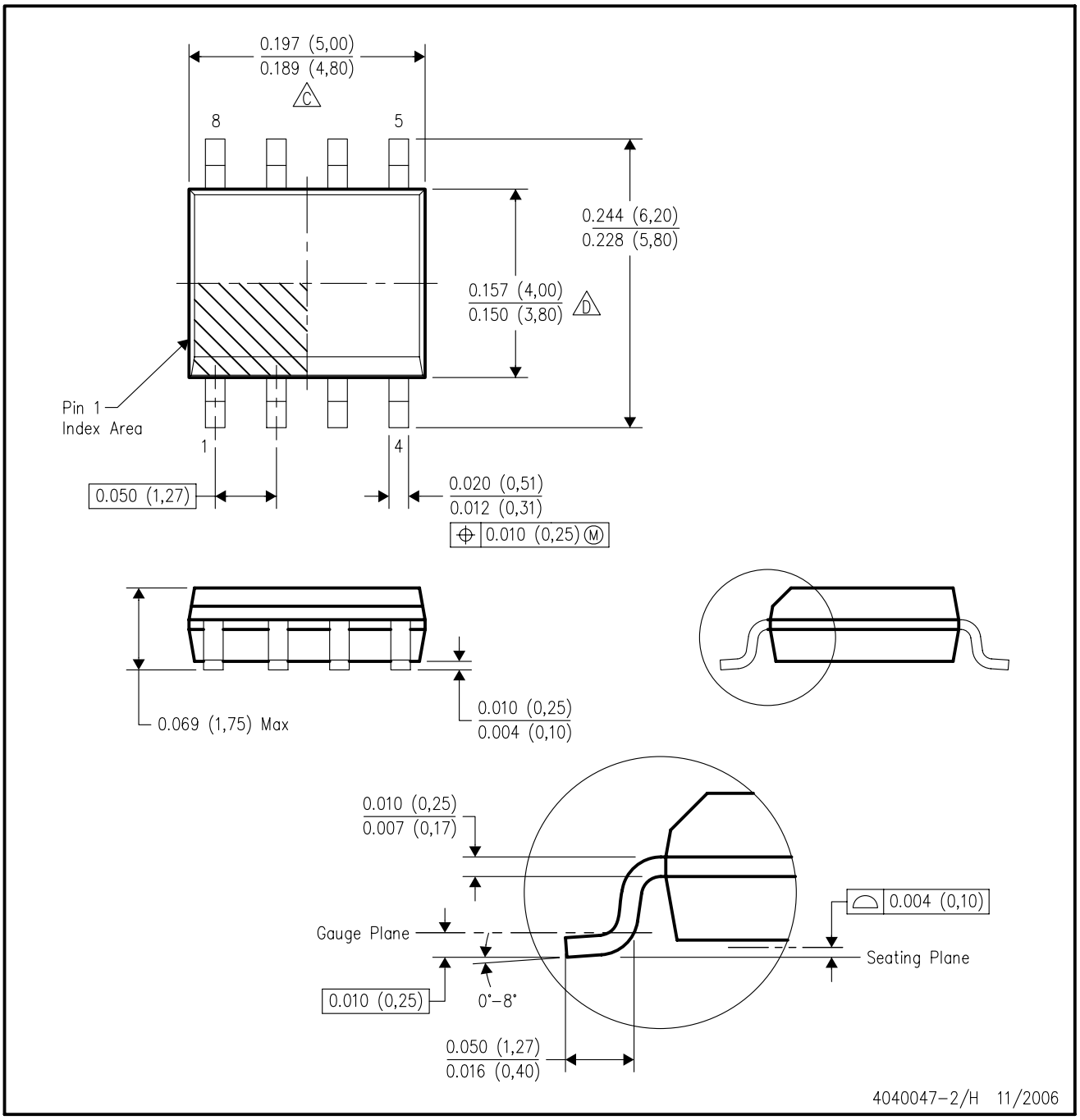
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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