S-19100xxxH Series

FOR AUTOMOTIVE 105°C OPERATION VOLTAGE DETECTOR BUILT-IN DELAY CIRCUIT (EXTERNAL DELAY TIME SETTING)

www.sii-ic.com

The S-19100xxxH Series, developed by using CMOS technology, is a voltage detector IC for automotive 105°C operation. The detection voltage is fixed internally with an accuracy of ±2.5% ($-V_{DET}$ = 2.4 V). It operates with current consumption of 270 nA typ.
The release signal can be delayed by setting a capacitor externally, and the delay time accuracy at Ta = +25°C is ±15%. The operation temperature range is Ta = −40°C to +105°C. Two output forms Nch open-drain and CMOS output are available.
Compared with conventional CMOS voltage detectors, the S-19100xxxH Series has super-low current consumption and small packages.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to SII Semiconductor Corporation is indispensable.

■ Features

- Detection voltage: 1.2 V to 4.6 V (0.1 V step)
- Detection voltage accuracy: ±2.5% (2.4 V ≤ $-V_{DET}$ ≤ 4.6 V, Ta = −40°C to +105°C)
  ±(2.0% + 12 mV) (1.2 V ≤ $-V_{DET}$ < 2.4 V, Ta = −40°C to +105°C)
- Current consumption: 270 nA typ. (1.2 V ≤ $-V_{DET}$ < 2.3 V)
- Operation voltage range: 0.6 V to 10.0 V (CMOS output product)
- Hysteresis width*1: 5% ±2% (Ta = −40°C to +105°C)
- Delay time accuracy: ±15% (C_D = 4.7 nF, Ta = +25°C)
- Output form: Nch open-drain output (active "L")
  CMOS output (active "L")
- Operation temperature range: Ta = −40°C to +105°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*2: SOT-23-5 package product, SC-82AB package product

***1.** The product without hysteresis width is also available.
***2.** SNT-4A package product is in the process of AEC-Q100.
Contact our sales office for details.

■ Applications

- For automotive use (meter, car body, headlight, ITS, accessory, car navigation system, car audio system, etc.)
  : SOT-23-5 package product, SC-82AB package product

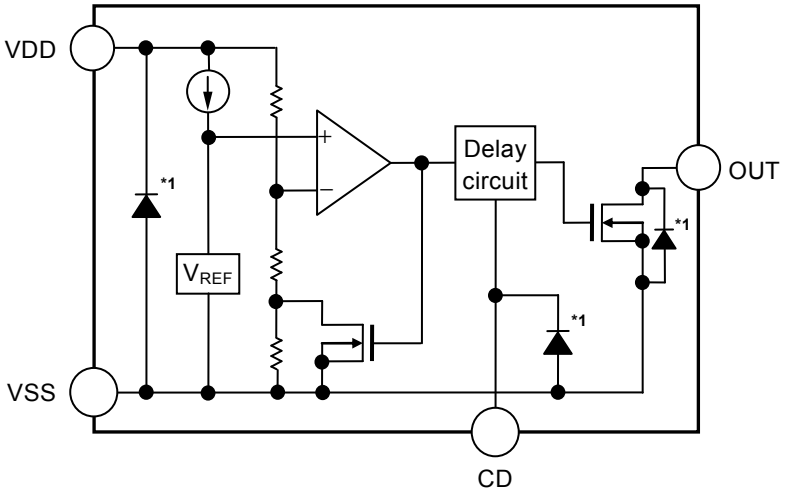
- For automotive use (accessory, car navigation system, car audio system, etc.)
  : SNT-4A package product

■ Packages

- SOT-23-5
- SC-82AB
- SNT-4A

■ Block Diagrams

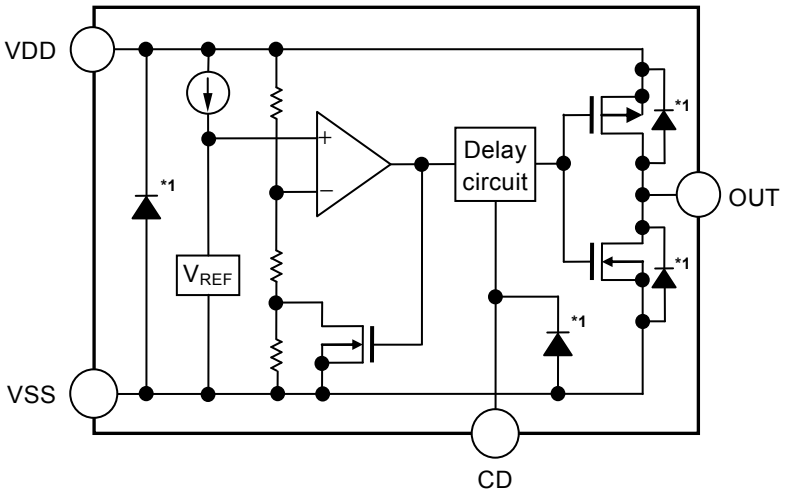
1. Nch open-drain output product



***1.** Parasitic diode

Figure 1

2. CMOS output product



***1.** Parasitic diode

Figure 2

■ AEC-Q100 Qualified*1

SOT-23-5 package product and SC-82AB package product of this IC support AEC-Q100 for the operation temperature grade 2.
Contact our sales office for details of AEC-Q100 reliability specification.

***1.** SNT-4A package product is in the process of AEC-Q100.
Contact our sales office for details.

■ Product Name Structure

Users can select the output form, the detection voltage value and the package type for the S-19100xxxH Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Packages**" regarding the package drawings and "**3. Product name list**" regarding details of product name.

1. Product name

S-19100 x xx H - xxxx U

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - M5T2: SOT-23-5, Tape
  - N4T2: SC-82AB, Tape
  - I4T1: SNT-4A, Tape
- Operation temperature
  - H: Ta = −40°C to +105°C
- Detection voltage value
  - 12 to 46
  - (e.g., when the detection voltage is 1.2 V, it is expressed as 12.)
- Output form
  - N: Nch open-drain output (active "L")
  - C: CMOS output (active "L")

***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–
SC-82AB	NP004-A-P-SD	NP004-A-C-SD NP004-A-C-S1	NP004-A-R-SD	–
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

3. Product name list

3. 1 Nch open-drain output product

Table 2

Detection Voltage	SOT-23-5	SC-82AB	SNT-4A
1.2 V ± (2.0% + 12 mV)	S-19100N12H-M5T2U	S-19100N12H-N4T2U	S-19100N12H-I4T1U
1.3 V ± (2.0% + 12 mV)	S-19100N13H-M5T2U	S-19100N13H-N4T2U	S-19100N13H-I4T1U
1.4 V ± (2.0% + 12 mV)	S-19100N14H-M5T2U	S-19100N14H-N4T2U	S-19100N14H-I4T1U
1.5 V ± (2.0% + 12 mV)	S-19100N15H-M5T2U	S-19100N15H-N4T2U	S-19100N15H-I4T1U
1.6 V ± (2.0% + 12 mV)	S-19100N16H-M5T2U	S-19100N16H-N4T2U	S-19100N16H-I4T1U
1.7 V ± (2.0% + 12 mV)	S-19100N17H-M5T2U	S-19100N17H-N4T2U	S-19100N17H-I4T1U
1.8 V ± (2.0% + 12 mV)	S-19100N18H-M5T2U	S-19100N18H-N4T2U	S-19100N18H-I4T1U
1.9 V ± (2.0% + 12 mV)	S-19100N19H-M5T2U	S-19100N19H-N4T2U	S-19100N19H-I4T1U
2.0 V ± (2.0% + 12 mV)	S-19100N20H-M5T2U	S-19100N20H-N4T2U	S-19100N20H-I4T1U
2.1 V ± (2.0% + 12 mV)	S-19100N21H-M5T2U	S-19100N21H-N4T2U	S-19100N21H-I4T1U
2.2 V ± (2.0% + 12 mV)	S-19100N22H-M5T2U	S-19100N22H-N4T2U	S-19100N22H-I4T1U
2.3 V ± (2.0% + 12 mV)	S-19100N23H-M5T2U	S-19100N23H-N4T2U	S-19100N23H-I4T1U
2.4 V ± 2.5%	S-19100N24H-M5T2U	S-19100N24H-N4T2U	S-19100N24H-I4T1U
2.5 V ± 2.5%	S-19100N25H-M5T2U	S-19100N25H-N4T2U	S-19100N25H-I4T1U
2.6 V ± 2.5%	S-19100N26H-M5T2U	S-19100N26H-N4T2U	S-19100N26H-I4T1U
2.7 V ± 2.5%	S-19100N27H-M5T2U	S-19100N27H-N4T2U	S-19100N27H-I4T1U
2.8 V ± 2.5%	S-19100N28H-M5T2U	S-19100N28H-N4T2U	S-19100N28H-I4T1U
2.9 V ± 2.5%	S-19100N29H-M5T2U	S-19100N29H-N4T2U	S-19100N29H-I4T1U
3.0 V ± 2.5%	S-19100N30H-M5T2U	S-19100N30H-N4T2U	S-19100N30H-I4T1U
3.1 V ± 2.5%	S-19100N31H-M5T2U	S-19100N31H-N4T2U	S-19100N31H-I4T1U
3.2 V ± 2.5%	S-19100N32H-M5T2U	S-19100N32H-N4T2U	S-19100N32H-I4T1U
3.3 V ± 2.5%	S-19100N33H-M5T2U	S-19100N33H-N4T2U	S-19100N33H-I4T1U
3.4 V ± 2.5%	S-19100N34H-M5T2U	S-19100N34H-N4T2U	S-19100N34H-I4T1U
3.5 V ± 2.5%	S-19100N35H-M5T2U	S-19100N35H-N4T2U	S-19100N35H-I4T1U
3.6 V ± 2.5%	S-19100N36H-M5T2U	S-19100N36H-N4T2U	S-19100N36H-I4T1U
3.7 V ± 2.5%	S-19100N37H-M5T2U	S-19100N37H-N4T2U	S-19100N37H-I4T1U
3.8 V ± 2.5%	S-19100N38H-M5T2U	S-19100N38H-N4T2U	S-19100N38H-I4T1U
3.9 V ± 2.5%	S-19100N39H-M5T2U	S-19100N39H-N4T2U	S-19100N39H-I4T1U
4.0 V ± 2.5%	S-19100N40H-M5T2U	S-19100N40H-N4T2U	S-19100N40H-I4T1U
4.1 V ± 2.5%	S-19100N41H-M5T2U	S-19100N41H-N4T2U	S-19100N41H-I4T1U
4.2 V ± 2.5%	S-19100N42H-M5T2U	S-19100N42H-N4T2U	S-19100N42H-I4T1U
4.3 V ± 2.5%	S-19100N43H-M5T2U	S-19100N43H-N4T2U	S-19100N43H-I4T1U
4.4 V ± 2.5%	S-19100N44H-M5T2U	S-19100N44H-N4T2U	S-19100N44H-I4T1U
4.5 V ± 2.5%	S-19100N45H-M5T2U	S-19100N45H-N4T2U	S-19100N45H-I4T1U
4.6 V ± 2.5%	S-19100N46H-M5T2U	S-19100N46H-N4T2U	S-19100N46H-I4T1U

3. 2 CMOS output product

Table 3

Detection Voltage	SOT-23-5	SC-82AB	SNT-4A
1.2 V ± (2.0% + 12 mV)	S-19100C12H-M5T2U	S-19100C12H-N4T2U	S-19100C12H-I4T1U
1.3 V ± (2.0% + 12 mV)	S-19100C13H-M5T2U	S-19100C13H-N4T2U	S-19100C13H-I4T1U
1.4 V ± (2.0% + 12 mV)	S-19100C14H-M5T2U	S-19100C14H-N4T2U	S-19100C14H-I4T1U
1.5 V ± (2.0% + 12 mV)	S-19100C15H-M5T2U	S-19100C15H-N4T2U	S-19100C15H-I4T1U
1.6 V ± (2.0% + 12 mV)	S-19100C16H-M5T2U	S-19100C16H-N4T2U	S-19100C16H-I4T1U
1.7 V ± (2.0% + 12 mV)	S-19100C17H-M5T2U	S-19100C17H-N4T2U	S-19100C17H-I4T1U
1.8 V ± (2.0% + 12 mV)	S-19100C18H-M5T2U	S-19100C18H-N4T2U	S-19100C18H-I4T1U
1.9 V ± (2.0% + 12 mV)	S-19100C19H-M5T2U	S-19100C19H-N4T2U	S-19100C19H-I4T1U
2.0 V ± (2.0% + 12 mV)	S-19100C20H-M5T2U	S-19100C20H-N4T2U	S-19100C20H-I4T1U
2.1 V ± (2.0% + 12 mV)	S-19100C21H-M5T2U	S-19100C21H-N4T2U	S-19100C21H-I4T1U
2.2 V ± (2.0% + 12 mV)	S-19100C22H-M5T2U	S-19100C22H-N4T2U	S-19100C22H-I4T1U
2.3 V ± (2.0% + 12 mV)	S-19100C23H-M5T2U	S-19100C23H-N4T2U	S-19100C23H-I4T1U
2.4 V ± 2.5%	S-19100C24H-M5T2U	S-19100C24H-N4T2U	S-19100C24H-I4T1U
2.5 V ± 2.5%	S-19100C25H-M5T2U	S-19100C25H-N4T2U	S-19100C25H-I4T1U
2.6 V ± 2.5%	S-19100C26H-M5T2U	S-19100C26H-N4T2U	S-19100C26H-I4T1U
2.7 V ± 2.5%	S-19100C27H-M5T2U	S-19100C27H-N4T2U	S-19100C27H-I4T1U
2.8 V ± 2.5%	S-19100C28H-M5T2U	S-19100C28H-N4T2U	S-19100C28H-I4T1U
2.9 V ± 2.5%	S-19100C29H-M5T2U	S-19100C29H-N4T2U	S-19100C29H-I4T1U
3.0 V ± 2.5%	S-19100C30H-M5T2U	S-19100C30H-N4T2U	S-19100C30H-I4T1U
3.1 V ± 2.5%	S-19100C31H-M5T2U	S-19100C31H-N4T2U	S-19100C31H-I4T1U
3.2 V ± 2.5%	S-19100C32H-M5T2U	S-19100C32H-N4T2U	S-19100C32H-I4T1U
3.3 V ± 2.5%	S-19100C33H-M5T2U	S-19100C33H-N4T2U	S-19100C33H-I4T1U
3.4 V ± 2.5%	S-19100C34H-M5T2U	S-19100C34H-N4T2U	S-19100C34H-I4T1U
3.5 V ± 2.5%	S-19100C35H-M5T2U	S-19100C35H-N4T2U	S-19100C35H-I4T1U
3.6 V ± 2.5%	S-19100C36H-M5T2U	S-19100C36H-N4T2U	S-19100C36H-I4T1U
3.7 V ± 2.5%	S-19100C37H-M5T2U	S-19100C37H-N4T2U	S-19100C37H-I4T1U
3.8 V ± 2.5%	S-19100C38H-M5T2U	S-19100C38H-N4T2U	S-19100C38H-I4T1U
3.9 V ± 2.5%	S-19100C39H-M5T2U	S-19100C39H-N4T2U	S-19100C39H-I4T1U
4.0 V ± 2.5%	S-19100C40H-M5T2U	S-19100C40H-N4T2U	S-19100C40H-I4T1U
4.1 V ± 2.5%	S-19100C41H-M5T2U	S-19100C41H-N4T2U	S-19100C41H-I4T1U
4.2 V ± 2.5%	S-19100C42H-M5T2U	S-19100C42H-N4T2U	S-19100C42H-I4T1U
4.3 V ± 2.5%	S-19100C43H-M5T2U	S-19100C43H-N4T2U	S-19100C43H-I4T1U
4.4 V ± 2.5%	S-19100C44H-M5T2U	S-19100C44H-N4T2U	S-19100C44H-I4T1U
4.5 V ± 2.5%	S-19100C45H-M5T2U	S-19100C45H-N4T2U	S-19100C45H-I4T1U
4.6 V ± 2.5%	S-19100C46H-M5T2U	S-19100C46H-N4T2U	S-19100C46H-I4T1U

■ Pin Configurations

1. SOT-23-5

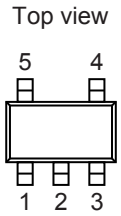


Figure 3

Table 4

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Input voltage pin
3	VSS	GND pin
4	NC*1	No connection
5	CD	Connection pin for delay capacitor

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

2. SC-82AB

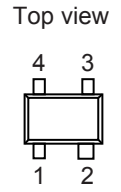


Figure 4

Table 5

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Input voltage pin
3	CD	Connection pin for delay capacitor
4	OUT	Voltage detection output pin

3. SNT-4A

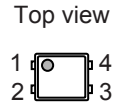


Figure 5

Table 6

Pin No.	Symbol	Description
1	VSS	GND pin
2	OUT	Voltage detection output pin
3	CD	Connection pin for delay capacitor
4	VDD	Input voltage pin

■ Absolute Maximum Ratings

Table 7

(Ta = –40°C to +105°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD} – V_{SS}	12	V
CD pin input voltage		V_{CD}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} – 0.3 to 12.0	V
	CMOS output product		V_{SS} – 0.3 to V_{DD} + 0.3	V
Output current		I_{OUT}	50	mA
Operation ambient temperature		T_{opr}	–40 to +105	°C
Storage temperature		T_{stg}	–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 8

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{ja}	SOT-23-5	Board 1	–	192	–	°C/W
			Board 2	–	160	–	°C/W
		SC-82AB	Board 1	–	236	–	°C/W
			Board 2	–	204	–	°C/W
		SNT-4A	Board 1	–	300	–	°C/W
			Board 2	–	242	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Thermal Characteristics**" for details of power dissipation and test board.

■ Electrical Characteristics

1. Nch open-drain output product

Table 9

(Ta = –40°C to +105°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	1.2 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)} \times 0.98 - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02 + 0.012$	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)} \times 0.975$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	1
Current consumption	I_{SS}	V_{DD} = $+V_{DET}$ + 0.6 V	1.2 V ≤ $-V_{DET}$ < 2.3 V	–	0.27	1.10	µA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	–	0.42	1.20	µA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	–	0.39	1.20	µA	2
Operation voltage	V_{DD}	–		0.8	–	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*2 = 0.5 V	V_{DD} = 0.7 V S-19100N12 to 14	0.14	0.40	–	mA	3
			V_{DD} = 1.2 V S-19100N15 to 46	0.73	1.33	–	mA	3
			V_{DD} = 2.4 V S-19100N27 to 46	1.17	2.39	–	mA	3
Leakage current	I_{LEAK}	Output transistor Nch V_{DD} = 10.0 V, V_{OUT} = 10.0 V		–	–	1.20	µA	3
Delay time	t_D	C_D = 4.7 nF		12.0	26.0	57.0	ms	4

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (The center value of the detection voltage range in **Table 2**.)

***2.** V_{DS}: Drain-to-source voltage of the output transistor

2. CMOS output product

Table 10

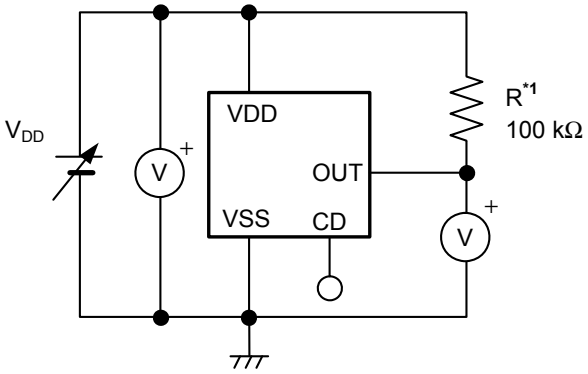
(Ta = –40°C to +105°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	1.2 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)} \times 0.98 - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02 + 0.012$	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)} \times 0.975$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	1
Current consumption	I_{SS}	V_{DD} = $+V_{DET}$ + 0.6 V	1.2 V ≤ $-V_{DET}$ < 2.3 V	–	0.27	1.70	µA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	–	0.42	1.90	µA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	–	0.39	1.90	µA	2
Operation voltage	V_{DD}	–		0.6	–	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*2 = 0.5 V	V_{DD} = 0.7 V S-19100C12 to 14	0.14	0.40	–	mA	3
			V_{DD} = 1.2 V S-19100C15 to 46	0.73	1.33	–	mA	3
			V_{DD} = 2.4 V S-19100C27 to 46	1.17	2.39	–	mA	3
		Output transistor Pch V_{DS}*2 = 0.5 V	V_{DD} = 4.8 V S-19100C12 to 39	1.42	2.60	–	mA	5
			V_{DD} = 6.0 V S-19100C40 to 46	1.58	2.86	–	mA	5
Delay time	t_D	C_D = 4.7 nF		12.0	26.0	57.0	ms	4

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (The center value of the detection voltage range in **Table 3**.)

***2.** V_{DS}: Drain-to-source voltage of the output transistor

■ Test Circuits



***1.** R is unnecessary for CMOS output product.

Figure 6 Test Circuit 1

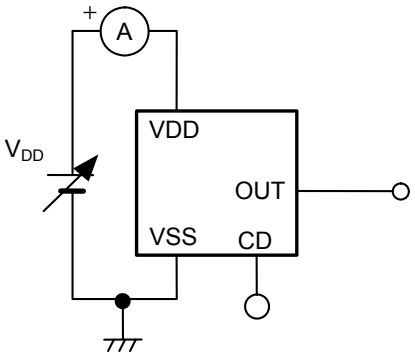


Figure 7 Test Circuit 2

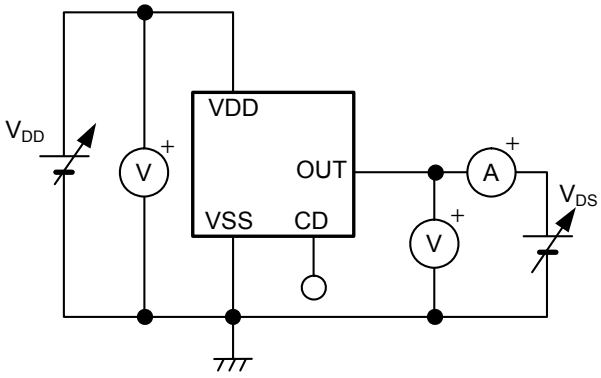
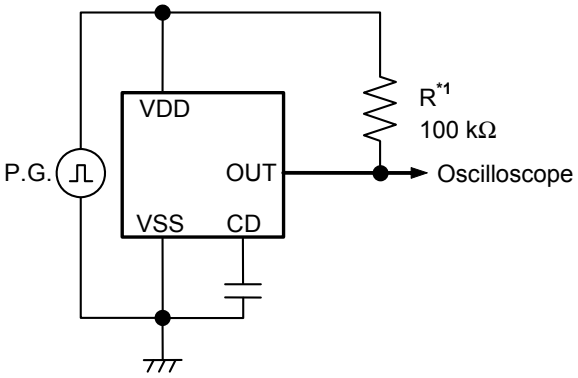


Figure 8 Test Circuit 3



***1.** R is unnecessary for CMOS output product.

Figure 9 Test Circuit 4

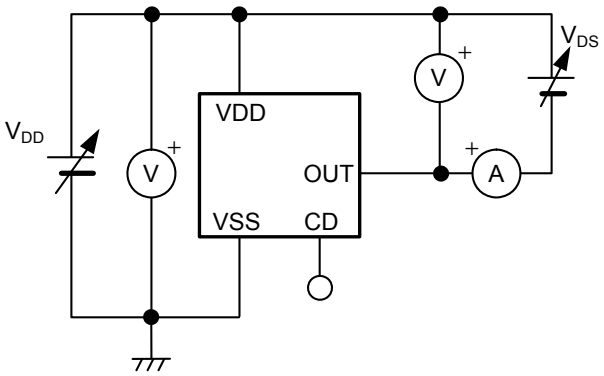


Figure 10 Test Circuit 5

■ Timing Charts

1. Nch open-drain output product

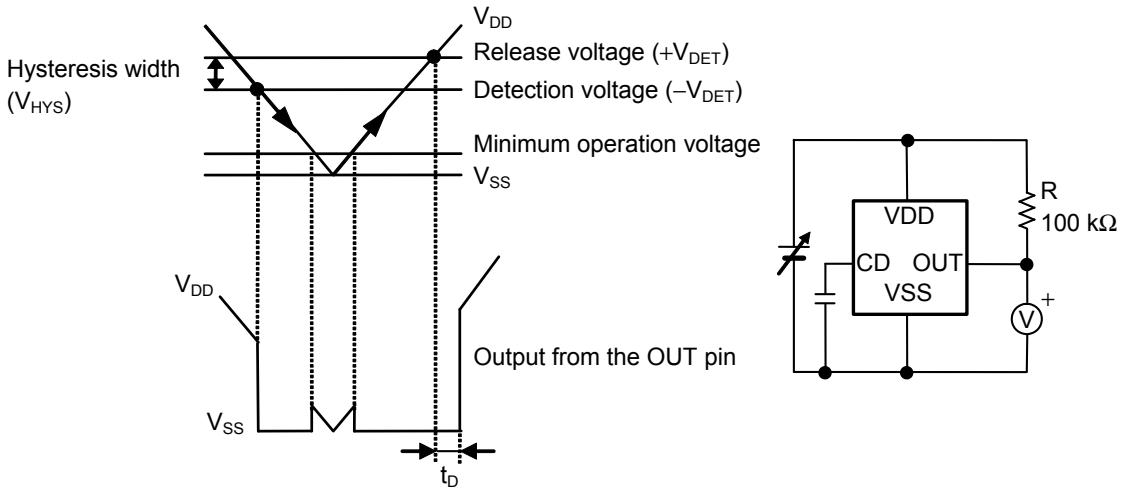
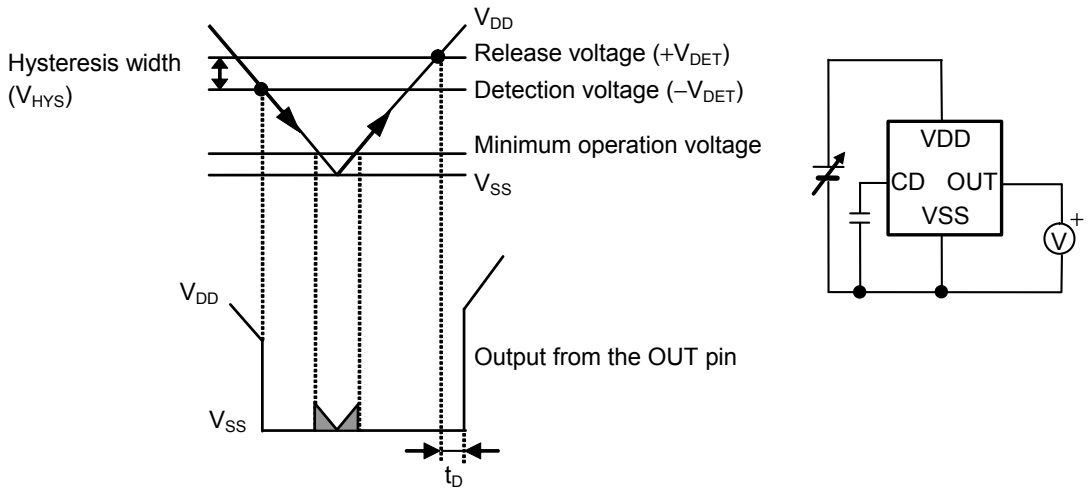


Figure 11

2. CMOS output product



Remark When V_{DD} is the minimum operation voltage or less, the output voltage from the OUT pin is indefinite in the shaded area.

Figure 12

■ Operation

1. Basic operation: CMOS output (active "L") product

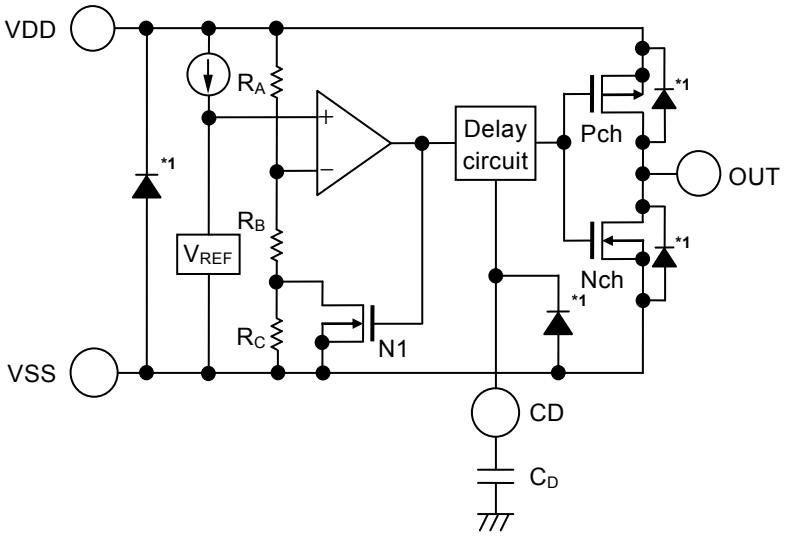
(1) When the power supply voltage (V_{DD}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off and the Pch transistor is turned on to output V_{DD} ("H"). Since the Nch transistor N1 in **Figure 13** is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) Even if V_{DD} decreases to $+V_{DET}$ or lower, V_{DD} is output when V_{DD} is higher than the detection voltage ($-V_{DET}$). When V_{DD} decreases to $-V_{DET}$ (point A in **Figure 14**) or lower, the Nch transistor is turned on and the Pch transistor is turned off, and then V_{SS} ("L") is output. At this time, the Nch transistor N1 in **Figure 13** is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

(3) The output is unstable if V_{DD} further decreases to the IC's minimum operation voltage or lower, and the output is V_{DD} when the output is pulled up.

(4) V_{SS} is output when V_{DD} increases to the minimum operation voltage or higher. Even if V_{DD} exceeds $-V_{DET}$, the output is V_{SS} when V_{DD} is lower than $+V_{DET}$.

(5) When V_{DD} increases to $+V_{DET}$ (point B in **Figure 14**) or higher, the Nch transistor is turned off and the Pch transistor is turned on, and then V_{DD} is output. At this time, V_{DD} is output from the OUT pin after the elapse of the delay time (t_D).



***1.** Parasitic diode

Figure 13 Operation 1

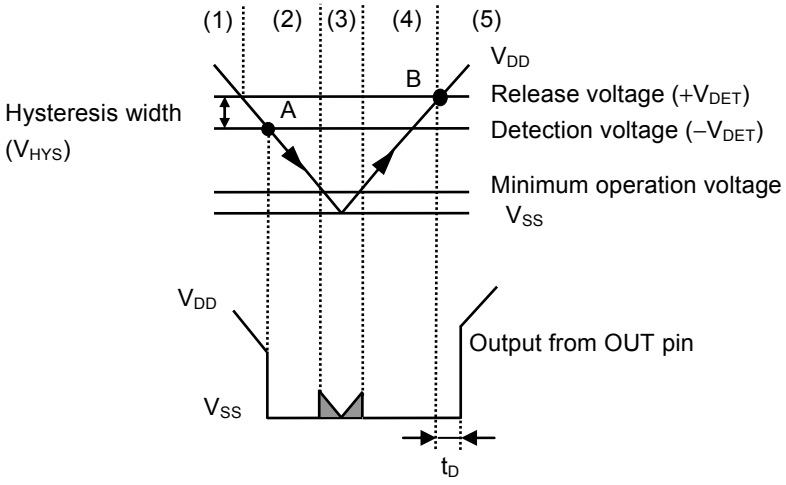


Figure 14 Operation 2

2. Delay circuit

The delay circuit delays the output signal to the OUT pin from the time at which the power supply voltage (V_{DD}) exceeds the release voltage ($+V_{DET}$) when the power supply voltage (V_{DD}) is turned on. The output signal is not delayed when V_{DD} decreases to the detection voltage ($-V_{DET}$) or less (refer to "**Figure 14 Operation 2**").
The delay time (t_D) is determined by the time constant of the built-in constant current (approx. 100 nA) and the attached delay capacitor (C_D), or the delay time when the CD pin is open (t_{D0}), and calculated from the following equation. When the C_D value is sufficiently large, the t_{D0} value can be ignored.

t_D [ms] = Delay coefficient $\times$ C_D [nF] + t_{D0} [ms]

Table 11 Delay Coefficient

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +105°C	2.58	3.70	5.40
Ta = +25°C	4.70	5.47	6.24
Ta = –40°C	5.64	8.40	12.01

Table 12 Delay Time

Operation Temperature	Delay Time when CD Pin is Open (t_{D0})		
	Min.	Typ.	Max.
Ta = –40°C to +105°C	0.01 ms	0.10 ms	0.80 ms

Caution 1. When the CD pin is open, a double pulse shown in Figure 15 may appear at release. To avoid the double pulse, attach 100 pF or more capacitor to the CD pin. Do not apply voltage to the CD pin from the exterior.

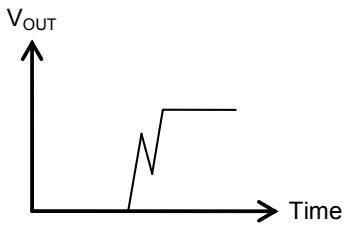
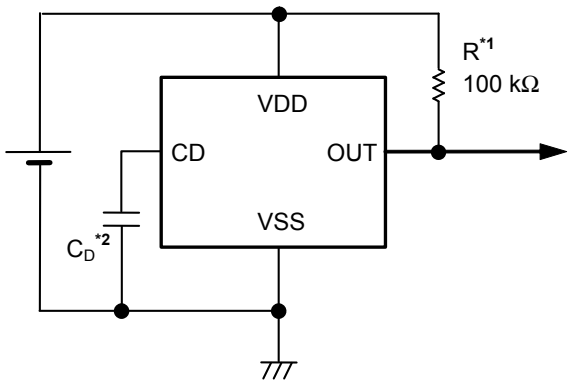


Figure 15

2. **Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.**
3. **There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value. Leakage current causes deviation in delay time. When the leakage current is larger than the built-in constant current, no release takes place.**

■ Standard Circuit



***1.** R is unnecessary for CMOS output products.
***2.** The delay capacitor (C_D) should be connected directly to the CD pin and the VSS pin.

Figure 16

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Explanation of Terms

1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 19** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (refer to **Figure 17**).

Example: In the S-19100C20H, the detection voltage is either one in the range of $1.948\ V \le -V_{DET} \le 2.052\ V$. This means, at the operation temperature Ta = −40°C to +105°C, some S-19100C20H have $-V_{DET}$ = 1.948 V and some have $-V_{DET}$ = 2.052 V.

2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 19** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (refer to **Figure 18**). The value is calculated from the actual detection voltage ($-V_{DET}$) of a product and is in the range of $-V_{DET} \times 1.03 \le +V_{DET} \le -V_{DET} \times 1.07$.

Example: In the S-19100C20H, the release voltage is either one in the range of $2.007\ V \le +V_{DET} \le 2.195\ V$. This means, at the operation temperature Ta = −40°C to +105°C, some S-19100C20H have $+V_{DET}$ = 2.007 V and some have $+V_{DET}$ = 2.195 V.

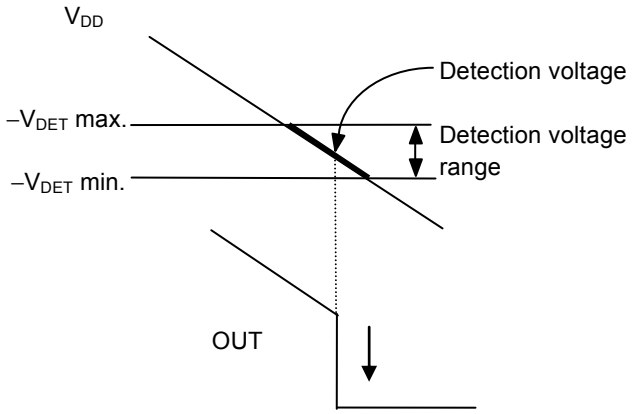


Figure 17 Detection Voltage

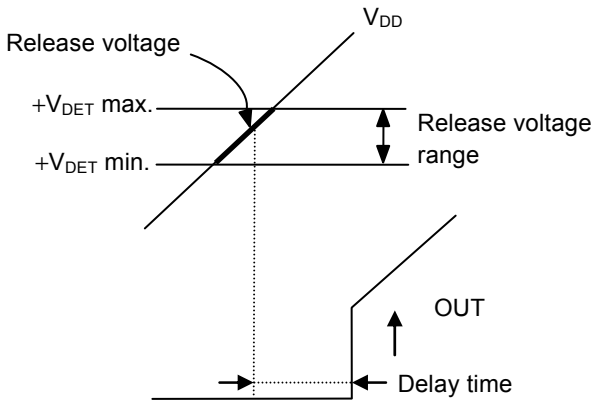
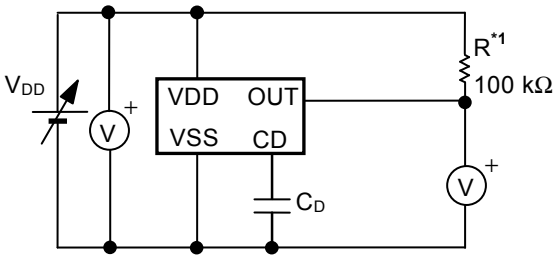


Figure 18 Release Voltage



***1.** R is unnecessary for CMOS output product.

Figure 19 Test Circuit of Detection Voltage and Release Voltage

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B − the voltage at point A = V_{HYS} in "**Figure 14 Operation 2**"). Setting the hysteresis width between the detection voltage and the release voltage to prevent malfunction caused by noise on the input voltage.

4. Delay time (t_D)

The delay time in the S-19100xxxH Series is a period from the input voltage to the VDD pin exceeding the release voltage ($+V_{DET}$) until the output from the OUT pin inverts. The delay time changes according to the delay capacitor (C_D).

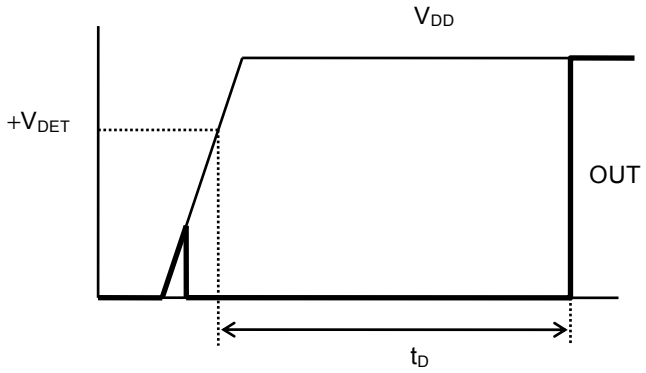


Figure 20 Delay Time

5. Feed-through current

Feed-through current is a current that flows instantaneously at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

6. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 21**), taking a CMOS output (active "L") product for example, the feed-through current which is generated when the output goes from "L" to "H" (release) causes a voltage drop equal to [feed-through current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

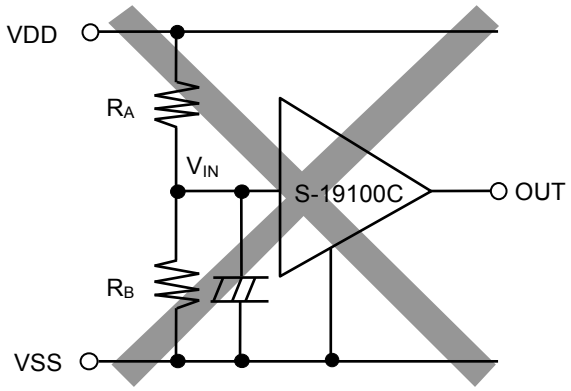


Figure 21 Example for Bad Implementation Due to Detection Voltage Change

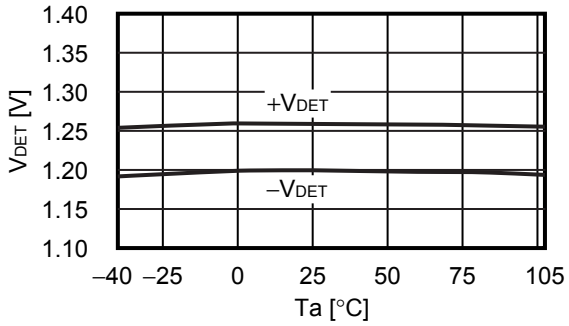
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output product, the feed-through current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the feed-through current during releasing.
- In CMOS output product, oscillation may occur when a pull-down resistor is used, and falling speed of the power supply voltage (V_{DD}) is slow near the detection voltage.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. SII Semiconductor Corporation shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

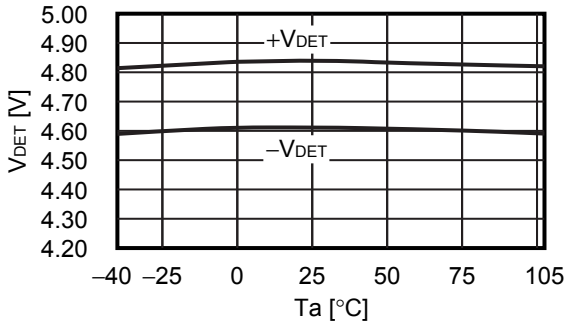
■ Characteristics (Typical Data)

1. Detection voltage (V_{DET}) vs. Temperature (Ta)

S-19100N12

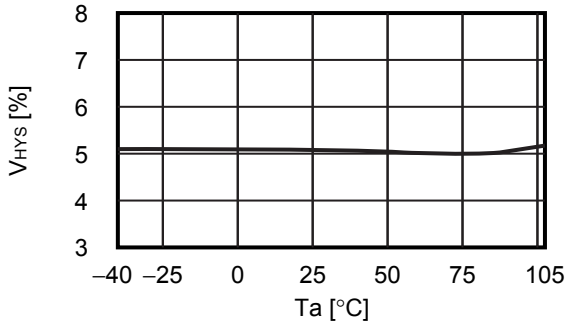


S-19100N46

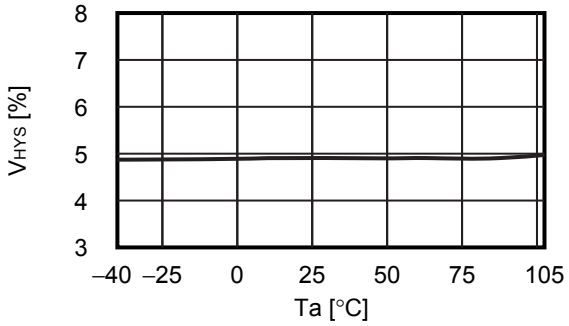


2. Hysteresis width (V_{HYS}) vs. Temperature (Ta)

S-19100N12

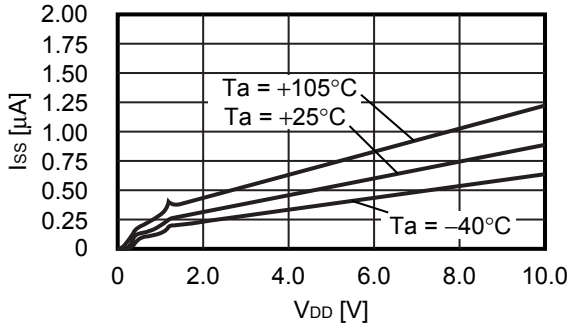


S-19100N46

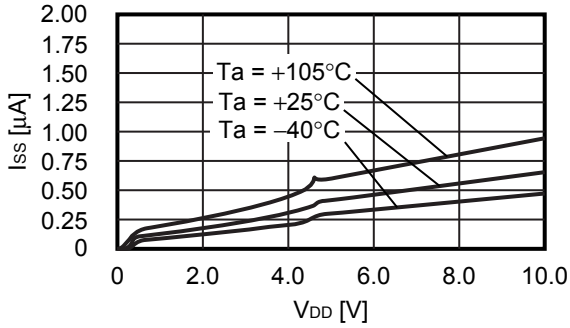


3. Current consumption (I_{SS}) vs. Input voltage (V_{DD})

S-19100C12

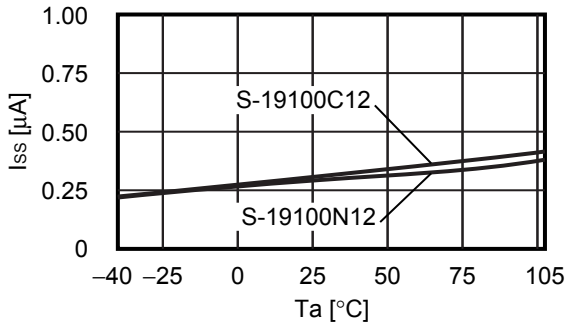


S-19100C46

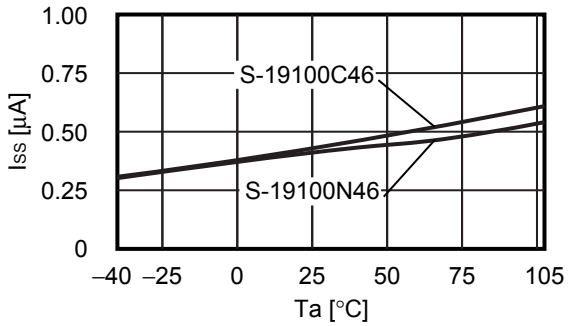


4. Current consumption (I_{SS}) vs. Temperature (Ta)

S-19100N12/19100C12 V_{DD} = +V_{DET} + 0.6 V

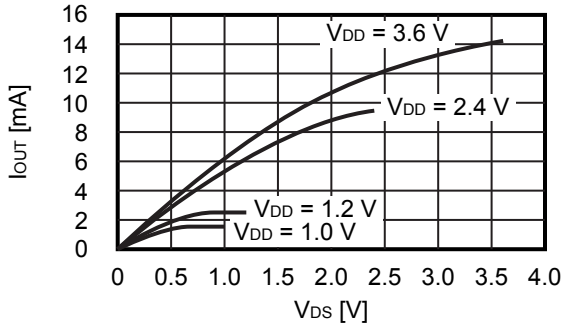


S-19100N46/19100C46 V_{DD} = +V_{DET} + 0.6 V

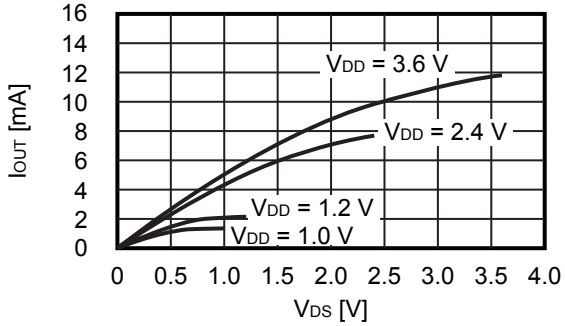


5. Nch transistor output current (I_{OUT}) vs. V_{DS}

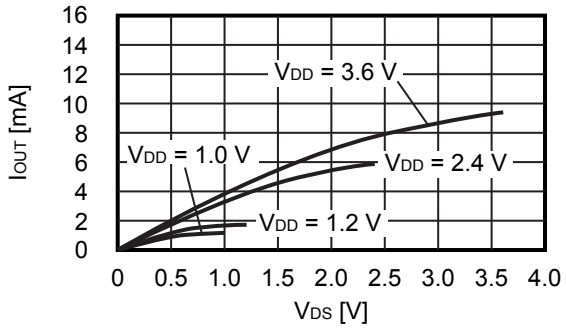
S-19100N46 Ta = –40°C



S-19100N46 Ta = +25°C

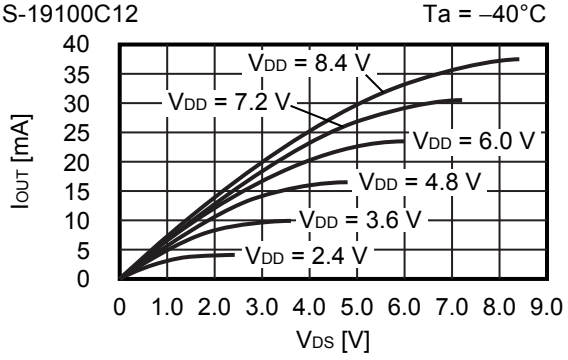


S-19100N46 Ta = +105°C

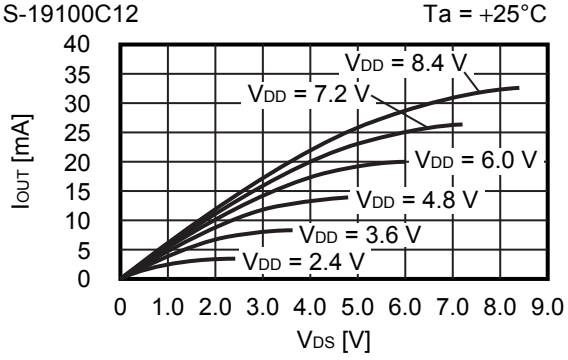


6. Pch transistor output current (I_{OUT}) vs. V_{DS}

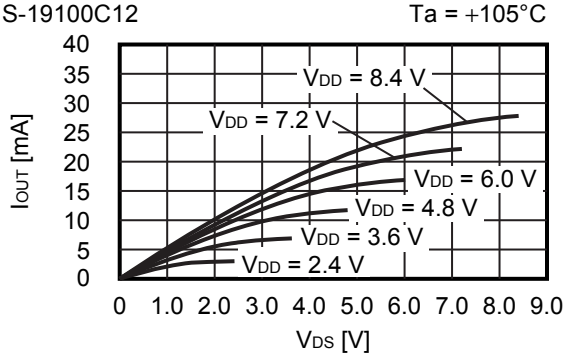
S-19100C12 Ta = –40°C



S-19100C12 Ta = +25°C



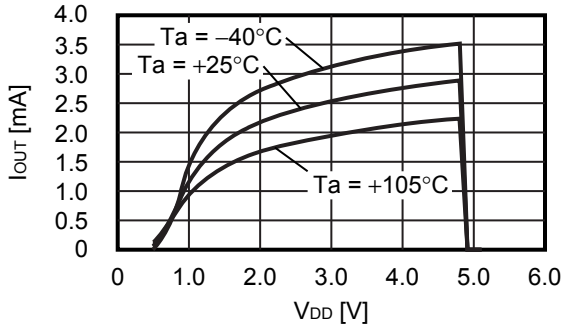
S-19100C12 Ta = +105°C



Remark V_{DS}: Drain-to-source voltage of the output transistor

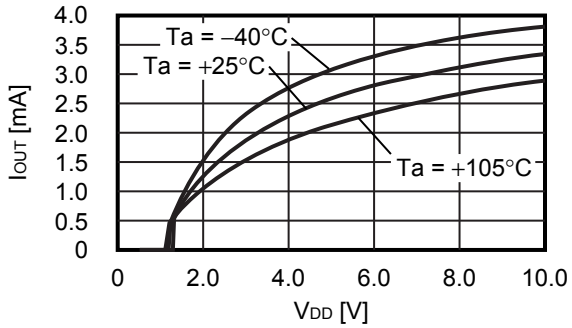
7. Nch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})

S-19100N46 V_{DS} = 0.5 V



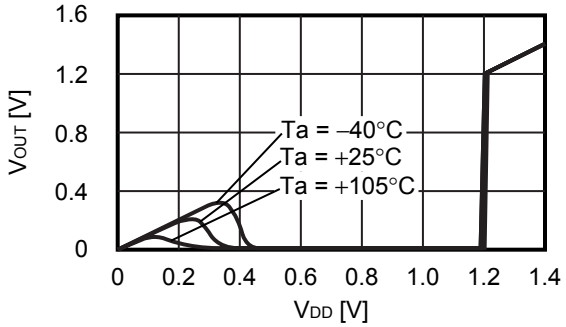
8. Pch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})

S-19100C12 V_{DS} = 0.5 V

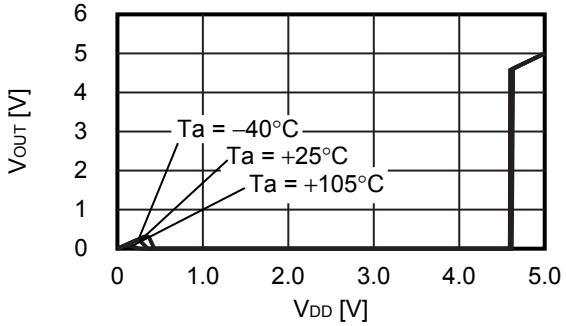


9. Minimum operation voltage (V_{OUT}) vs. Input voltage (V_{DD})

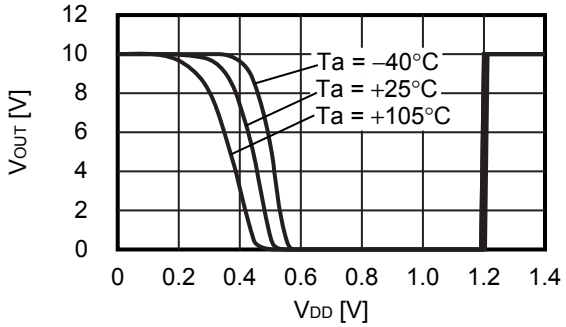
S-19100N12 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



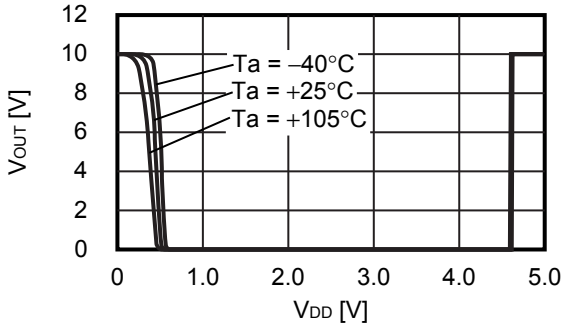
S-19100N46 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



S-19100N12 Pull-up to 10 V
Pull-up resistance: 100 kΩ



S-19100N46 Pull-up to 10 V
Pull-up resistance: 100 kΩ

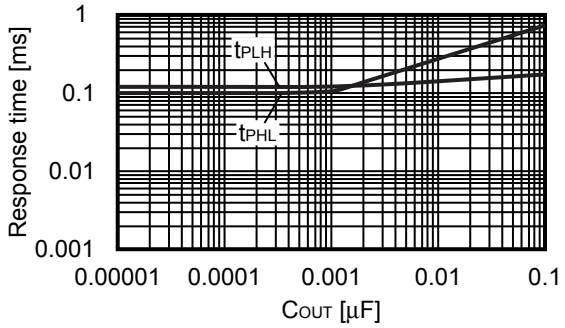


Remark V_{DS}: Drain-to-source voltage of the output transistor

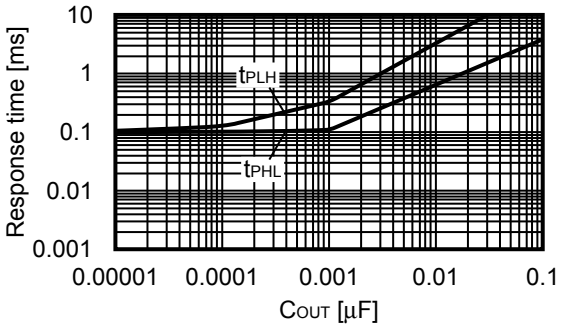
10. Dynamic response characteristics vs. Output pin capacitance (C_{OUT}) (CD pin; open)

10. 1 $-V_{DET}$ = 1.2 V

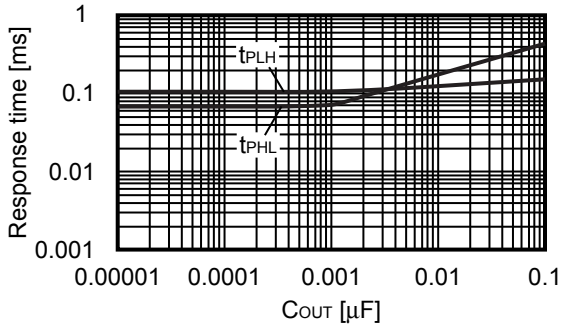
S-19100C12 Ta = −40°C



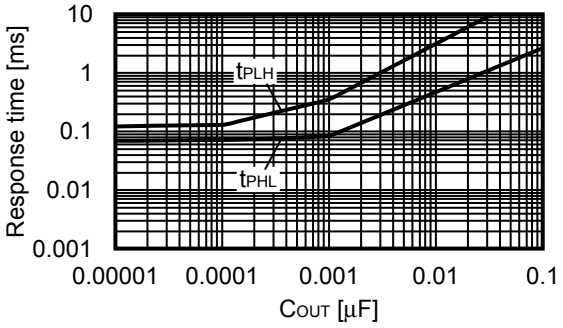
S-19100N12 Ta = −40°C



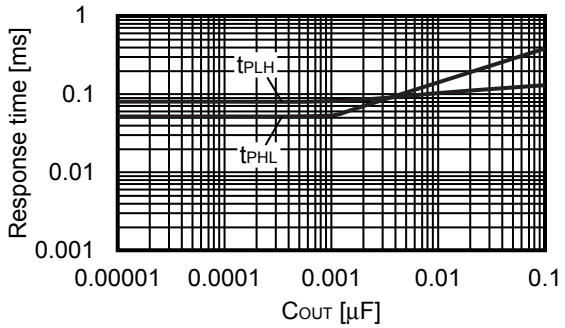
S-19100C12 Ta = +25°C



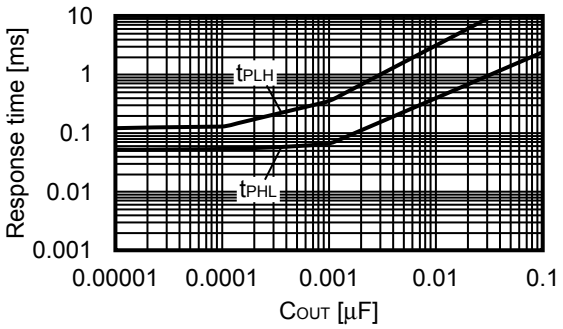
S-19100N12 Ta = +25°C



S-19100C12 Ta = +105°C

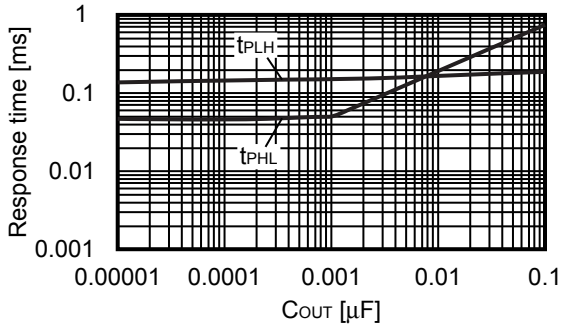


S-19100N12 Ta = +105°C

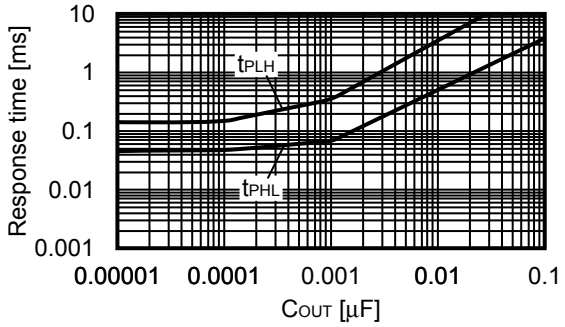


10. 2 $-V_{DET}$ = 4.6 V

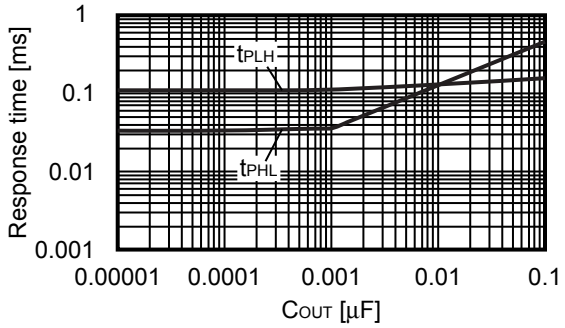
S-19100C46 Ta = –40°C



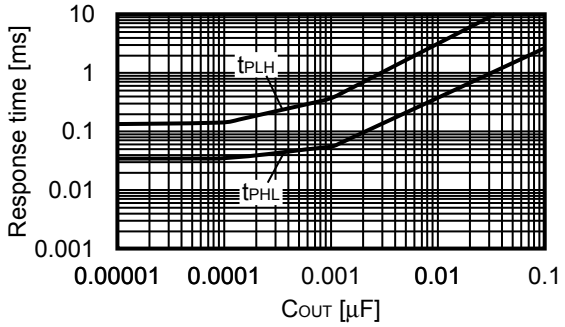
S-19100N46 Ta = –40°C



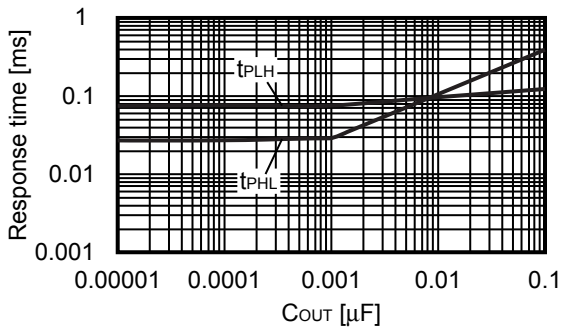
S-19100C46 Ta = +25°C



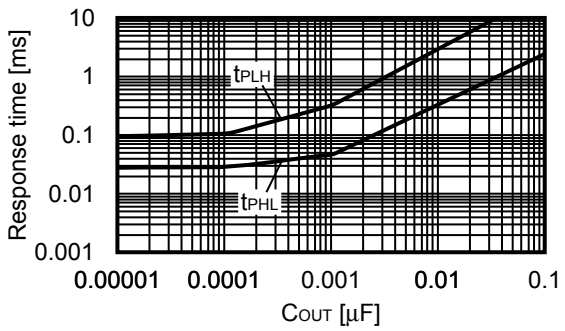
S-19100N46 Ta = +25°C

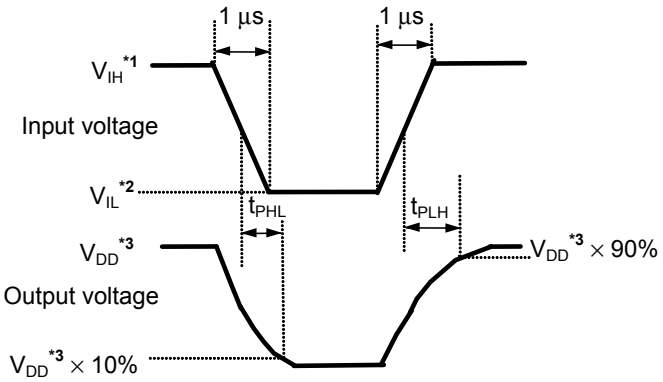


S-19100C46 Ta = +105°C



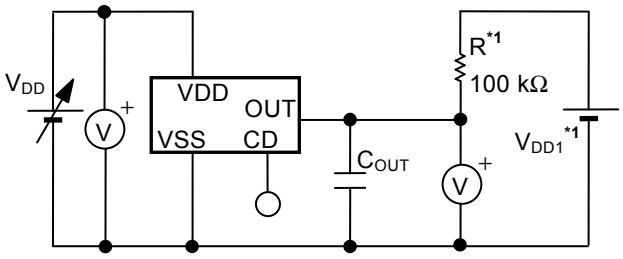
S-19100N46 Ta = +105°C





***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.8 V
***3.** CMOS output product: V_{DD}
Nch open-drain product: V_{DD1}

Figure 22 Test Condition of Response Time



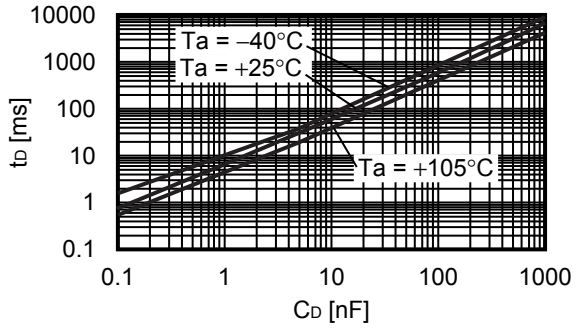
***1.** R and V_{DD1} are unnecessary for CMOS output product.

Figure 23 Test Circuit of Response Time

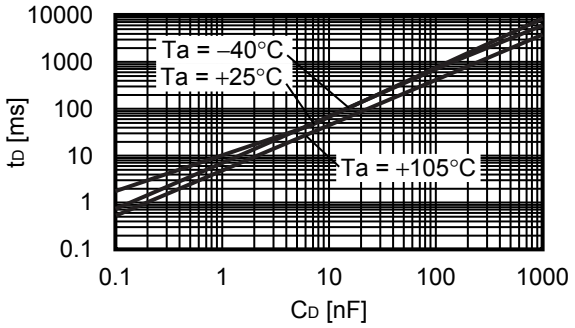
Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
2. When the CD pin is open, a double pulse may appear at release. To avoid the double pulse, attach 100 pF or more capacitor to the CD pin. Response time when detecting (t_{PHL}) is not affected by CD pin capacitance. Besides, response time when releasing (t_{PLH}) can set the delay time by attaching the CD pin. Refer to "11. Delay time (t_D) vs. CD pin capacitance (C_D) (without output pin capacitance)" for details.

11. Delay time (t_D) vs. CD pin capacitance (C_D) (without output pin capacitance)

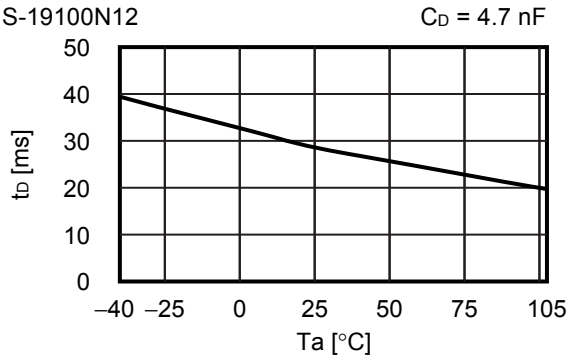
S-19100C12

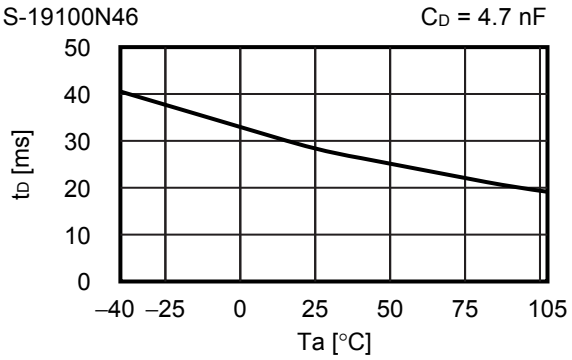


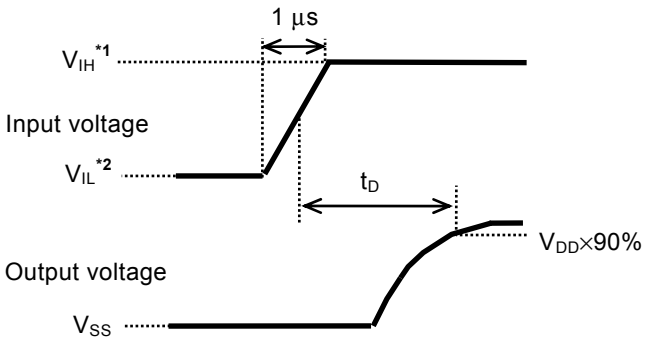
S-19100C46



12. Delay time (t_D) vs. Temperature (Ta)

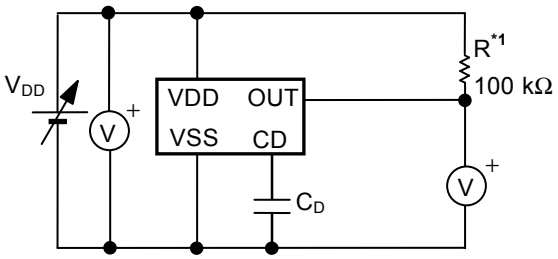






***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.8 V

Figure 24 Test Condition of Delay Time



***1.** R is unnecessary for CMOS output product.

Figure 25 Test Circuit of Delay Time

**Caution The above connection diagram and constant will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constant.**

■ Application Circuit Examples

1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the minimum operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.
Using the S-19100xxxH Series which has the low minimum operation voltage, a high-accuracy detection voltage and hysteresis, reset circuits can be easily constructed as seen in **Figure 26** and **Figure 27**.

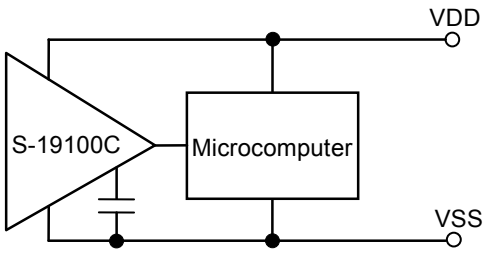


Figure 26 Example of Reset Circuit (CMOS Output Product)

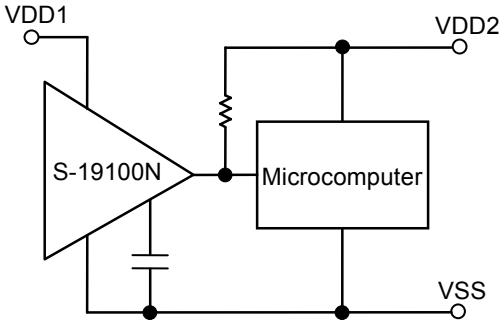
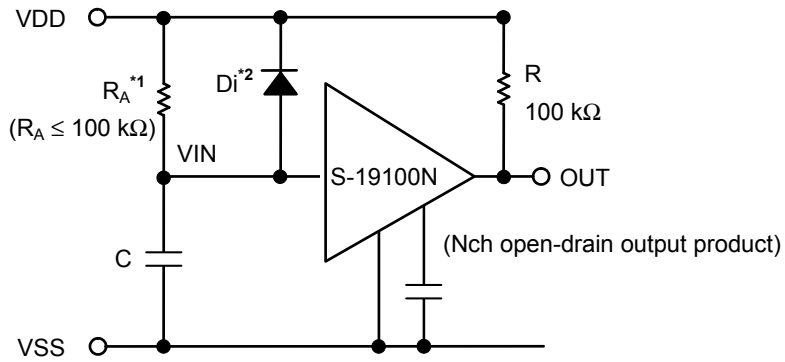


Figure 27 Example of Reset Circuit (Nch Open-drain Output Product)

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Power-on reset circuit (Nch open-drain output product only)

A power-on reset circuit can be constructed using the S-19100NxxH Series.



***1.** R_A should be 100 kΩ or less to prevent oscillation.

***2.** Diode (Di) instantaneously discharges the charge stored in the capacitor (C) at the power falling. Di can be removed when the delay of the falling time is not important.

Figure 28

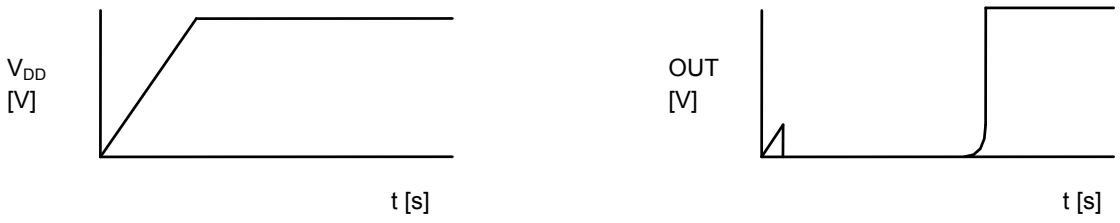


Figure 29

Remark When the power rises sharply, the output may instantaneously be set to the "H" level due to the IC's indefinite area (the output voltage is indefinite when it is the IC's minimum operation voltage or less), as seen in **Figure 30.**

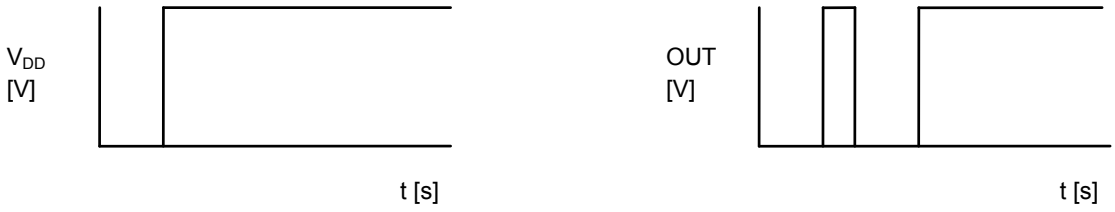


Figure 30

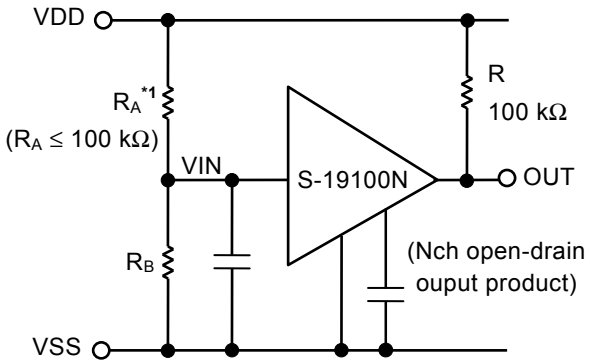
Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Note that the hysteresis width may be larger as the following equation shows when using the above connection. Perform thorough evaluation using the actual application to set the constant.

Maximum hysteresis width = V_{HYS} + R_A • 20 μA

3. Change of detection voltage (Nch open-drain output product only)

If there is not a product with a specified detection voltage value in the S-19100NxxH Series, the detection voltage can be changed by using a resistance divider or a diode, as seen in **Figure 31** and **Figure 32**.
In **Figure 31**, the hysteresis width also changes.



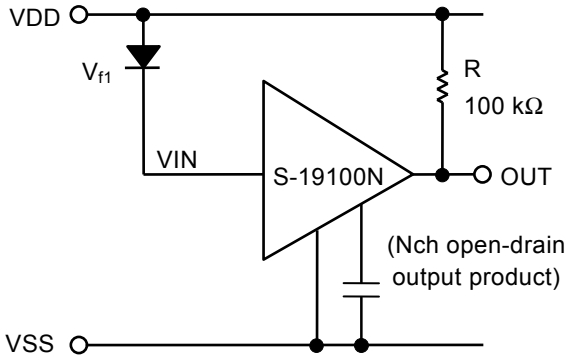
Detection voltage = $\frac{R_A + R_B}{R_B} \bullet -V_{DET}$

Hysteresis width = $\frac{R_A + R_B}{R_B} \bullet V_{HYS}$

***1.** R_A should be 100 kΩ or less to prevent oscillation.

Caution If R_A and R_B are large, the hysteresis width may also be larger than the value given by the above equation due to the feed-through current.

Figure 31



Detection voltage = $V_{f1} + (-V_{DET})$

Figure 32

Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

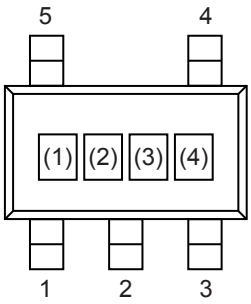
2. Note that the hysteresis width may be larger as the following equation shows when using the above connections. Perform thorough evaluation using the actual application to set the constant.

Maximum hysteresis width = $\frac{R_A + R_B}{R_B} \bullet V_{HYS} + R_A \bullet 20\ \mu A$

■ Marking Specifications

1. SOT-23-5

Top view



(1) to (3): Product code (Refer to **Product name vs. Product code**)
(4): Lot number

Product name vs. Product code

1. 1 Nch open-drain output product

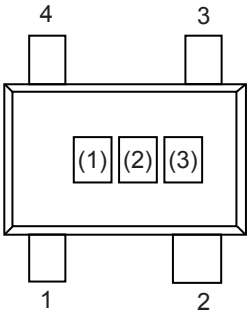
Product Name	Product Code		
	(1)	(2)	(3)
S-19100N12H-M5T2U	3	P	A
S-19100N13H-M5T2U	3	P	B
S-19100N14H-M5T2U	3	P	C
S-19100N15H-M5T2U	3	P	D
S-19100N16H-M5T2U	3	P	E
S-19100N17H-M5T2U	3	P	F
S-19100N18H-M5T2U	3	P	G
S-19100N19H-M5T2U	3	P	H
S-19100N20H-M5T2U	3	P	I
S-19100N21H-M5T2U	3	P	J
S-19100N22H-M5T2U	3	P	K
S-19100N23H-M5T2U	3	P	L
S-19100N24H-M5T2U	3	P	M
S-19100N25H-M5T2U	3	P	N
S-19100N26H-M5T2U	3	P	O
S-19100N27H-M5T2U	3	P	P
S-19100N28H-M5T2U	3	P	Q
S-19100N29H-M5T2U	3	P	R
S-19100N30H-M5T2U	3	P	S
S-19100N31H-M5T2U	3	P	T
S-19100N32H-M5T2U	3	P	U
S-19100N33H-M5T2U	3	P	V
S-19100N34H-M5T2U	3	P	W
S-19100N35H-M5T2U	3	P	X
S-19100N36H-M5T2U	3	P	Y
S-19100N37H-M5T2U	3	P	Z
S-19100N38H-M5T2U	3	P	1
S-19100N39H-M5T2U	3	P	2
S-19100N40H-M5T2U	3	P	3
S-19100N41H-M5T2U	3	P	4
S-19100N42H-M5T2U	3	P	5
S-19100N43H-M5T2U	3	P	6
S-19100N44H-M5T2U	3	P	7
S-19100N45H-M5T2U	3	P	8
S-19100N46H-M5T2U	3	P	9

1. 2 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-19100C12H-M5T2U	3	O	A
S-19100C13H-M5T2U	3	O	B
S-19100C14H-M5T2U	3	O	C
S-19100C15H-M5T2U	3	O	D
S-19100C16H-M5T2U	3	O	E
S-19100C17H-M5T2U	3	O	F
S-19100C18H-M5T2U	3	O	G
S-19100C19H-M5T2U	3	O	H
S-19100C20H-M5T2U	3	O	I
S-19100C21H-M5T2U	3	O	J
S-19100C22H-M5T2U	3	O	K
S-19100C23H-M5T2U	3	O	L
S-19100C24H-M5T2U	3	O	M
S-19100C25H-M5T2U	3	O	N
S-19100C26H-M5T2U	3	O	O
S-19100C27H-M5T2U	3	O	P
S-19100C28H-M5T2U	3	O	Q
S-19100C29H-M5T2U	3	O	R
S-19100C30H-M5T2U	3	O	S
S-19100C31H-M5T2U	3	O	T
S-19100C32H-M5T2U	3	O	U
S-19100C33H-M5T2U	3	O	V
S-19100C34H-M5T2U	3	O	W
S-19100C35H-M5T2U	3	O	X
S-19100C36H-M5T2U	3	O	Y
S-19100C37H-M5T2U	3	O	Z
S-19100C38H-M5T2U	3	O	1
S-19100C39H-M5T2U	3	O	2
S-19100C40H-M5T2U	3	O	3
S-19100C41H-M5T2U	3	O	4
S-19100C42H-M5T2U	3	O	5
S-19100C43H-M5T2U	3	O	6
S-19100C44H-M5T2U	3	O	7
S-19100C45H-M5T2U	3	O	8
S-19100C46H-M5T2U	3	O	9

2. SC-82AB

Top view



(1) to (3): Product code (Refer to **Product name vs. Product code**)

Product name vs. Product code

2. 1 Nch open-drain output product

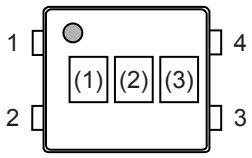
Product Name	Product Code		
	(1)	(2)	(3)
S-19100N12H-N4T2U	3	P	A
S-19100N13H-N4T2U	3	P	B
S-19100N14H-N4T2U	3	P	C
S-19100N15H-N4T2U	3	P	D
S-19100N16H-N4T2U	3	P	E
S-19100N17H-N4T2U	3	P	F
S-19100N18H-N4T2U	3	P	G
S-19100N19H-N4T2U	3	P	H
S-19100N20H-N4T2U	3	P	I
S-19100N21H-N4T2U	3	P	J
S-19100N22H-N4T2U	3	P	K
S-19100N23H-N4T2U	3	P	L
S-19100N24H-N4T2U	3	P	M
S-19100N25H-N4T2U	3	P	N
S-19100N26H-N4T2U	3	P	O
S-19100N27H-N4T2U	3	P	P
S-19100N28H-N4T2U	3	P	Q
S-19100N29H-N4T2U	3	P	R
S-19100N30H-N4T2U	3	P	S
S-19100N31H-N4T2U	3	P	T
S-19100N32H-N4T2U	3	P	U
S-19100N33H-N4T2U	3	P	V
S-19100N34H-N4T2U	3	P	W
S-19100N35H-N4T2U	3	P	X
S-19100N36H-N4T2U	3	P	Y
S-19100N37H-N4T2U	3	P	Z
S-19100N38H-N4T2U	3	P	1
S-19100N39H-N4T2U	3	P	2
S-19100N40H-N4T2U	3	P	3
S-19100N41H-N4T2U	3	P	4
S-19100N42H-N4T2U	3	P	5
S-19100N43H-N4T2U	3	P	6
S-19100N44H-N4T2U	3	P	7
S-19100N45H-N4T2U	3	P	8
S-19100N46H-N4T2U	3	P	9

2. 2 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-19100C12H-N4T2U	3	O	A
S-19100C13H-N4T2U	3	O	B
S-19100C14H-N4T2U	3	O	C
S-19100C15H-N4T2U	3	O	D
S-19100C16H-N4T2U	3	O	E
S-19100C17H-N4T2U	3	O	F
S-19100C18H-N4T2U	3	O	G
S-19100C19H-N4T2U	3	O	H
S-19100C20H-N4T2U	3	O	I
S-19100C21H-N4T2U	3	O	J
S-19100C22H-N4T2U	3	O	K
S-19100C23H-N4T2U	3	O	L
S-19100C24H-N4T2U	3	O	M
S-19100C25H-N4T2U	3	O	N
S-19100C26H-N4T2U	3	O	O
S-19100C27H-N4T2U	3	O	P
S-19100C28H-N4T2U	3	O	Q
S-19100C29H-N4T2U	3	O	R
S-19100C30H-N4T2U	3	O	S
S-19100C31H-N4T2U	3	O	T
S-19100C32H-N4T2U	3	O	U
S-19100C33H-N4T2U	3	O	V
S-19100C34H-N4T2U	3	O	W
S-19100C35H-N4T2U	3	O	X
S-19100C36H-N4T2U	3	O	Y
S-19100C37H-N4T2U	3	O	Z
S-19100C38H-N4T2U	3	O	1
S-19100C39H-N4T2U	3	O	2
S-19100C40H-N4T2U	3	O	3
S-19100C41H-N4T2U	3	O	4
S-19100C42H-N4T2U	3	O	5
S-19100C43H-N4T2U	3	O	6
S-19100C44H-N4T2U	3	O	7
S-19100C45H-N4T2U	3	O	8
S-19100C46H-N4T2U	3	O	9

3. SNT-4A

Top view



(1) to (3): Product code (refer to **Product name vs. Product code**)

Product name vs. Product code

3. 1 Nch open-drain output product

Product Name	Product Code		
	(1)	(2)	(3)
S-19100N12H-I4T1U	3	P	A
S-19100N13H-I4T1U	3	P	B
S-19100N14H-I4T1U	3	P	C
S-19100N15H-I4T1U	3	P	D
S-19100N16H-I4T1U	3	P	E
S-19100N17H-I4T1U	3	P	F
S-19100N18H-I4T1U	3	P	G
S-19100N19H-I4T1U	3	P	H
S-19100N20H-I4T1U	3	P	I
S-19100N21H-I4T1U	3	P	J
S-19100N22H-I4T1U	3	P	K
S-19100N23H-I4T1U	3	P	L
S-19100N24H-I4T1U	3	P	M
S-19100N25H-I4T1U	3	P	N
S-19100N26H-I4T1U	3	P	O
S-19100N27H-I4T1U	3	P	P
S-19100N28H-I4T1U	3	P	Q
S-19100N29H-I4T1U	3	P	R
S-19100N30H-I4T1U	3	P	S
S-19100N31H-I4T1U	3	P	T
S-19100N32H-I4T1U	3	P	U
S-19100N33H-I4T1U	3	P	V
S-19100N34H-I4T1U	3	P	W
S-19100N35H-I4T1U	3	P	X
S-19100N36H-I4T1U	3	P	Y
S-19100N37H-I4T1U	3	P	Z
S-19100N38H-I4T1U	3	P	1
S-19100N39H-I4T1U	3	P	2
S-19100N40H-I4T1U	3	P	3
S-19100N41H-I4T1U	3	P	4
S-19100N42H-I4T1U	3	P	5
S-19100N43H-I4T1U	3	P	6
S-19100N44H-I4T1U	3	P	7
S-19100N45H-I4T1U	3	P	8
S-19100N46H-I4T1U	3	P	9

3. 2 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-19100C12H-I4T1U	3	O	A
S-19100C13H-I4T1U	3	O	B
S-19100C14H-I4T1U	3	O	C
S-19100C15H-I4T1U	3	O	D
S-19100C16H-I4T1U	3	O	E
S-19100C17H-I4T1U	3	O	F
S-19100C18H-I4T1U	3	O	G
S-19100C19H-I4T1U	3	O	H
S-19100C20H-I4T1U	3	O	I
S-19100C21H-I4T1U	3	O	J
S-19100C22H-I4T1U	3	O	K
S-19100C23H-I4T1U	3	O	L
S-19100C24H-I4T1U	3	O	M
S-19100C25H-I4T1U	3	O	N
S-19100C26H-I4T1U	3	O	O
S-19100C27H-I4T1U	3	O	P
S-19100C28H-I4T1U	3	O	Q
S-19100C29H-I4T1U	3	O	R
S-19100C30H-I4T1U	3	O	S
S-19100C31H-I4T1U	3	O	T
S-19100C32H-I4T1U	3	O	U
S-19100C33H-I4T1U	3	O	V
S-19100C34H-I4T1U	3	O	W
S-19100C35H-I4T1U	3	O	X
S-19100C36H-I4T1U	3	O	Y
S-19100C37H-I4T1U	3	O	Z
S-19100C38H-I4T1U	3	O	1
S-19100C39H-I4T1U	3	O	2
S-19100C40H-I4T1U	3	O	3
S-19100C41H-I4T1U	3	O	4
S-19100C42H-I4T1U	3	O	5
S-19100C43H-I4T1U	3	O	6
S-19100C44H-I4T1U	3	O	7
S-19100C45H-I4T1U	3	O	8
S-19100C46H-I4T1U	3	O	9

■ Thermal Characteristics

1. SOT-23-5

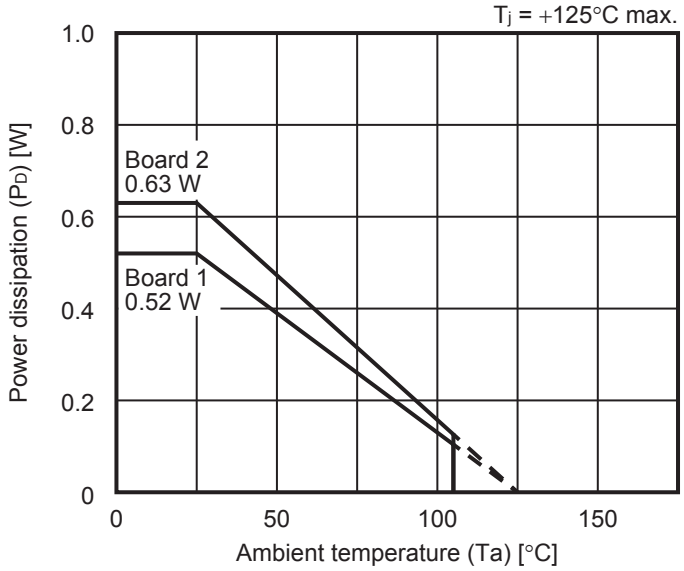


Figure 33 Power Dissipation of Package (When Mounted on Board)

1. 1 Board 1*1

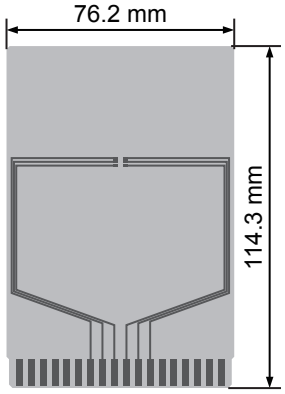


Figure 34

Table 13

Item		Specification
Thermal resistance value (θ_{ja})		192°C/W
Size		114.3 mm × 76.2 mm × t1.6 mm
Material		FR-4
Number of copper foil layer		2
Copper foil layer	1	Land pattern and wiring for testing: t0.070 mm
	2	–
	3	–
	4	74.2 mm × 74.2 mm × t0.070 mm
Thermal via		–

1. 2 Board 2*1

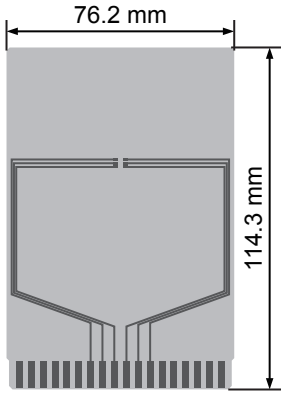


Figure 35

Table 14

Item		Specification
Thermal resistance value (θ_{ja})		160°C/W
Size		114.3 mm × 76.2 mm × t1.6 mm
Material		FR-4
Number of copper foil layer		4
Copper foil layer	1	Land pattern and wiring for testing: t0.070 mm
	2	74.2 mm × 74.2 mm × t0.035 mm
	3	74.2 mm × 74.2 mm × t0.035 mm
	4	74.2 mm × 74.2 mm × t0.070 mm
Thermal via		–

***1.** The board is same in SOT-23-3, SOT-23-5 and SOT-23-6.

2. SC-82AB

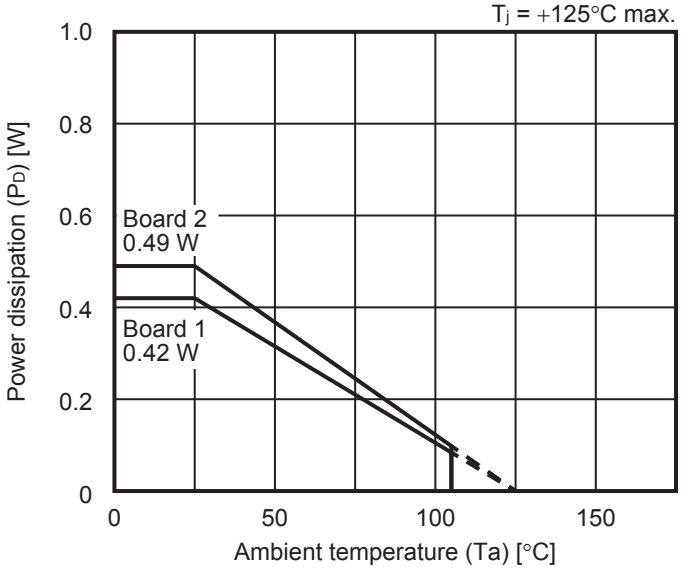


Figure 36 Power Dissipation of Package (When Mounted on Board)

2. 1 Board 1

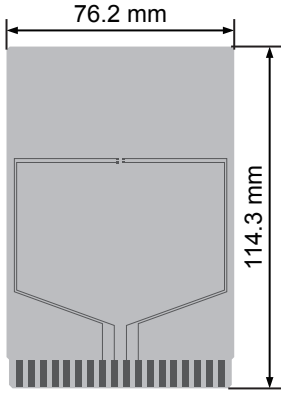


Figure 37

Table 15

Item		Specification
Thermal resistance value (θ_{ja})		236°C/W
Size		114.3 mm × 76.2 mm × t1.6 mm
Material		FR-4
Number of copper foil layer		2
Copper foil layer	1	Land pattern and wiring for testing: t0.070 mm
	2	–
	3	–
	4	74.2 mm × 74.2 mm × t0.070 mm
Thermal via		–

2. 2 Board 2

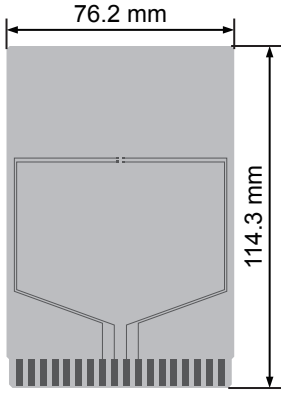


Figure 38

Table 16

Item		Specification
Thermal resistance value (θ_{ja})		204°C/W
Size		114.3 mm × 76.2 mm × t1.6 mm
Material		FR-4
Number of copper foil layer		4
Copper foil layer	1	Land pattern and wiring for testing: t0.070 mm
	2	74.2 mm × 74.2 mm × t0.035 mm
	3	74.2 mm × 74.2 mm × t0.035 mm
	4	74.2 mm × 74.2 mm × t0.070 mm
Thermal via		–

3. SNT-4A

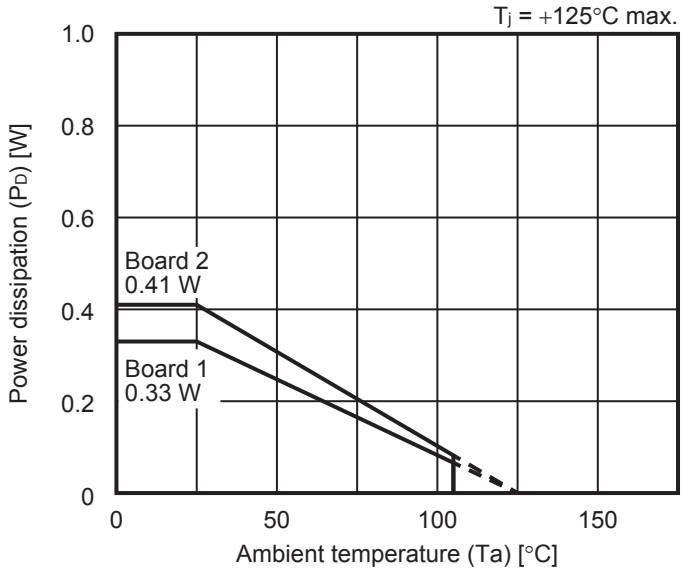


Figure 39 Power Dissipation of Package (When Mounted on Board)

3. 1 Board 1

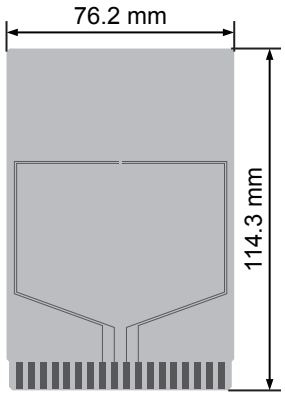


Figure 40

Table 17

Item		Specification
Thermal resistance value (θ_{ja})		300°C/W
Size		114.3 mm × 76.2 mm × t1.6 mm
Material		FR-4
Number of copper foil layer		2
Copper foil layer	1	Land pattern and wiring for testing: t0.070 mm
	2	–
	3	–
	4	74.2 mm × 74.2 mm × t0.070 mm
Thermal via		–

3. 2 Board 2

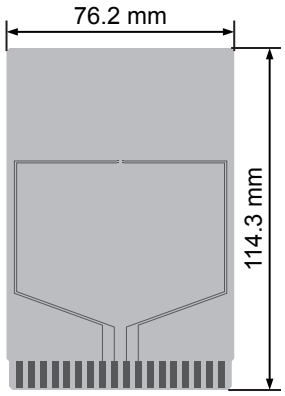
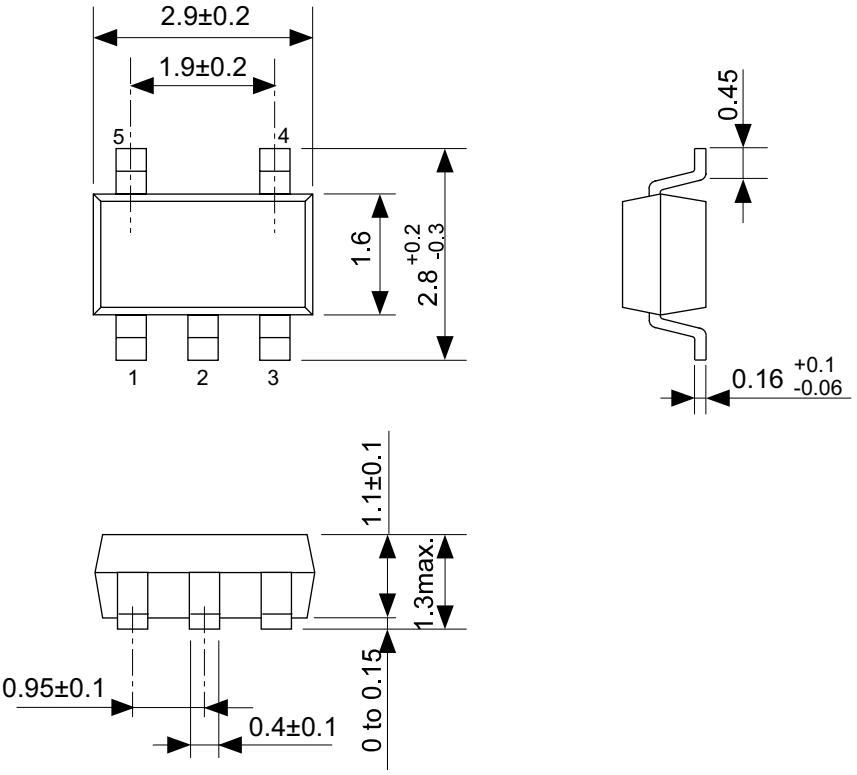


Figure 41

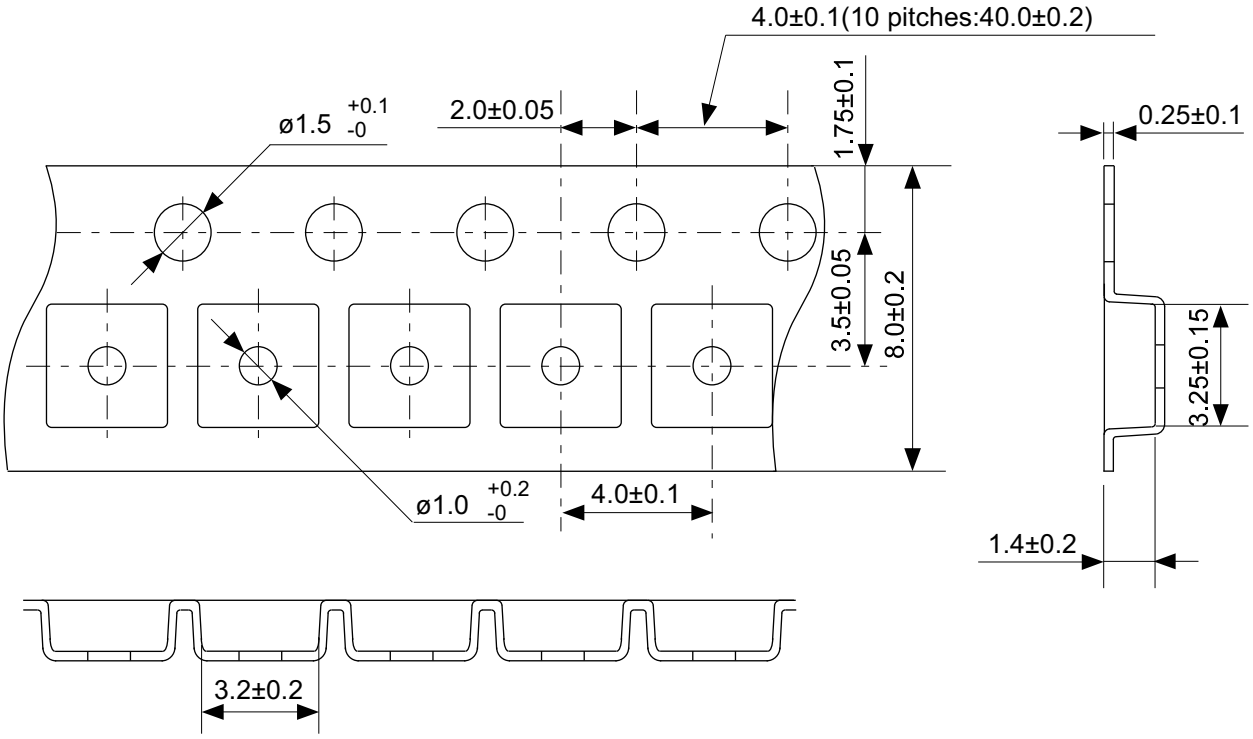
Table 18

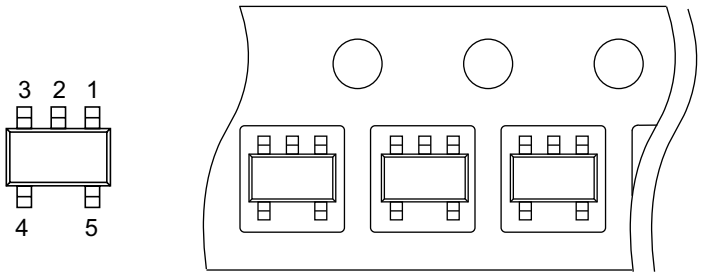
Item		Specification
Thermal resistance value (θ_{ja})		242°C/W
Size		114.3 mm × 76.2 mm × t1.6 mm
Material		FR-4
Number of copper foil layer		4
Copper foil layer	1	Land pattern and wiring for testing: t0.070 mm
	2	74.2 mm × 74.2 mm × t0.035 mm
	3	74.2 mm × 74.2 mm × t0.035 mm
	4	74.2 mm × 74.2 mm × t0.070 mm
Thermal via		–



No. MP005-A-P-SD-1.2

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.2
SCALE	
UNIT	mm
SII Semiconductor Corporation	

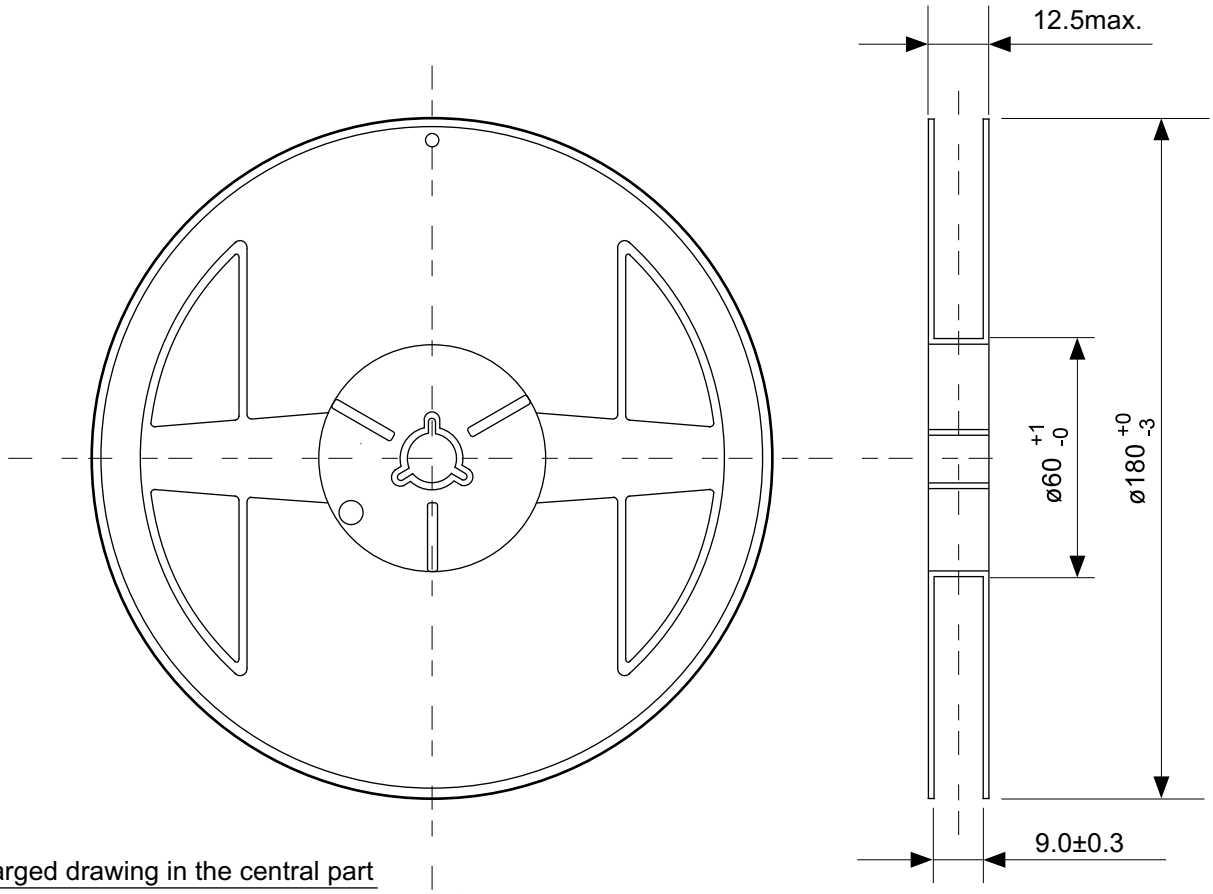




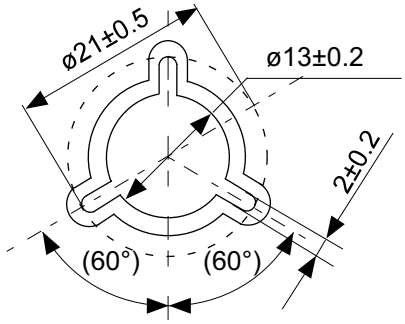
Feed direction

No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	

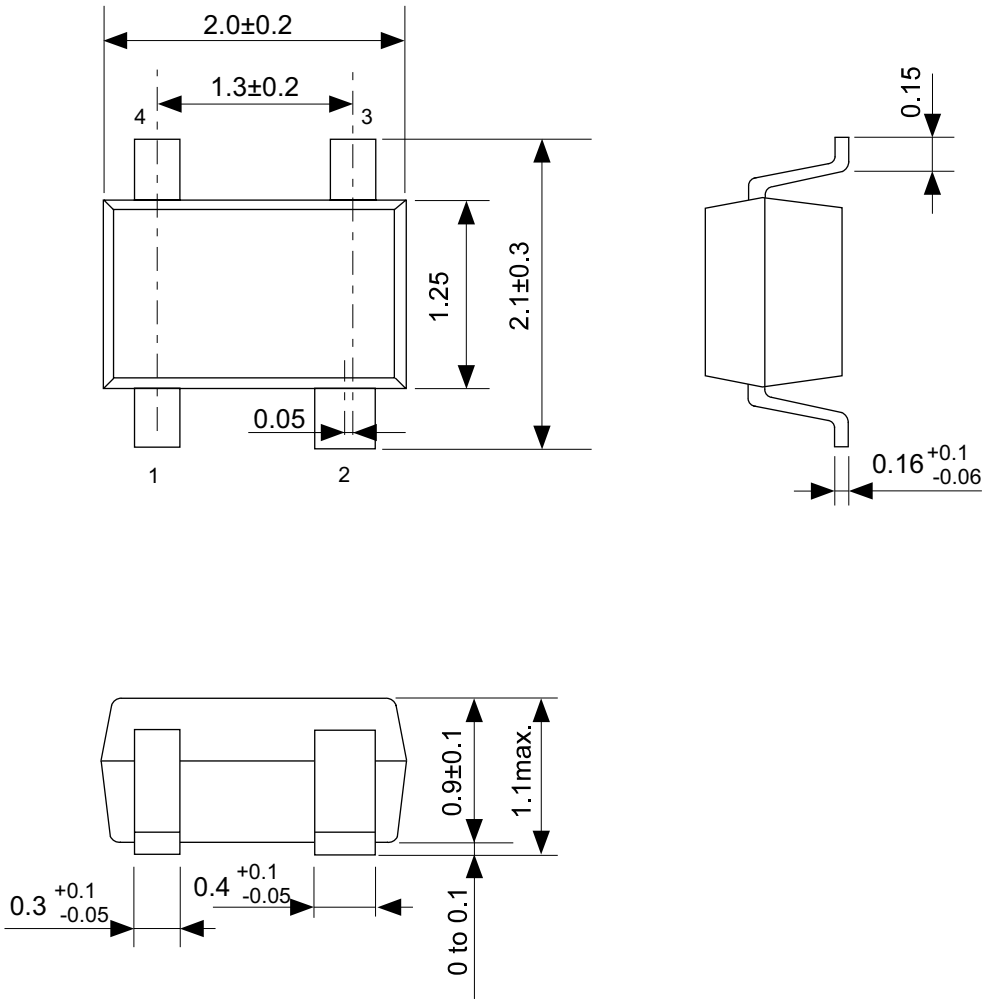


Enlarged drawing in the central part



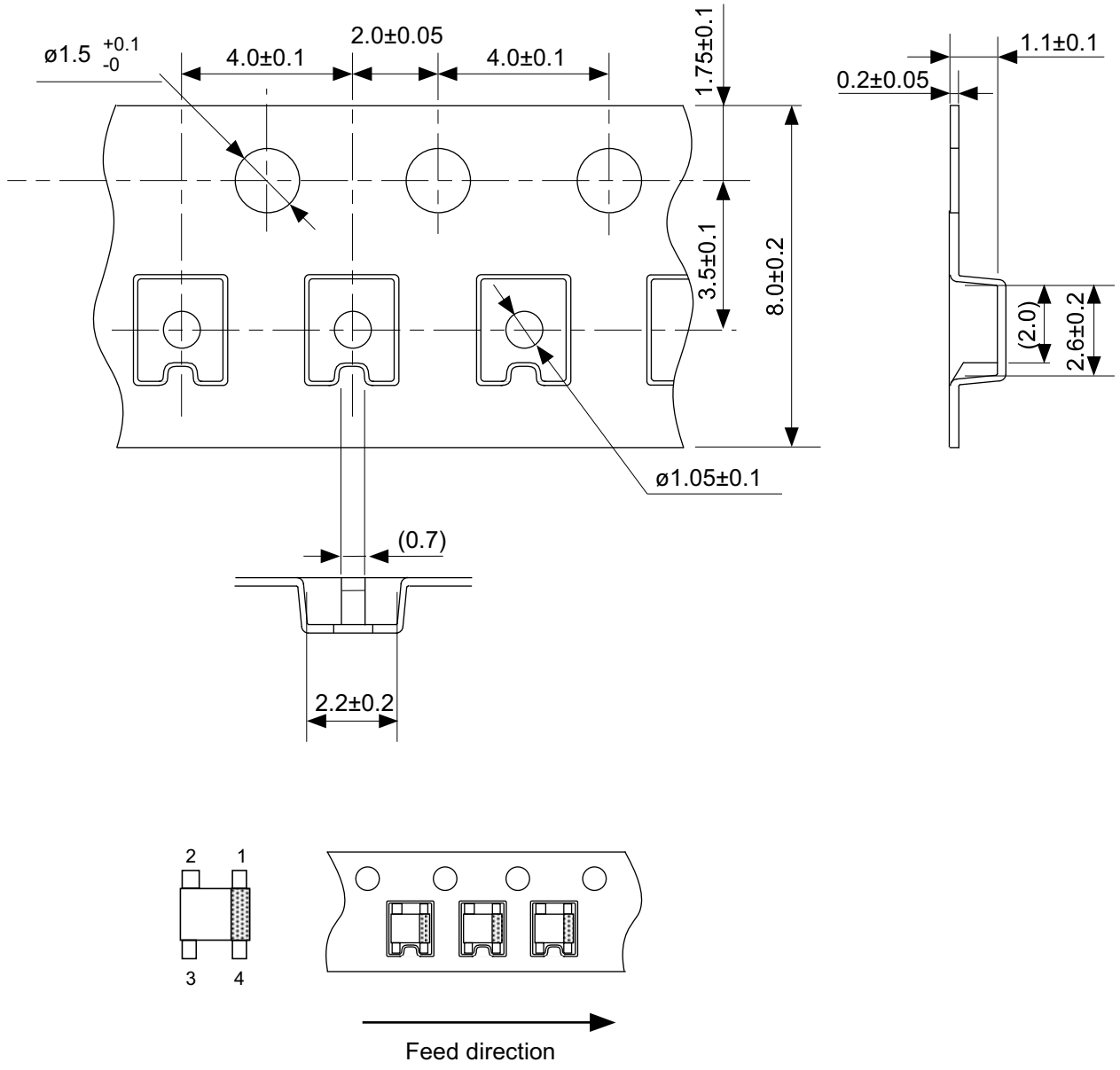
No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
SII Semiconductor Corporation			



No. NP004-A-P-SD-1.1

TITLE	SC82AB-A-PKG Dimensions
No.	NP004-A-P-SD-1.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	

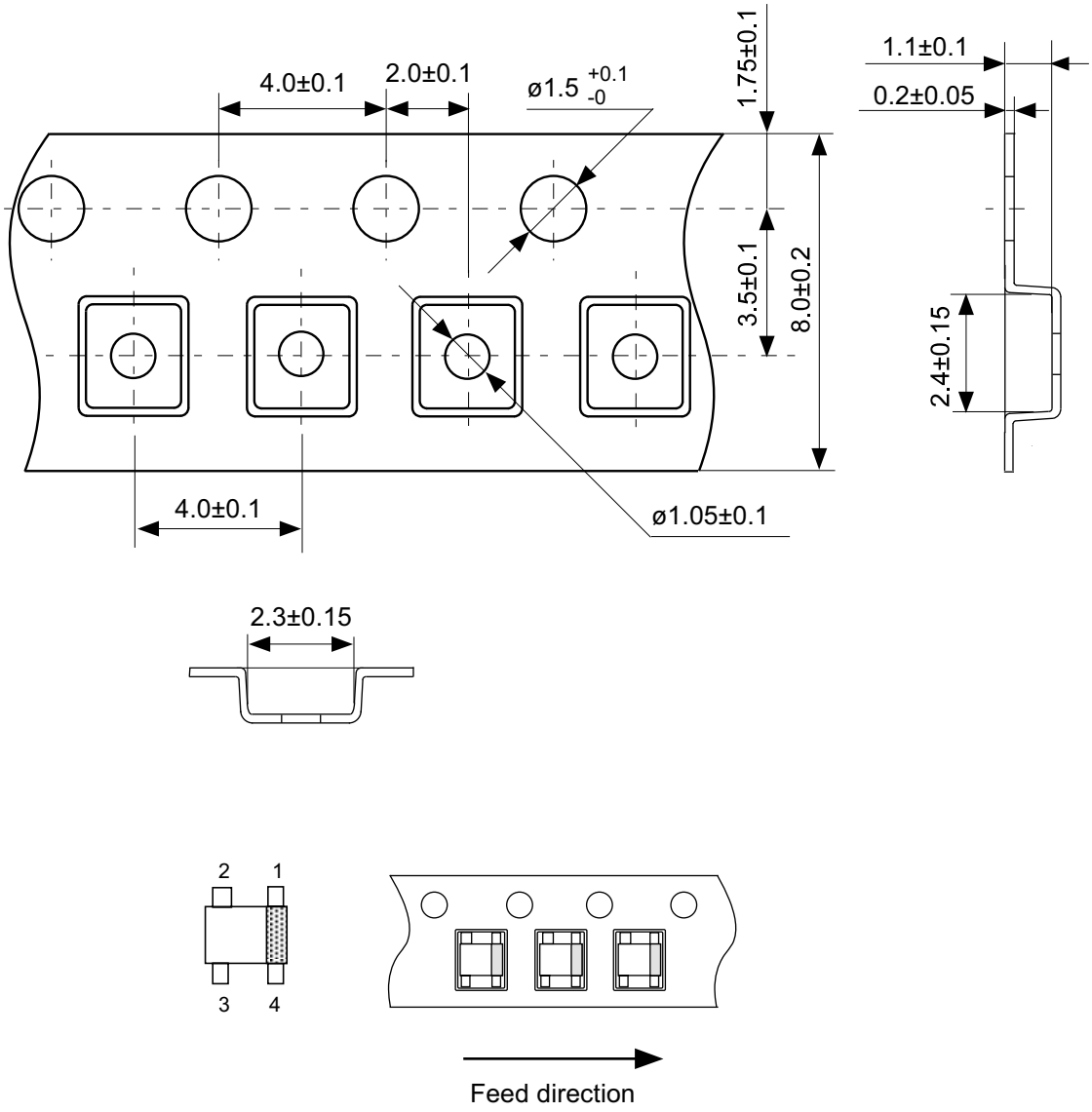


Feed direction

No. NP004-A-C-SD-3.0

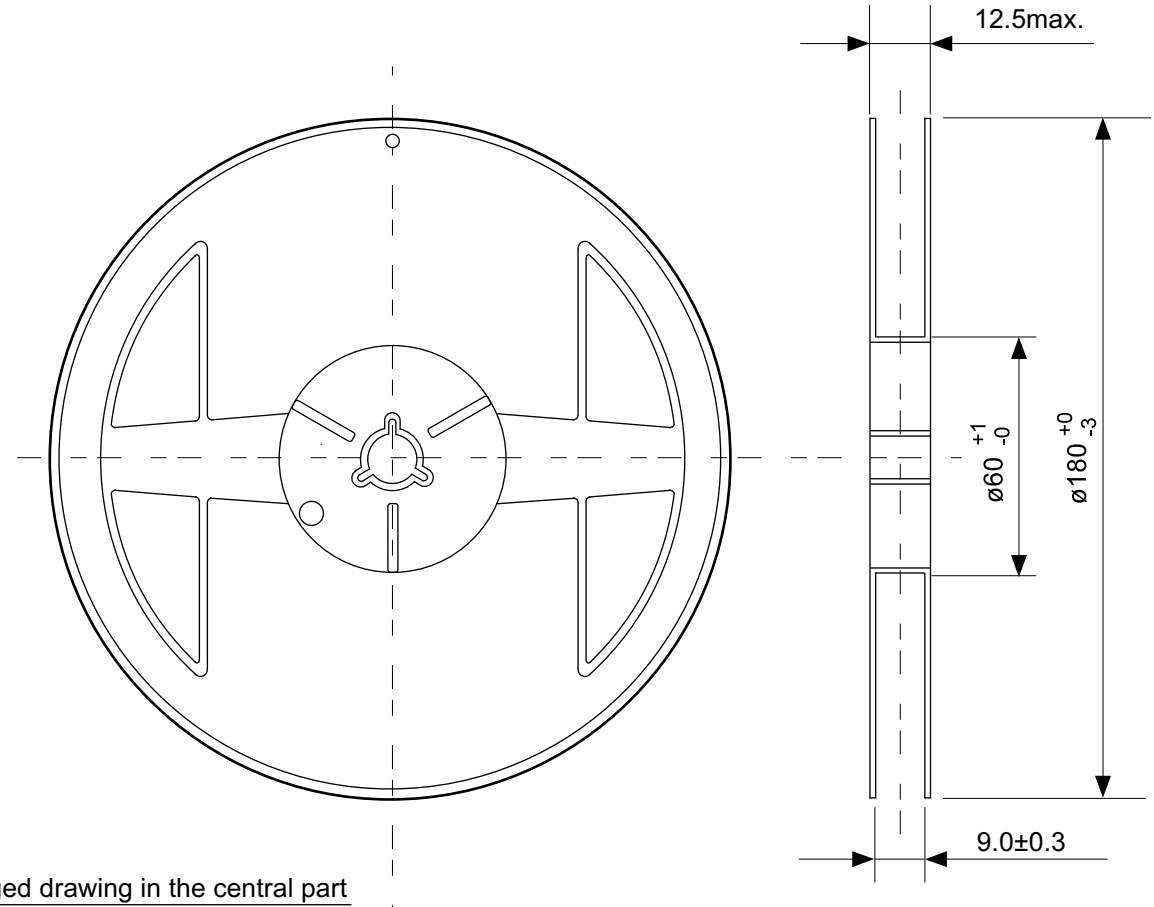
TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-SD-3.0
SCALE	
UNIT	mm

SII Semiconductor Corporation

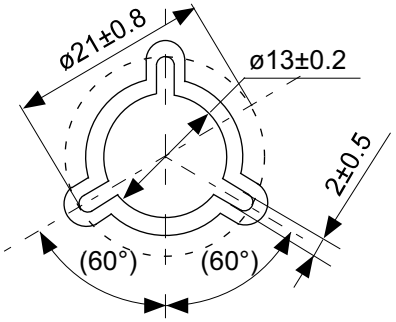


No. NP004-A-C-S1-2.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-S1-2.0
SCALE	
UNIT	mm
SII Semiconductor Corporation	

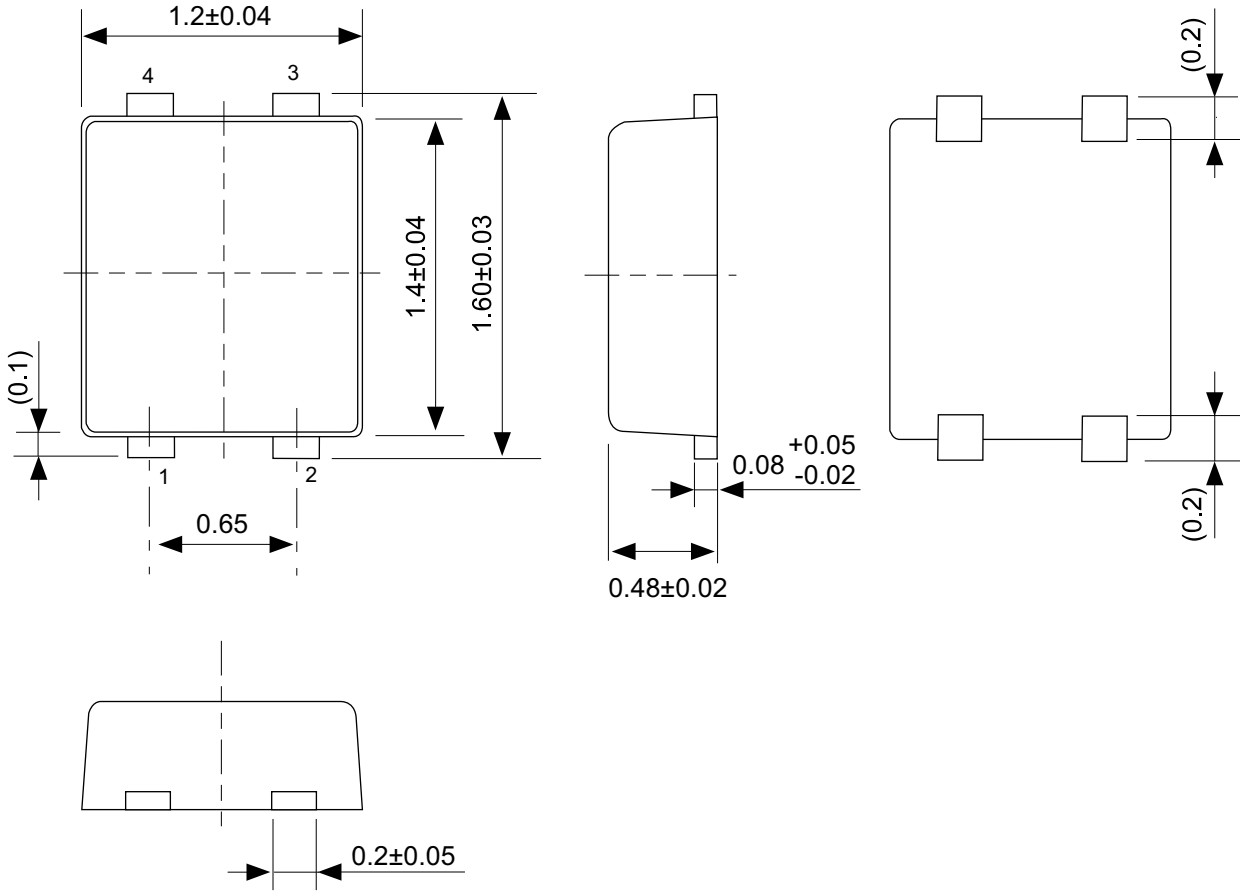


Enlarged drawing in the central part



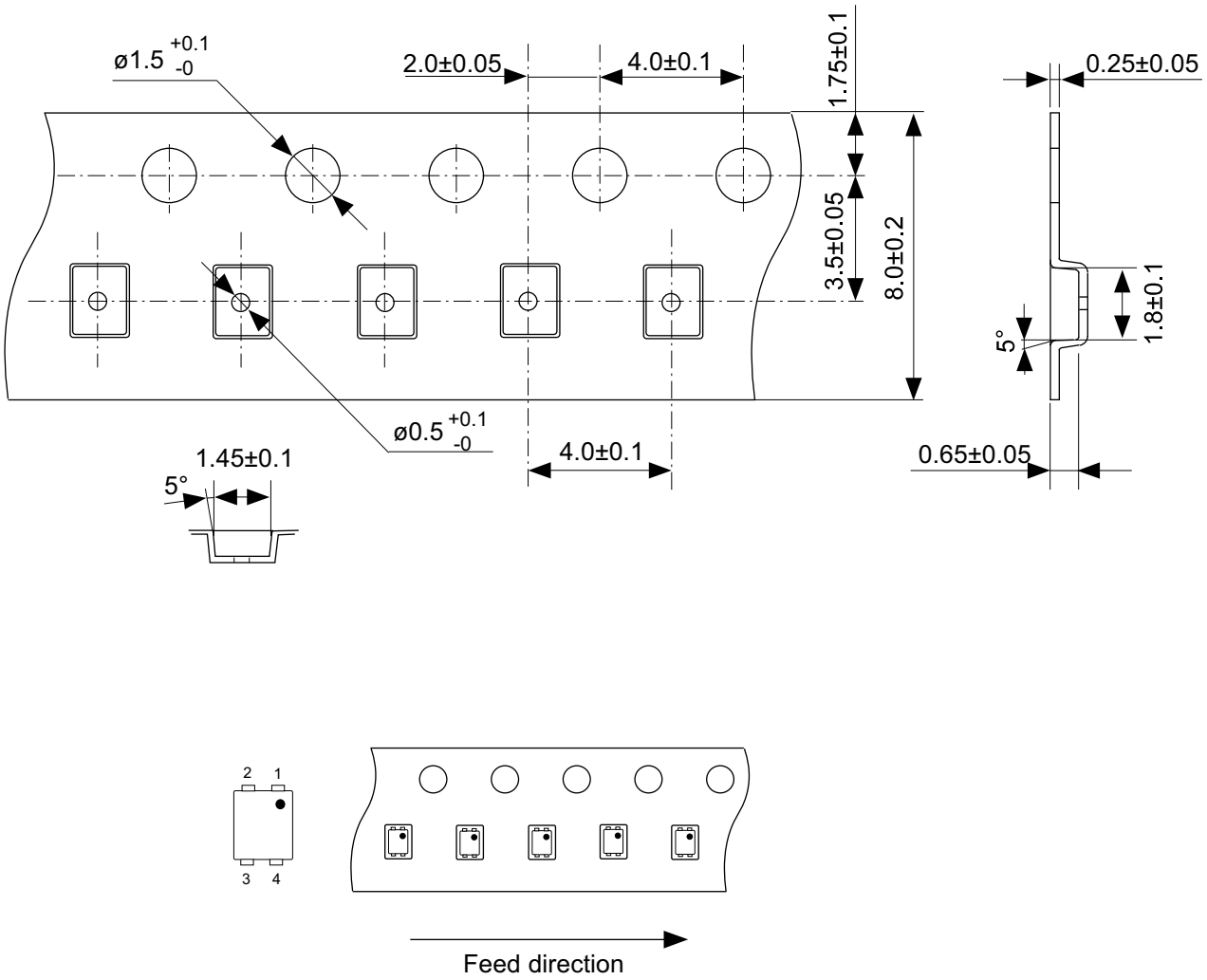
No. NP004-A-R-SD-1.1

TITLE	SC82AB-A-Reel		
No.	NP004-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
SII Semiconductor Corporation			



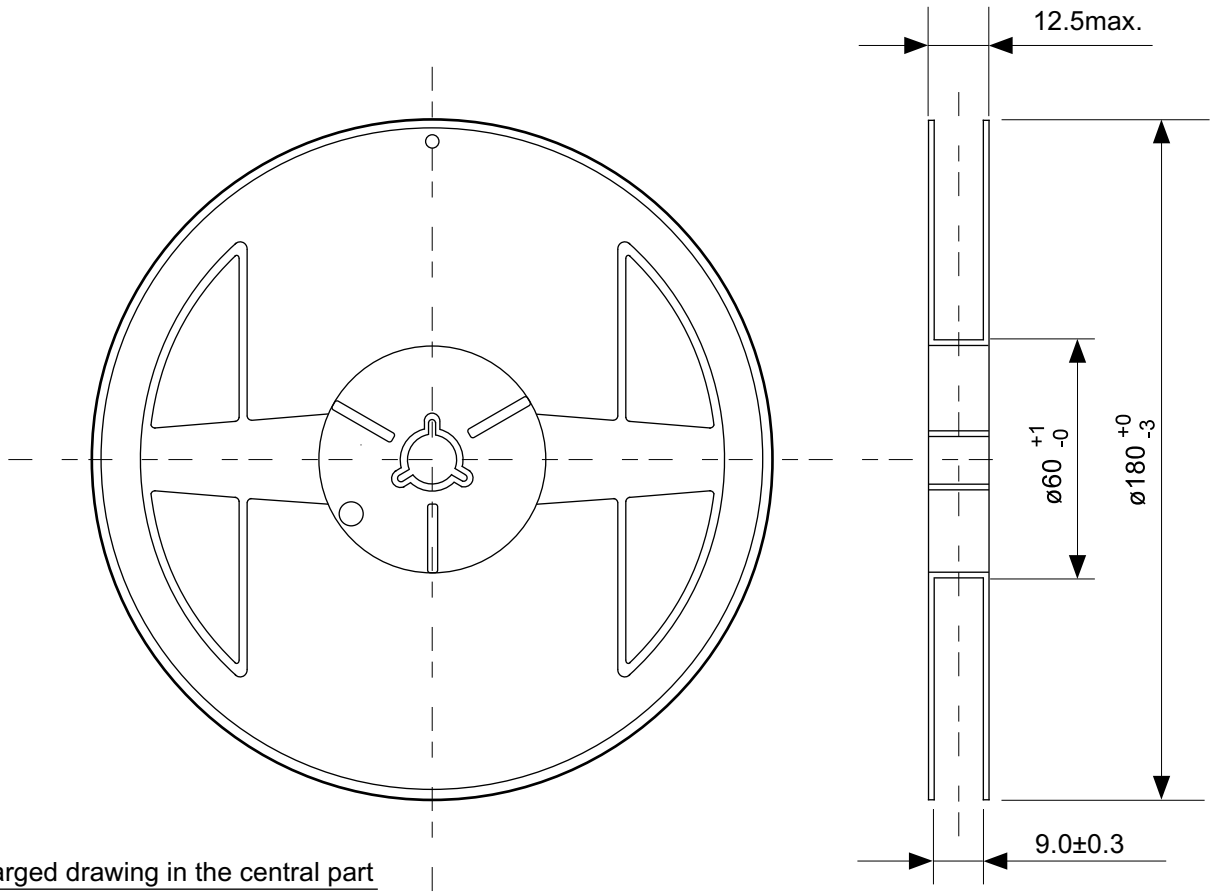
No. PF004-A-P-SD-4.0

TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-4.0
SCALE	
UNIT	mm
SII Semiconductor Corporation	

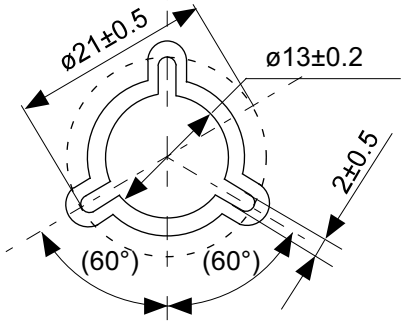


No. PF004-A-C-SD-1.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-1.0
SCALE	
UNIT	mm
SII Semiconductor Corporation	

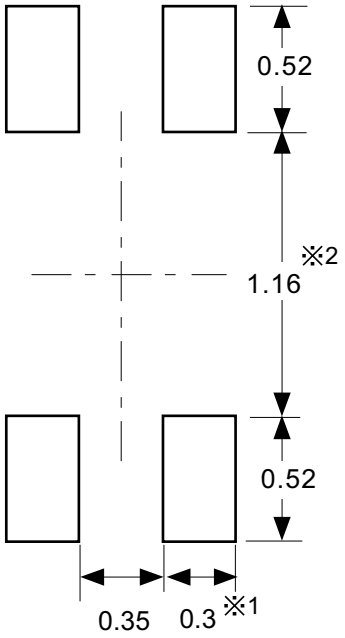


Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
SII Semiconductor Corporation			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	

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