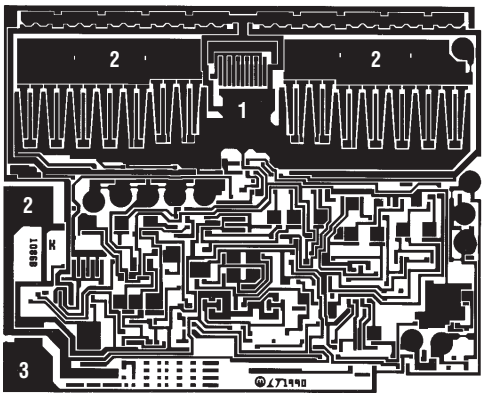
DICE SPECIFICATION

RH1086K/RH1086H 1.5A/0.5A Low Dropout Positive Regulators



103 × 85 mils

PAD FUNCTION

1. V_{IN}
2. V_{OUT}
3. ADJUST

Connect Backside Substrate to Pad #2

DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH1086H RH1086K	RH1086H DICE RH1086K DICE

DICE ELECTRICAL TEST LIMITS (Note 1)

PARAMETER	CONDITIONS	RH1086K (Note 6) MIN	RH1086K (Note 6) MAX	RH1086H (Note 6) MIN	RH1086H (Note 6) MAX	UNITS
Reference Voltage	I_{OUT} = 10mA, T_J = 25°C, ($V_{IN} - V_{OUT}$) = 3V 1.5V ≤ ($V_{IN} - V_{OUT}$) = 15V	1.238 1.225	1.262 1.270	 1.225	 1.270	V V
Line Regulation	I_{LOAD} = 10mA, 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 15V T_J = 25°C		0.2		0.2	%
Load Regulation	($V_{IN} - V_{OUT}$) = 3V, 10mA ≤ I_{OUT} ≤ 1.5A T_J = 25°C (0.5A for RH1086H) (Notes 1, 2, 5, 6)		0.3		0.3	%
Dropout Voltage ($V_{IN} - V_{OUT}$)	ΔV_{OUT}, ΔV_{REF} = 1%, I_{OUT} = 1.5A (0.5A for RH1086H) (Notes 3, 5, 6)		 1.5		1.25	V
Current Limit	($V_{IN} - V_{OUT}$) = 5V ($V_{IN} - V_{OUT}$) = 25V (Note 5)	1.5 0.050		0.5 0.020		A A
Mininum Load Current	($V_{IN} - V_{OUT}$) = 25V (Note 4)		10		10	mA
Ripple Rejection	f = 120Hz, C_{OUT} = 25µF Tantalum I_{OUT} = 1.5A, (I_{OUT} = 0.5A for RH1086H) C_{ADJ} = 25µF, ($V_{IN} - V_{OUT}$) = 3V (Note 5, 6)	60		60		dB
Adjust Pin Current	T_J = 25°C		120		120	µA
Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ 1.5A (0.5A for RH1086H) 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 15V (Note 5, 6)		5		5	µA

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

DICE ELECTRICAL TEST LIMITS

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing. Load regulation is measured at the output lead ≈ 1/8" from the package.

Note 2: Line and load regulation are guaranteed up to the maximum power dissipation of 15W for the RH1086K, 3W for the RH1086H. Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output voltage range. See Short Circuit Current Curve in the LT1086 Series standard data sheet for available output current.

Note 3: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage Curve in the LT1086 Series standard data sheet.

Note 4: Minimum load current is defined as the minimum output current required to maintain regulation. At 25V input/output differential the device is guaranteed to regulate if the output current is greater than 10mA.

Note 5: Guaranteed by design but not tested at wafer sort.

Note 6: For compliance with 883 revision C current density spec. RH1086K is derated to 1.0A max load operation.

Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much “softer” than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com

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