

2.0-18.0 GHz GaAs MMIC Low Noise Amplifier

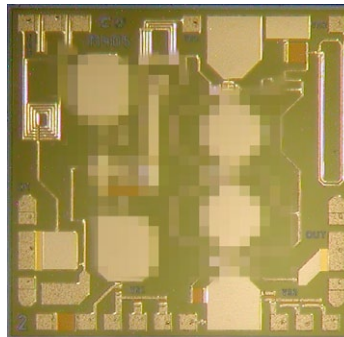
Features

- ✕ Self Bias Architecture
- ✕ 17.0 dB Small Signal Gain
- ✕ 3.5 dB Noise Figure
- ✕ +16.0 dBm P1dB Compression Point
- ✕ 100% Commercial-Level Visual Inspection Using Mil-Std-883 Method 2010

General Description

Mimix Broadband's two stage 2.0-18.0 GHz GaAs MMIC low noise amplifier has a small signal gain of 17.0 dB with a noise figure of 3.5 dB across the band. This MMIC uses Mimix Broadband's GaAs PHEMT device model technology, and is based upon optical lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for fiber optic, microwave radio, military, space, telecom infrastructure, test instrumentation and VSAT applications.

Chip Device Layout



Absolute Maximum Ratings

Supply Voltage (Vd)	+8.0 VDC
Supply Current (Id)	180 mA
Input Power (Pin)	+10 dBm
Storage Temperature (Tstg)	-65 to +165 °C
Operating Temperature (Ta)	-55 to +85 °C
Channel Temperature (Tch) ¹	+175 °C

(1) Channel temperature affects a device's MTTF. It is recommended to keep channel temperature as low as possible for maximum life.

Electrical Characteristics (Ambient Temperature T = 25 °C)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (f)	GHz	2.0	-	18.0
Input Return Loss (S11)	dB	6.0	9.0	-
Output Return Loss (S22)	dB	8.0	17.0	-
Small Signal Gain (S21)	dB	14.0	17.0	-
Gain Flatness ($\Delta S21$)	dB	-	+/-0.5	-
Reverse Isolation (S12)	dB	-	40.0	-
Noise Figure (NF)	dB	-	3.5	5.0
Output Power for 1 dB Compression (P1dB)	dBm	+13.0	+16.0	-
Output Second Order Intercept Point (OIP2)	dBm	-	+33.0	-
Output Third Order Intercept Point (OIP3)	dBm	-	+26.0	-
Drain Bias Voltage (Vd1,2)	VDC	-	+5.0	+7.0
Supply Current (Id) (Vd1,2=5.0V)	mA	90	100	120

100% on-wafer DC testing and 100% RF wafer qualification. Wafer qualification includes sample testing from each quadrant with an 80% pass rate required.

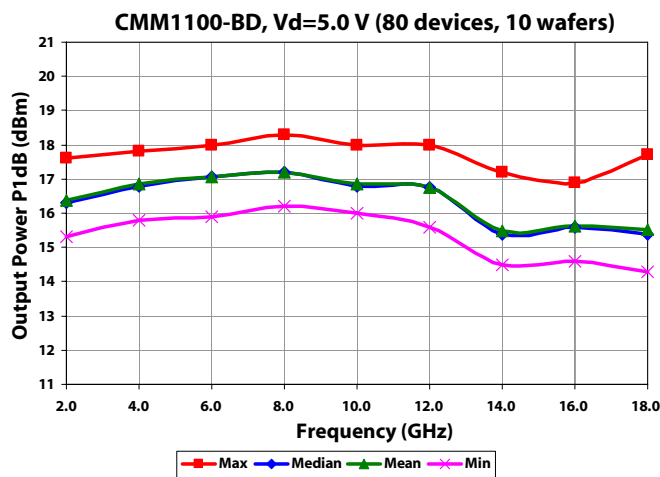
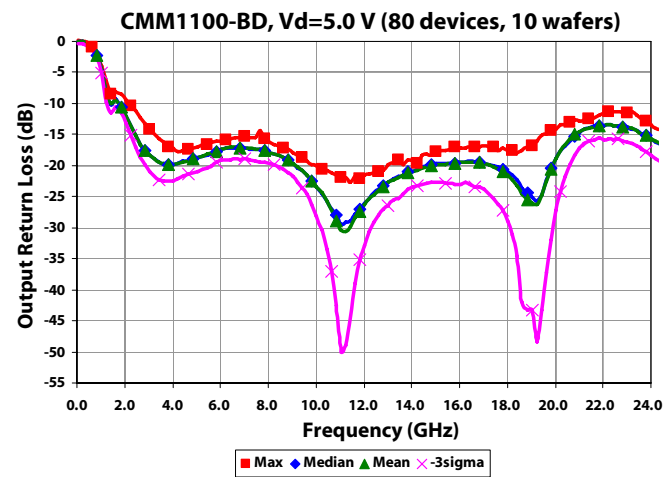
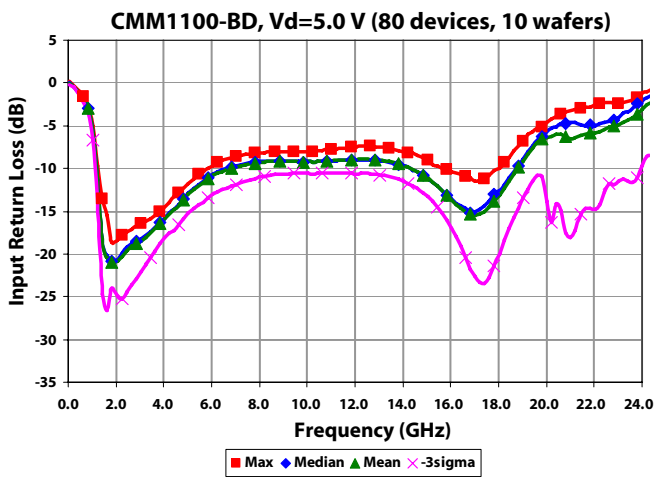
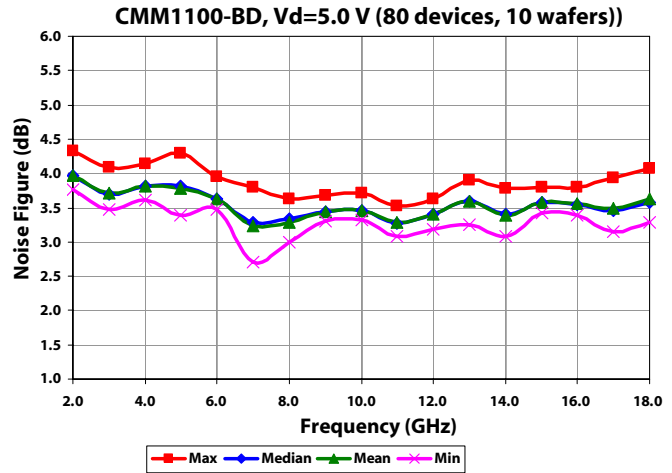
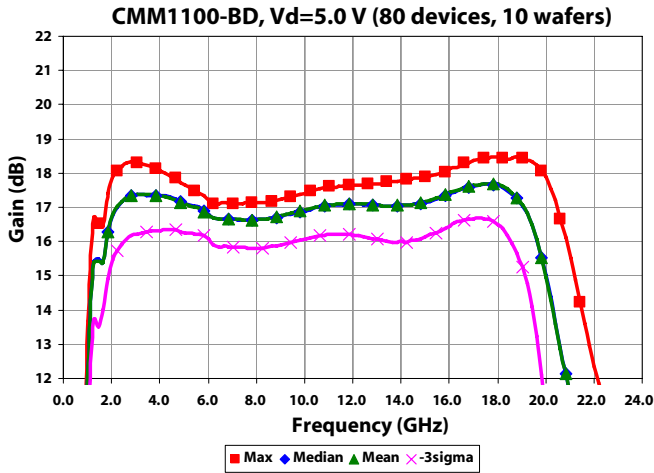
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Low Noise Amplifier Measurements (On Wafer)



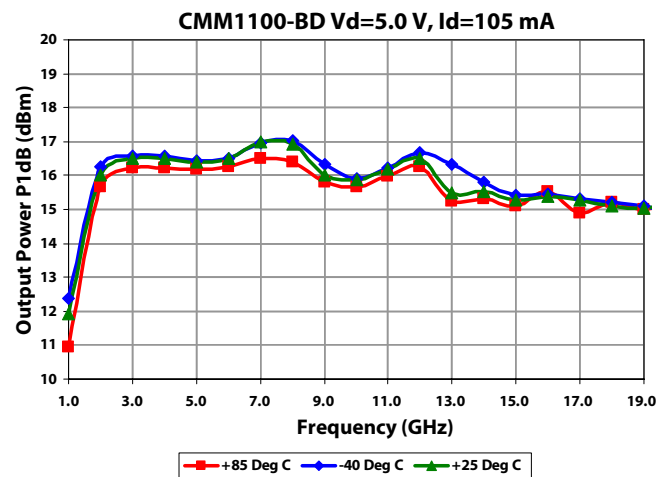
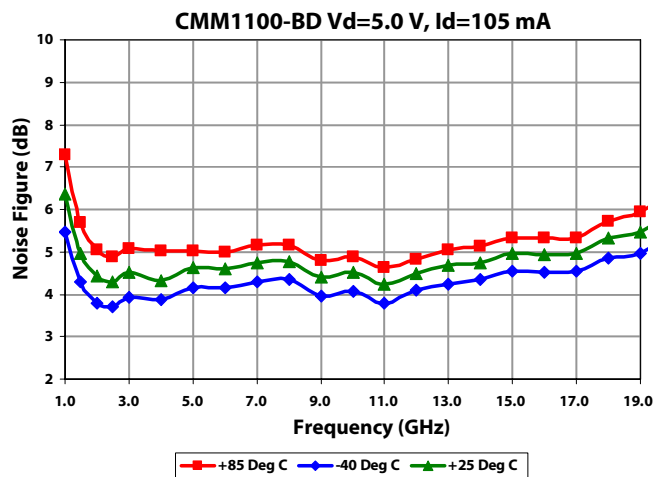
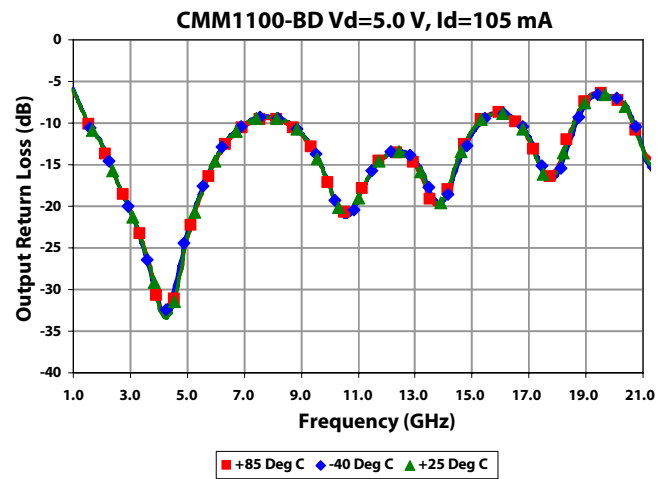
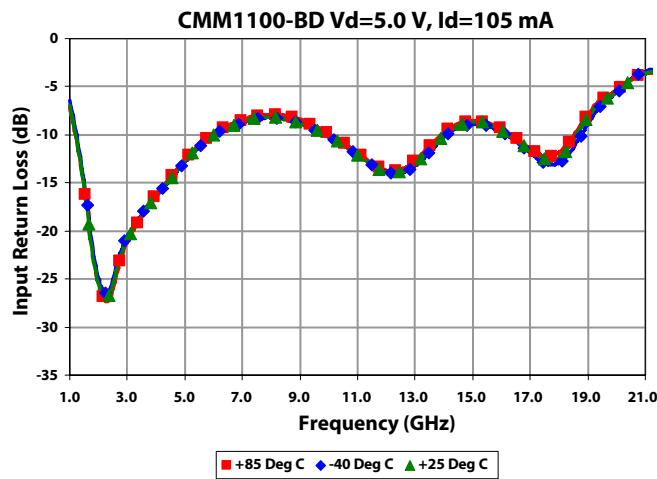
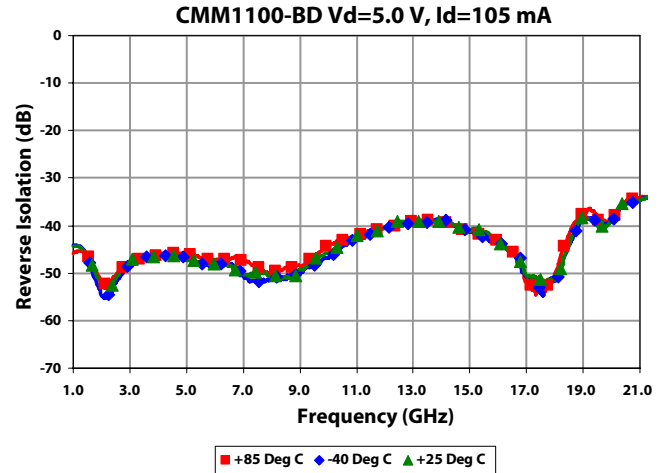
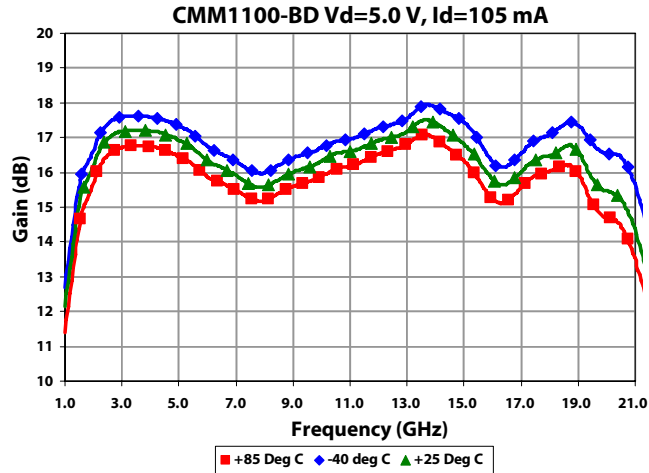
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Low Noise Amplifier Measurements (Test Fixture)



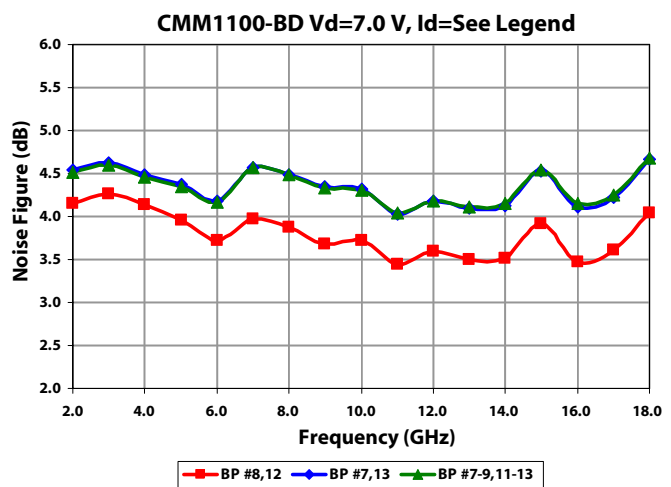
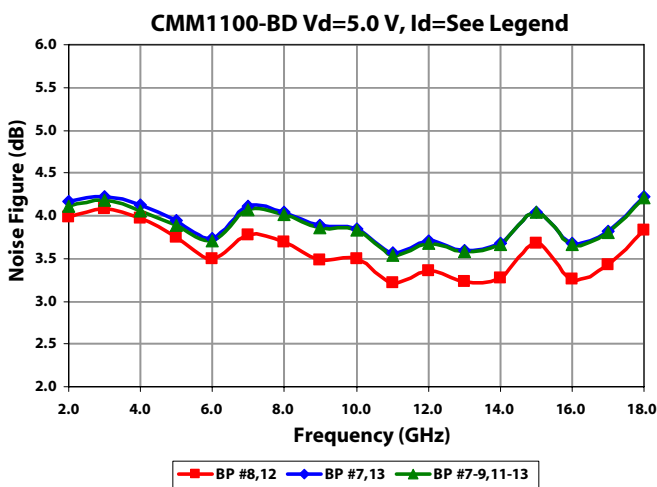
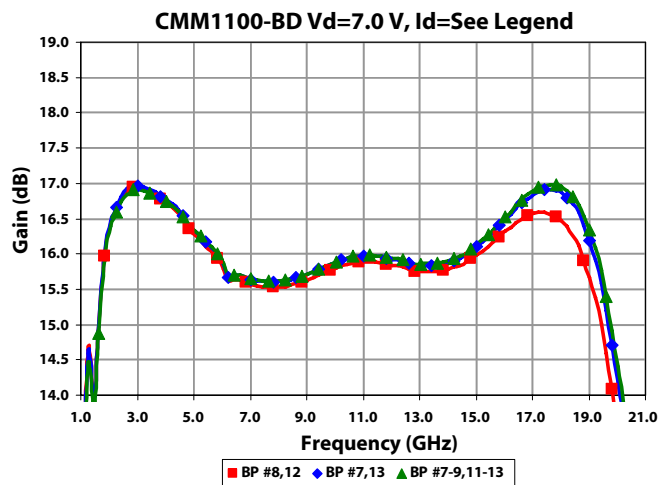
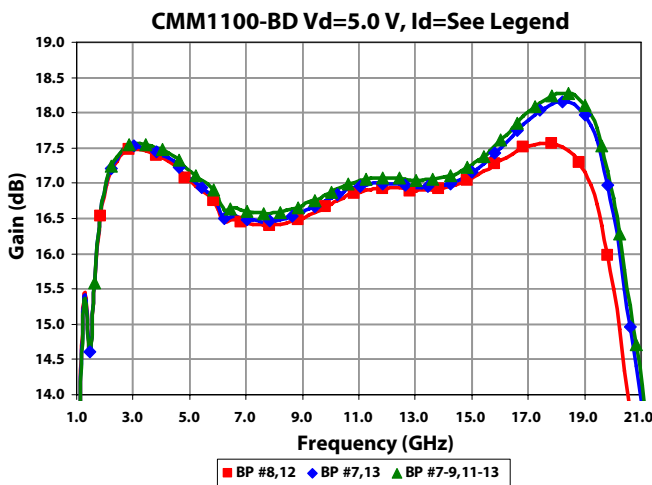
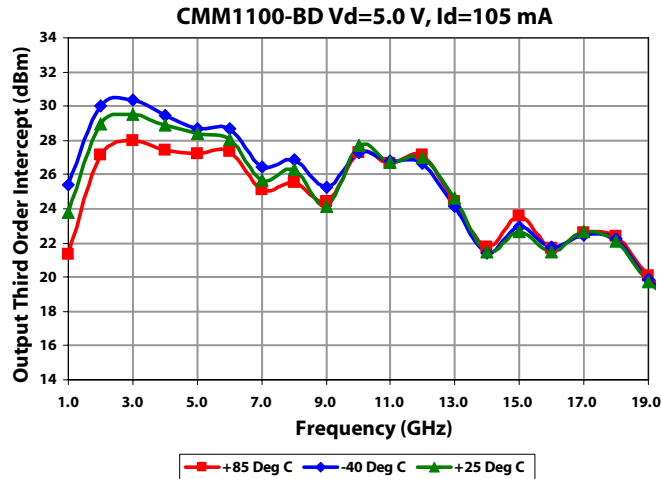
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Low Noise Amplifier Measurements (Test Fixture) (cont.)



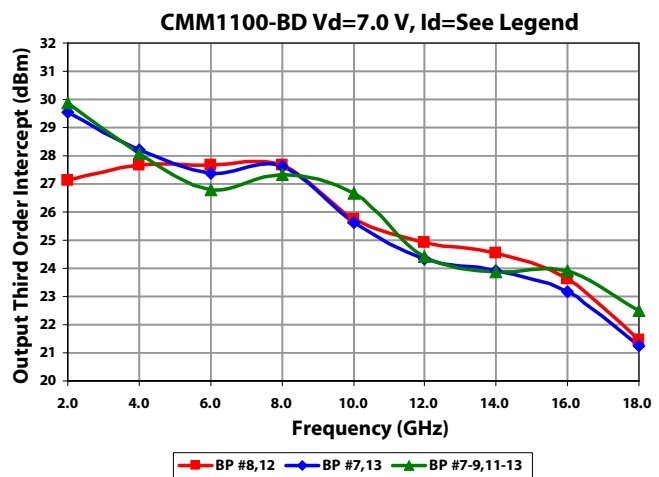
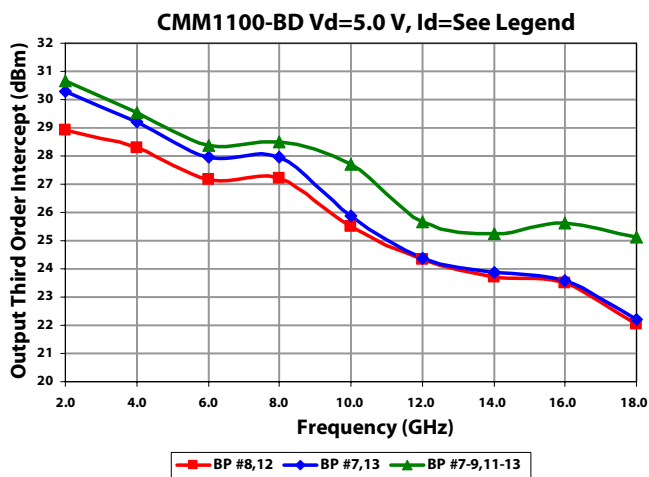
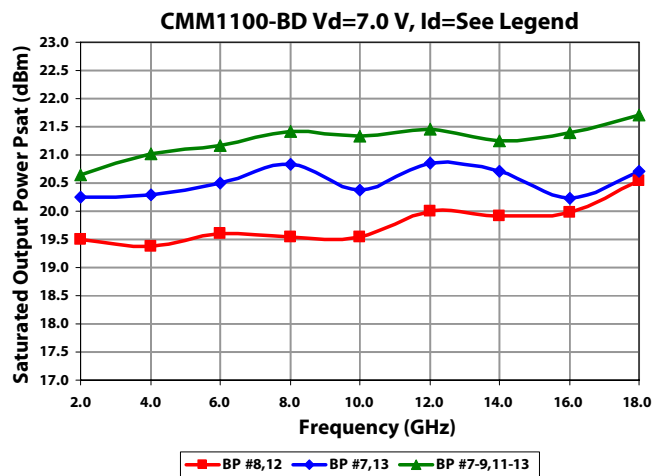
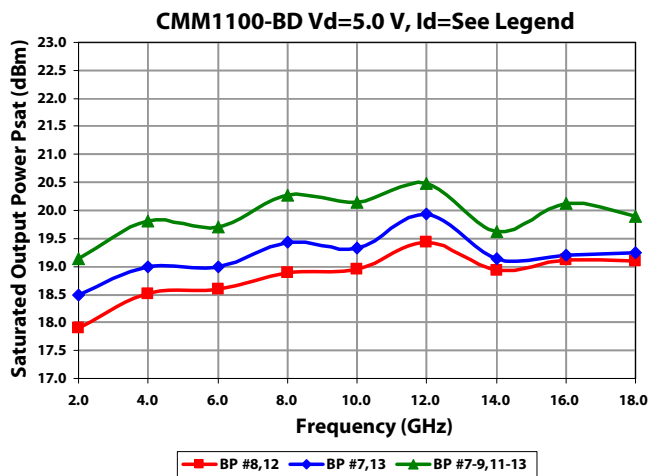
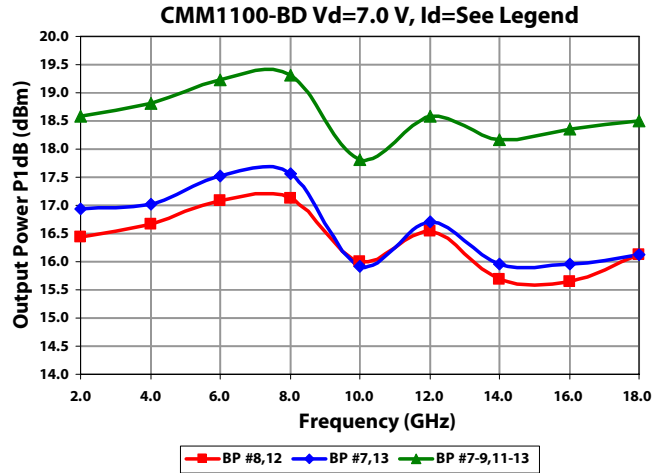
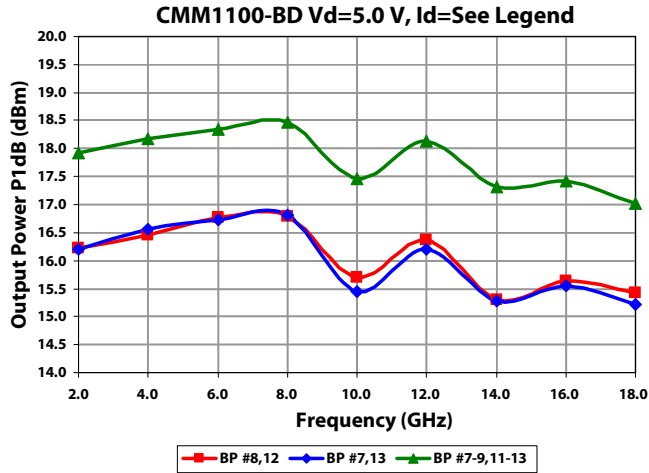
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Low Noise Amplifier Measurements (Test Fixture) (cont.)



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S-Parameters

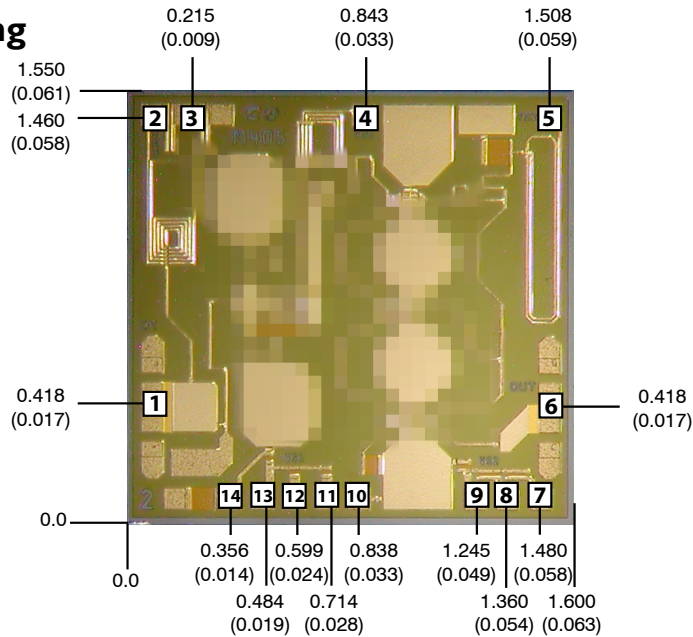
Typical S-Parameter Data for CMM1100

Vd=5.0 V Id=106 mA

Frequency (GHz)	S11 (Mag)	S11 (Ang)	S21 (Mag)	S21 (Ang)	S12 (Mag)	S12 (Ang)	S22 (Mag)	S22 (Ang)
1.0	0.564	113.40	3.998	-135.42	0.0072	-64.86	0.608	-147.64
2.0	0.073	-51.85	7.217	61.62	0.0009	113.67	0.245	169.55
3.0	0.108	-112.43	7.697	-10.40	0.0027	95.10	0.105	168.57
4.0	0.156	-109.03	7.579	-60.06	0.0036	60.15	0.092	-167.04
5.0	0.231	-111.81	7.270	-100.74	0.0042	30.44	0.117	-163.10
6.0	0.300	-123.14	6.945	-136.61	0.0048	10.91	0.139	-169.57
7.0	0.341	-135.59	6.755	-167.71	0.0056	-12.13	0.143	173.76
8.0	0.360	-145.49	6.714	161.60	0.0060	-40.52	0.130	158.50
9.0	0.358	-153.82	6.795	131.18	0.0063	-56.60	0.103	139.11
10.0	0.355	-159.38	6.950	100.24	0.0067	-83.85	0.060	116.93
11.0	0.356	-164.32	7.077	68.16	0.0075	-99.83	0.015	53.27
12.0	0.365	-171.49	7.088	35.62	0.0081	-123.98	0.039	-67.58
13.0	0.363	177.34	7.023	3.31	0.0084	-136.58	0.068	-94.03
14.0	0.335	161.48	6.990	-28.77	0.0091	-158.13	0.089	-110.68
15.0	0.285	139.48	7.064	-61.34	0.0097	-177.70	0.101	-119.80
16.0	0.216	106.64	7.277	-96.06	0.0111	157.68	0.104	-129.14
17.0	0.179	53.21	7.468	-133.62	0.0123	134.05	0.108	-140.57
18.0	0.231	1.35	7.529	-174.55	0.0138	106.85	0.091	-158.99
19.0	0.355	-27.53	7.272	139.73	0.0140	76.50	0.041	142.10
20.0	0.536	-50.52	6.255	89.50	0.0133	25.64	0.091	-7.89
21.0	0.672	-74.63	4.519	41.30	0.0105	-3.89	0.184	-57.94
22.0	0.724	-93.09	3.071	1.39	0.0087	-37.62	0.213	-89.57
23.0	0.744	-104.71	2.382	-39.37	0.0075	-82.40	0.214	-112.14
24.0	0.817	-115.54	1.594	-90.33	0.0084	-111.46	0.165	-126.73
25.0	0.833	-134.08	0.779	-139.00	0.0101	-159.83	0.130	-128.87
26.0	0.642	-152.52	0.290	-165.96	0.0074	175.00	0.104	-123.13
27.0	0.339	-134.36	0.174	-163.07	0.0062	-166.95	0.111	-111.81
28.0	0.588	-114.26	0.122	166.67	0.0076	111.86	0.101	-106.87
29.0	0.701	-124.81	0.067	148.80	0.0070	141.10	0.097	-98.09
30.0	0.751	-134.74	0.036	142.87	0.0084	114.00	0.105	-83.07

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Mechanical Drawing

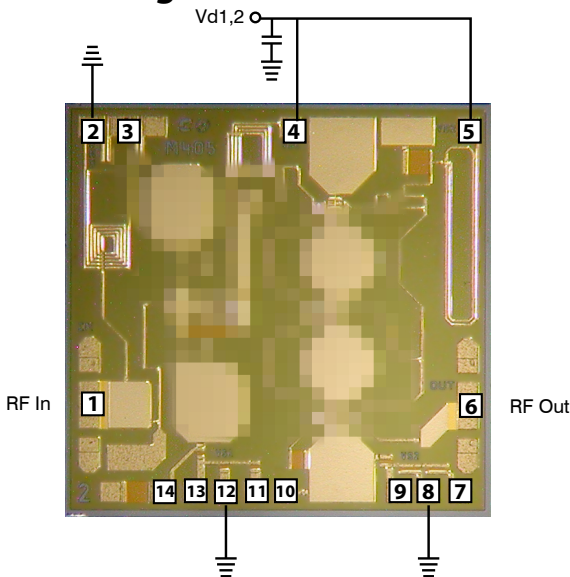


(Note: Engineering designator is M425)

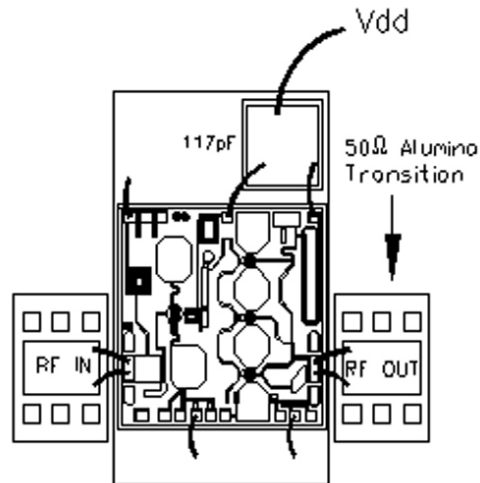
Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
 Thickness: 0.076 +/- 0.010 (0.003 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
 All DC Bond Pads are 0.080 x 0.080 (0.003 x 0.003). All RF Bond Pads are 0.180 x 0.080 (0.007 x 0.003).
 Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
 Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 1.538 mg

Bond Pad #1 (RF In)	Bond Pad #4 (Vd1)	Bond Pad #7 (Rs2-9.0Ω)	Bond Pad #11 (Rs1-29.0Ω)
Bond Pad #2 (Vg1a)	Bond Pad #5 (Vd2)	Bond Pad #8 (Rs2-12.5Ω)	Bond Pad #12 (Rs1-29.0Ω)
Bond Pad #3 (Vg1b)	Bond Pad #6 (RF Out)	Bond Pad #9 (Rs2-12.5Ω)	Bond Pad #13 (Rs1-16.6Ω)
		Bond Pad #10 (Rs2-Off Chip)	Bond Pad #14 (Rs1-Off Chip)

Bias Arrangement



Bypass Capacitors - See App Note [2]



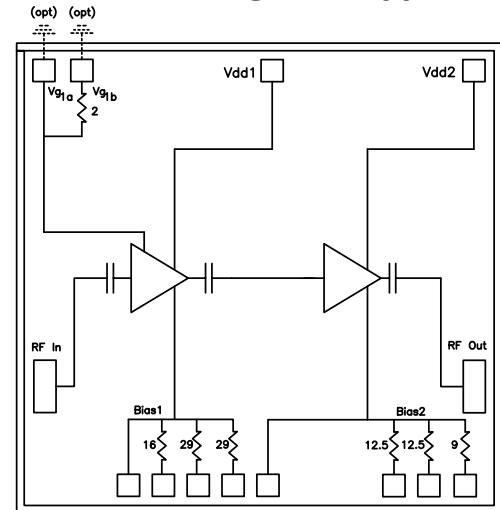
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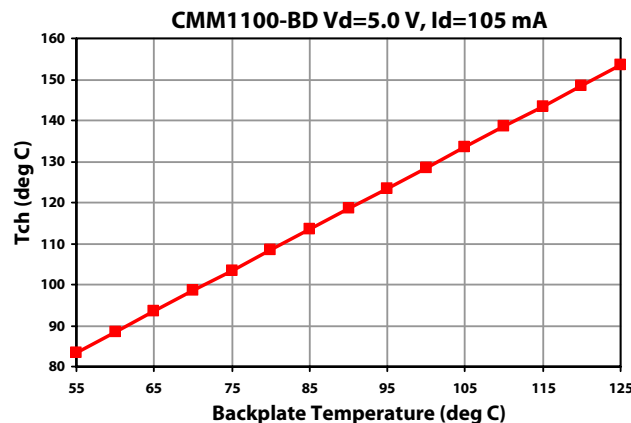
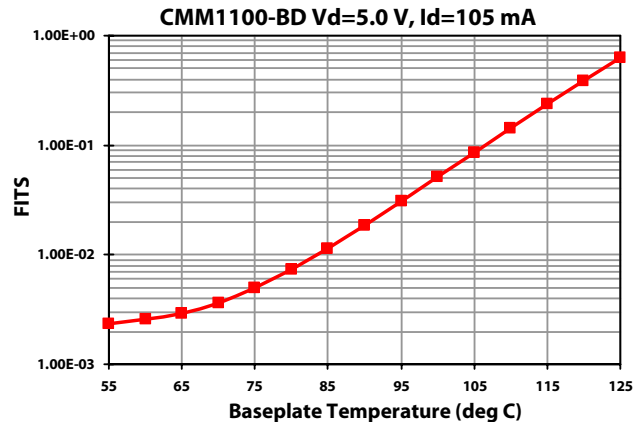
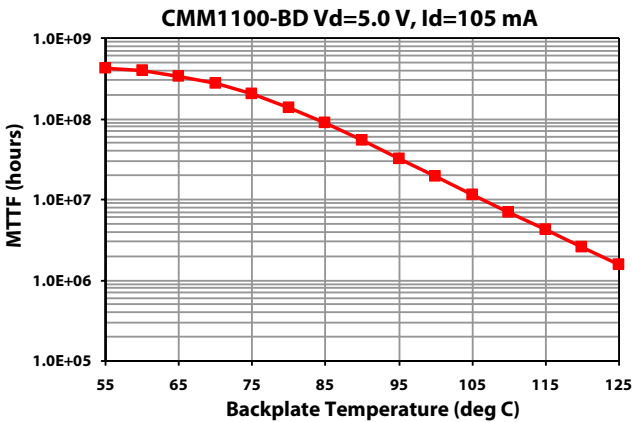
App Note [1] Biasing - As shown in the bonding diagram, this device operates using a self-biased architecture and only requires one drain bias. Bias is nominally $V_{d1}=V_{d2}=5V$, $I_{(total)}=105mA$. Additionally there are six total source resistors on chip. The three resistors on the input stage are 16.6, 29.0 and 29.0 Ohms. The three resistors on the output stage are 12.5, 12.5 and 9.0 Ohms. One of these must be bonded to ground for each amplifier stage to achieve performance as shown. Bonding to one of the other resistors or any or all in parallel may allow additional performance adjustment. Lastly for additional stability pad #3 can be grounded instead of bond pad #2.

App Note [2] Bias Arrangement - Each DC pad (Vd) needs to have DC bypass capacitance (~100-200 pF) as close to the device as possible. Additional DC bypass capacitance (~0.01 uF) is also recommended.



MTTF Graphs

These numbers were calculated based upon accelerated life test information received from the fabricating foundry and extensive thermal modeling/finite element analysis done at Mimix Broadband. The values shown here are only to be used as a guideline against the end application requirements and only represent reliability information under one bias condition. Ultimately bias conditions and resulting power dissipation along with the practical aspects, i.e. thermal material stack-up, attach method of die placement are the key parts in determining overall reliability for a specific application, see previous pages. If the data shown below does not meet your reliability requirements or if the bias conditions are not within your operating limits please contact technical sales for additional information.



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Handling and Assembly Information

CAUTION! - Mimix Broadband MMIC Products contain gallium arsenide (GaAs) which can be hazardous to the human body and the environment. For safety, observe the following procedures:

- Do not ingest.
- Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by-products are dangerous to the human body if inhaled, ingested, or swallowed.
- Observe government laws and company regulations when discarding this product. This product must be discarded in accordance with methods specified by applicable hazardous waste procedures.

Life Support Policy - Mimix Broadband's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President and General Counsel of Mimix Broadband. As used herein: (1) Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user. (2) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ESD - Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded antistatic workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

Die Attachment - GaAs Products from Mimix Broadband are 0.076 mm (0.003") thick and have vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK or DM6030HK-Pt cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the Mimix "Epoxy Specifications for Bare Die" application note. If eutectic mounting is preferred, then a fluxless gold-tin (AuSn) preform, approximately 0.001² thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280° C (Note: Gold Germanium should be avoided). The work station temperature should be 310°C +/- 10°C. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding - Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminum wire should be avoided. Thermo-compression bonding is recommended though thermosonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonics are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.

Part Number for Ordering

CMM1100-BD-000W

PB-CMM1100-BD-0000

Description

RoHS compliant die packed in waffle trays

CMM1100-BD evaluation module



Caution: ESD Sensitive
Appropriate precautions in handling, packaging
and testing devices must be observed.

Proper ESD procedures should be followed when handling this device.