KS0040

65 COM / 132 SEG DRIVER & CONTROLLER FOR STN LCD

July. 1999.

Ver. 1.3

Prepared by: TAE-KWANG PARK Tae-Kwang, Park

parktk@samsung.co.kr

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KS0040 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Mar.1998
1.0	1) Changed function MPU interface pin & method are changed. DDRAM extended style is changed from horizontal to vertical. Reference voltage can be selected between internal V_{REF} and V_{DD} by REF pin. 2) Removed function Horizontal display shift function is removed. 3) Added function Double height character display function Center mode display function CGRAM full graphic function Line cursor function Vertical shift by character & first line fix and vertical shift function 4-bit interface mode 4) Changed pin name DT1 → DUMMY (Not connected) DT0 → REF (Reference voltage selection) DIRC → MI (6800- / 8080-series selection) DIRS → IF (8- / 4- bit interface length selection) RES → RESET (H/W reset) RW → RW_WR (Read / Write selection in 6800-series, Write enable in 8080-series) E → E_RD (Read / Write enable in 6800-series, Read enable in 8080-series) COMS1, 2 → COMI1, 2 (Common icon) SEGS1 ~ SEGS4 → SEGI1 ~ SEGI4 (Segment icons)	Jun.1998
1.1	1) Changed pin name VC5ON → TEST3 (Connect to VSS) TMPS0 → TEST4 (Connect to VSS) TMPS1 → TEST5 (Connect to VSS) 2) DC Spec changed IDD (3V): 150μA Max. → 180μA Max. IDD (5V): 250μA Max. → 280μA Max. 3) Power ON / OFF sequence is added.	Apr.1999
1.2	Page 1, 3, 23: CGROM character size is changed from 8,192 to 8,160. Page 63, 64: V_{REF} Item, REF = H → REF = L	Jun.1999
1.3	Page 6: X-coordinates are changed (Pad No.206 to 246)	Jul.1999

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INTRODUCTION

The KS0040 is a LCD driver and controller LSI for liquid crystal dot matrix character display systems. It can display 1 to 4 lines of 8 characters with 16 x 16 dots format. So it is suitable for display of Asian characters such as Korean, Chinese and Japanese. Also 8 x 16 dot half size alphanumeric characters can be displayed. And it can display 64 x 128 dots graphic LCD using internal CGRAM. Voltage converter (2 to 4 times), voltage regulator and voltage follower & bias circuits are built in the IC.

FEATURES

Driver Output Circuits

- Common outputs: 64 common + 1 common for icon
- Segment outputs: 128 segment + 4 segment for icon

Applicable Duty Ratios

Display size	Duty	Contents of outputs
1-line x 8 characters	1/17	1 x 8 characters + 16 x 4 vertical icons + 128 horizontal icons
2-line x 8 characters	1/33	2 x 8 characters + 32 x 4 vertical icons + 128 horizontal icons
3-line X 8 characters	1/49	3 x 8 characters + 48 x 4 vertical icons + 128 horizontal icons
4-line X 8 characters	1/65	4 x 8 characters + 64 x 4 vertical icons + 128 horizontal icons

On-chip Display Data RAM

- Full-size Character Generator ROM (FCGROM): 2,088,960 bits (8,160 characters x 16 x 16 dot)
- Half-size Character Generator ROM (HCGROM): 16,384 bits (128 characters x 8 x 16 dot)
- Character Generator RAM (CGRAM): 8,192 bits (32 characters x 16 x 16 dot)
- Display Data RAM (DDRAM): 1,024 bits (64 characters x 2 byte)
- Icon RAM (ICONRAM): 384 bits (128 horizontal icons + 64 x 4 vertical icons)

Microprocessor Interface

- 8- / 4- bit parallel interface mode: 6800-series, 8080-series
- Serial interface mode: 4 pins clock synchronous serial interface

Function Set

- Various instruction sets: vertical dot-by-dot display shift, double height character, power control, etc.
- COM / SEG bi-directional
- H/W reset

On-chip Analog Circuit

- Automatically adjusted oscillator circuit by duty set
- Electrical volume for contrast control (64 steps)
- Voltage converter (2 to 4 times) / voltage regulator (temperature coefficient = -0.05%/ ^{o}C) / voltage follower & bias circuit

Operating Voltage Range

- Supply voltage (V_{DD}): 2.4 to 5.5V
- LCD driving voltage (V_{LCD} = V0 - V_{SS}) = 13.0V

Low Power Consumption

- Sleep mode operation (V_{DD} = 3V: 5uA Max.)
- Normal mode operation (V_{DD} = 3V, V0 = 9V: 150uA Typ.)

Package Type

- Gold bumped chip or TCP

BLOCK DIAGRAM

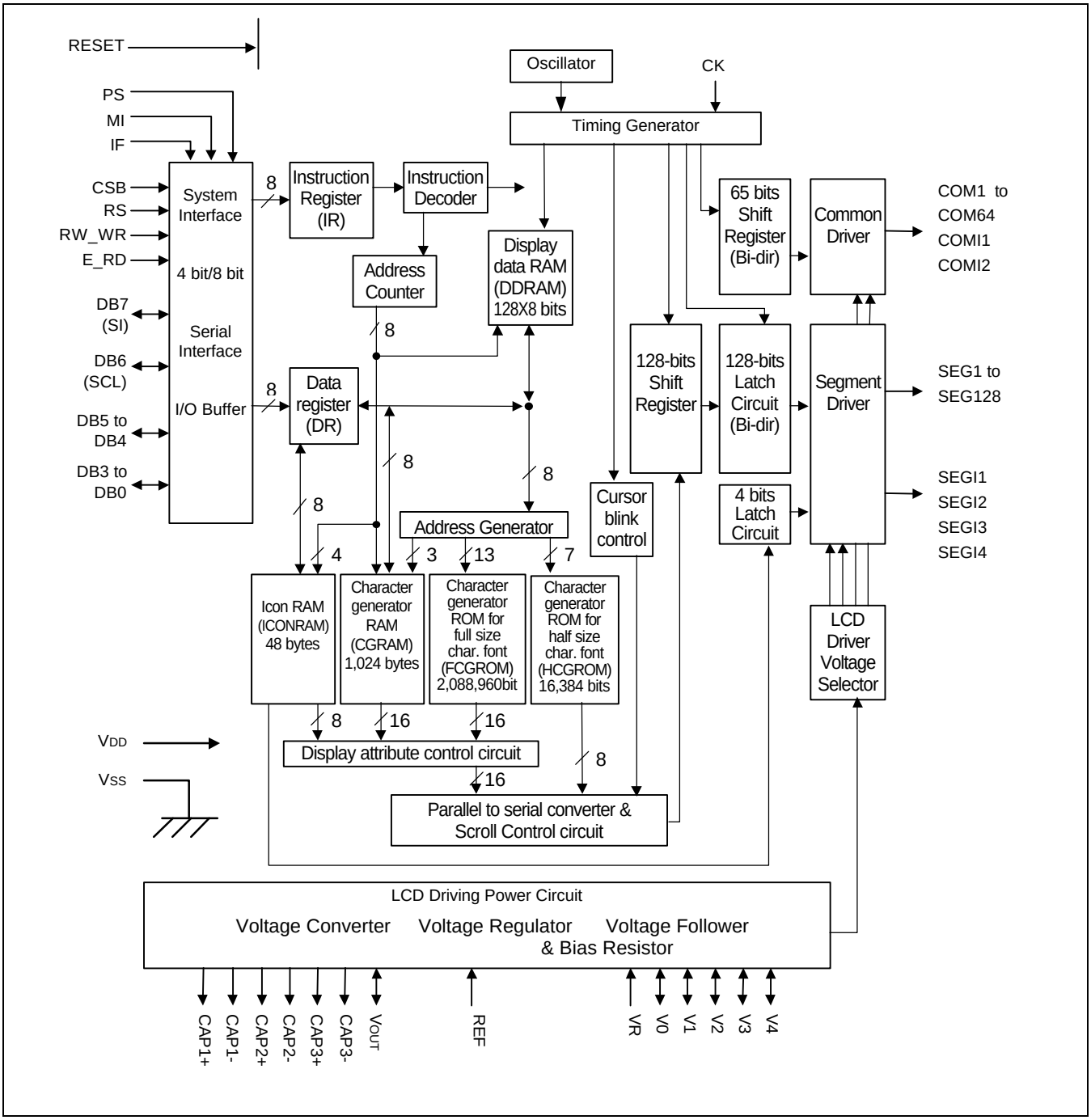


Figure 1. Block Diagram

PAD CONFIGURATION

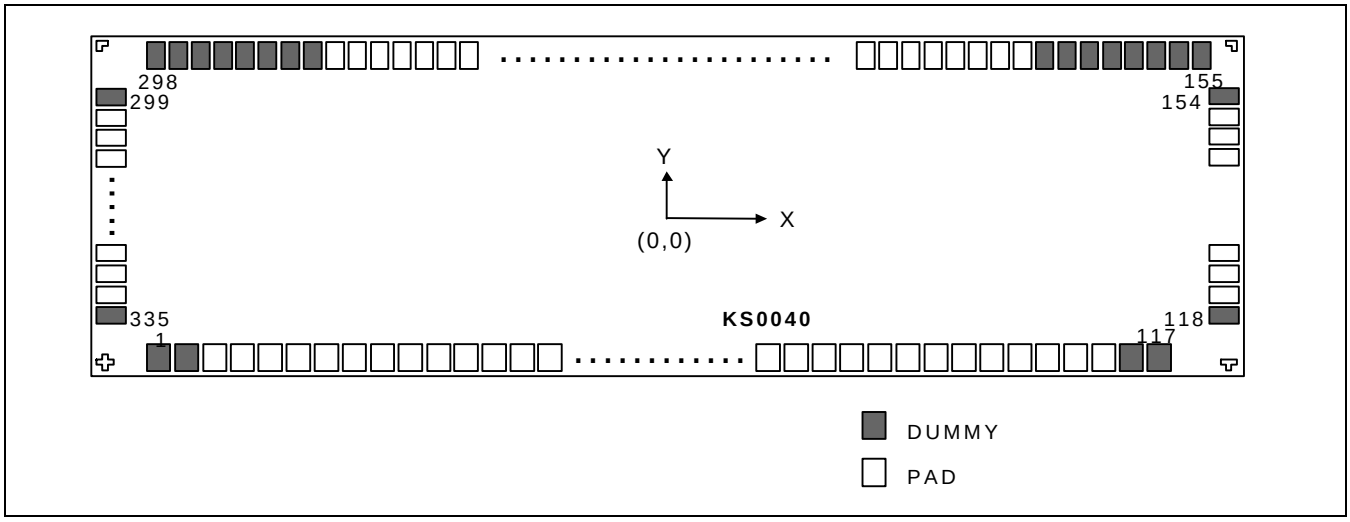
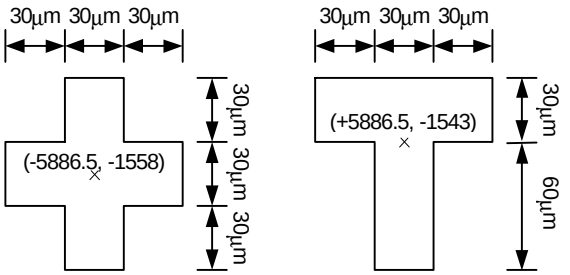


Figure 2. Pad Configuration

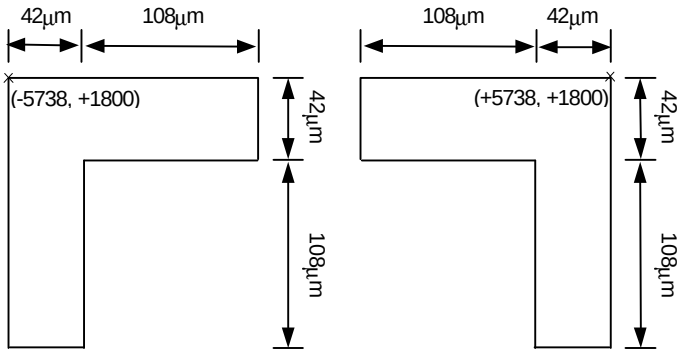
Table 1. KS0040 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	12160	3860	µm
Pad pitch	1 to 117	90		
	118 to 335	70		
Bumped pad size	1 to 117	56	114	
	118 to 154	108	50	
	155 to 298	50	108	
	229 to 335	108	50	
Bumped pad height	1 to 138	17 (Typ.)		

COG Align Key Coordinate



ILB Align Key Coordinate



SAMSUNG ELECTRONICS

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	DUMMY	-5220	-1806	42	VSS	-1530	-1806	83	CAP2-	2160	-1806
2	DUMMY	-5130	-1806	43	DUMMY	-1440	-1806	84	DUMMY	2250	-1806
3	VSS	-5040	-1806	44	VDD	-1350	-1806	85	DUMMY	2340	-1806
4	TEST1	-4950	-1806	45	VDD	-1260	-1806	86	VR	2430	-1806
5	VDD	-4860	-1806	46	VDD	-1170	-1806	87	VR	2520	-1806
6	DUMMY	-4770	-1806	47	VDD	-1080	-1806	88	VR	2610	-1806
7	VSS	-4680	-1806	48	VDD	-990	-1806	89	VR	2700	-1806
8	REF	-4590	-1806	49	VDD	-900	-1806	90	DUMMY	2790	-1806
9	VDD	-4500	-1806	50	VDD	-810	-1806	91	V0	2880	-1806
10	MI	-4410	-1806	51	VDD	-720	-1806	92	V0	2970	-1806
11	VSS	-4320	-1806	52	VDD	-630	-1806	93	V0	3060	-1806
12	IF	-4230	-1806	53	VDD	-540	-1806	94	V0	3150	-1806
13	VDD	-4140	-1806	54	DUMMY	-450	-1806	95	DUMMY	3240	-1806
14	PS	-4050	-1806	55	VOUT	-360	-1806	96	V1	3330	-1806
15	VSS	-3960	-1806	56	VOUT	-270	-1806	97	V1	3420	-1806
16	CSB	-3870	-1806	57	VOUT	-180	-1806	98	V2	3510	-1806
17	VDD	-3780	-1806	58	VOUT	-90	-1806	99	V2	3600	-1806
18	RESET	-3690	-1806	59	DUMMY	0	-1806	100	V3	3690	-1806
19	RS	-3600	-1806	60	CAP3+	90	-1806	101	V3	3780	-1806
20	RW_WR	-3510	-1806	61	CAP3+	180	-1806	102	V4	3870	-1806
21	E_RD	-3420	-1806	62	CAP3+	270	-1806	103	V4	3960	-1806
22	DB7	-3330	-1806	63	CAP3+	360	-1806	104	DUMMY	4050	-1806
23	DB6	-3240	-1806	64	CAP3-	450	-1806	105	VSS	4140	-1806
24	DB5	-3150	-1806	65	CAP3-	540	-1806	106	TEST3	4230	-1806
25	DB4	-3060	-1806	66	CAP3-	630	-1806	107	VDD	4320	-1806
26	DB3	-2970	-1806	67	CAP3-	720	-1806	108	TEST5	4410	-1806
27	DB2	-2880	-1806	68	CAP1+	810	-1806	109	VSS	4500	-1806
28	DB1	-2790	-1806	69	CAP1+	900	-1806	110	TEST4	4590	-1806
29	DB0	-2700	-1806	70	CAP1+	990	-1806	111	VDD	4680	-1806
30	DUMMY	-2610	-1806	71	CAP1+	1080	-1806	112	TEST2	4770	-1806
31	DUMMY	-2520	-1806	72	CAP1-	1170	-1806	113	VSS	4860	-1806
32	DUMMY	-2430	-1806	73	CAP1-	1260	-1806	114	CK	4950	-1806
33	VSS	-2340	-1806	74	CAP1-	1350	-1806	115	VDD	5040	-1806
34	VSS	-2250	-1806	75	CAP1-	1440	-1806	116	DUMMY	5130	-1806
35	VSS	-2160	-1806	76	CAP2+	1530	-1806	117	DUMMY	5220	-1806
36	VSS	-2070	-1806	77	CAP2+	1620	-1806	118	DUMMY	5920	-1326
37	VSS	-1980	-1806	78	CAP2+	1710	-1806	119	COMI1	5920	-1256
38	VSS	-1890	-1806	79	CAP2+	1800	-1806	120	COM1	5920	-1186
39	VSS	-1800	-1806	80	CAP2-	1890	-1806	121	COM2	5920	-1116
40	VSS	-1710	-1806	81	CAP2-	1980	-1806	122	COM3	5920	-1046
41	VSS	-1620-	-1806	82	CAP2-	2070	-1806	123	COM4	5920	-976

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
124	COM5	5920	-906	165	SEG3	4305	1770	206	SEG44	1435	1770
125	COM6	5920	-836	166	SEG4	4235	1770	207	SEG45	1365	1770
126	COM7	5920	-766	167	SEG5	4165	1770	208	SEG46	1295	1770
127	COM8	5920	-696	168	SEG6	4095	1770	209	SEG47	1225	1770
128	COM17	5920	-626	169	SEG7	4025	1770	210	SEG48	1155	1770
129	COM18	5920	-556	170	SEG8	3955	1770	211	SEG49	1085	1770
130	COM19	5920	-486	171	SEG9	3885	1770	212	SEG50	1015	1770
131	COM20	5920	-416	172	SEG10	3815	1770	213	SEG51	945	1770
132	COM21	5920	-346	173	SEG11	3745	1770	214	SEG52	875	1770
133	COM22	5920	-276	174	SEG12	3675	1770	215	SEG53	805	1770
134	COM23	5920	-206	175	SEG13	3605	1770	216	SEG54	735	1770
135	COM24	5920	-136	176	SEG14	3535	1770	217	SEG55	665	1770
136	COM33	5920	-66	177	SEG15	3465	1770	218	SEG56	595	1770
137	COM34	5920	4	178	SEG16	3395	1770	219	SEG57	525	1770
138	COM35	5920	74	179	SEG17	3325	1770	220	SEG58	455	1770
139	COM36	5920	144	180	SEG18	3255	1770	221	SEG59	385	1770
140	COM37	5920	214	181	SEG19	3185	1770	222	SEG60	315	1770
141	COM38	5920	284	182	SEG20	3115	1770	223	SEG61	245	1770
142	COM39	5920	354	183	SEG21	3045	1770	224	SEG62	175	1770
143	COM40	5920	424	184	SEG22	2975	1770	225	SEG63	105	1770
144	COM49	5920	494	185	SEG23	2905	1770	226	SEG64	35	1770
145	COM50	5920	564	186	SEG24	2835	1770	227	SEG65	-35	1770
146	COM51	5920	634	187	SEG25	2765	1770	228	SEG66	-105	1770
147	COM52	5920	704	188	SEG26	2695	1770	229	SEG67	-175	1770
148	COM53	5920	774	189	SEG27	2625	1770	230	SEG68	-245	1770
149	COM54	5920	844	190	SEG28	2555	1770	231	SEG69	-315	1770
150	COM55	5920	914	191	SEG29	2485	1770	232	SEG70	-385	1770
151	COM56	5920	984	192	SEG30	2415	1770	233	SEG71	-455	1770
152	SEGI1	5920	1054	193	SEG31	2345	1770	234	SEG72	-525	1770
153	SEGI2	5920	1124	194	SEG32	2275	1770	235	SEG73	-595	1770
154	DUMMY	5920	1194	195	SEG33	2205	1770	236	SEG74	-665	1770
155	DUMMY	5005	1770	196	SEG34	2135	1770	237	SEG75	-735	1770
156	DUMMY	4935	1770	197	SEG35	2065	1770	238	SEG76	-805	1770
157	DUMMY	4865	1770	198	SEG36	1995	1770	239	SEG77	-875	1770
158	DUMMY	4795	1770	199	SEG37	1925	1770	240	SEG78	-945	1770
159	DUMMY	4725	1770	200	SEG38	1855	1770	241	SEG79	-1015	1770
160	DUMMY	4655	1770	201	SEG39	1785	1770	242	SEG80	-1085	1770
161	DUMMY	4585	1770	202	SEG40	1715	1770	243	SEG81	-1155	1770
162	DUMMY	4515	1770	203	SEG41	1645	1770	244	SEG82	-1225	1770
163	SEG1	4445	1770	204	SEG42	1575	1770	245	SEG83	-1295	1770
164	SEG2	4375	1770	205	SEG43	1505	1770	246	SEG84	-1365	1770

Table 2. Pad Location (Continued)

[Unit: μm]

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
247	SEG85	-1435	1770	277	SEG115	-3535	1770	307	COM60	-5920	634
248	SEG86	-1505	1770	278	SEG116	-3605	1770	308	COM59	-5920	564
249	SEG87	-1575	1770	279	SEG117	-3675	1770	309	COM58	-5920	494
250	SEG88	-1645	1770	280	SEG118	-3745	1770	310	COM57	-5920	424
251	SEG89	-1715	1770	281	SEG119	-3815	1770	311	COM48	-5920	354
252	SEG90	-1785	1770	282	SEG120	-3885	1770	312	COM47	-5920	284
253	SEG91	-1855	1770	283	SEG121	-3955	1770	313	COM46	-5920	214
254	SEG92	-1925	1770	284	SEG122	-4025	1770	314	COM45	-5920	144
255	SEG93	-1995	1770	285	SEG123	-4095	1770	315	COM44	5920	74
256	SEG94	-2065	1770	286	SEG124	-4165	1770	316	COM43	-5920	4
257	SEG95	-2135	1770	287	SEG125	-4235	1770	317	COM42	-5920	-66
258	SEG96	-2205	1770	288	SEG126	-4305	1770	318	COM41	-5920	-136
259	SEG97	-2275	1770	289	SEG127	-4375	1770	319	COM32	-5920	-206
260	SEG98	-2345	1770	290	SEG128	-4445	1770	320	COM31	-5920	-276
261	SEG99	-2415	1770	291	DUMMY	-4515	1770	321	COM30	-5920	-346
262	SEG100	-2485	1770	292	DUMMY	-4585	1770	322	COM29	-5920	-416
263	SEG101	-2555	1770	293	DUMMY	-4655	1770	323	COM28	-5920	-486
264	SEG102	-2625	1770	294	DUMMY	-4725	1770	324	COM27	-5920	-556
265	SEG103	-2695	1770	295	DUMMY	-4795	1770	325	COM26	-5920	-626
266	SEG104	-2765	1770	296	DUMMY	-4865	1770	326	COM25	-5920	-696
267	SEG105	-2835	1770	297	DUMMY	-4935	1770	327	COM16	-5920	-766
268	SEG106	-2905	1770	298	DUMMY	-5005	1770	328	COM15	-5920	-836
269	SEG107	-2975	1770	299	DUMMY	-5920	1194	329	COM14	-5920	-906
270	SEG108	-3045	1770	300	SEGI3	-5920	1124	330	COM13	-5920	-976
271	SEG109	-3115	1770	301	SEGI4	-5920	1054	331	COM12	-5920	-1046
272	SEG110	-3185	1770	302	COMI2	-5920	984	332	COM11	-5920	-1116
273	SEG111	-3255	1770	303	COM64	-5920	914	333	COM10	-5920	-1186
274	SEG112	-3325	1770	304	COM63	-5920	844	334	COM9	-5920	-1256
275	SEG113	-3395	1770	305	COM62	-5920	774	335	DUMMY	-5920	-1326
276	SEG114	-3465	1770	306	COM61	-5920	704				

PIN DESCRIPTION

POWER SUPPLY

Table 3. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td rowspan="2">Power</td><td>Power supply
Connect to MPU power supply pin</td></tr>
<tr><td>VSS</td><td>0V (GND)</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>Bias voltage level for LCD driving
Voltages have the following relationship:
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the on-chip power circuit is active, these voltages are generated according to the state of LCD bias, as following table.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/9 bias</td><td>(8/9) x V0</td><td>(7/9) x V0</td><td>(2/9) x V0</td><td>(1/9) x V0</td></tr>
<tr><td>1/8 bias</td><td>(7/8) x V0</td><td>(6/8) x V0</td><td>(2/8) x V0</td><td>(1/8) x V0</td></tr>
<tr><td>1/7 bias</td><td>(6/7) x V0</td><td>(5/7) x V0</td><td>(2/7) x V0</td><td>(1/7) x V0</td></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table></td></tr>
</table>

LCD DRIVER SUPPLY

Table 3. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>CAP1+</td><td rowspan="6">O</td><td>Capacitor1+ connect for the internal voltage converter</td></tr>
<tr><td>CAP1-</td><td>Capacitor1- connect for the internal voltage converter</td></tr>
<tr><td>CAP2+</td><td>Capacitor2+ connect for the internal voltage converter</td></tr>
<tr><td>CAP2-</td><td>Capacitor2- connect for the internal voltage converter</td></tr>
<tr><td>CAP3+</td><td>Capacitor3+ connect for the internal voltage converter</td></tr>
<tr><td>CAP3-</td><td>Capacitor3- connect for the internal voltage converter</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>Voltage converter output</td></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjustment pin which is valid only when using external resistors</td></tr>
<tr><td>REF</td><td>I</td><td>Select the reference voltage of internal voltage regulator
REF = "High": The reference voltage of internal voltage regulator is the voltage of VDD.
REF = "Low": The reference voltage of internal voltage regulator is the internal V_{REF} (2.0V).</td></tr>
</table>

SYSTEM CONTROL

Table 3. Pin Description (Continued)

Name	I/O	Description
CK	I	External clock input It must be fixed to "High" or “Low” when the internal oscillation circuit is used. In case of external clock mode, used as the clock input and OSC bit should be OFF.
MI	I	Select the kinds of the MPU to interface When MI = "High": 6800-series MPU interface mode When MI = "Low": 8080-series MPU interface
IF	I	Select the interface bit length when parallel interfacing (PS = "High") When IF = "High": 8-bit interface mode When IF = "Low": 4-bit interface mode
PS	I	Select Interface mode with the MPU When PS = "High": parallel interface mode When PS = "Low": serial interface mode

MPU INTERFACE

Table 3. Pin Description (Continued)

Name	I/O	Description
RESET	I	Hardware reset input Initialization is performed by edge sensing (rising or falling) of the RESET signal.
CSB	I	Used as chip selection input When CSB = "High", not selected When CSB = "Low", selected
RS	I	Used as register selection input When RS = "High", data register When RS = "Low", instruction register
RW_WR	I	When MI = "High"(6800-series MPU interfacing), used as read (RW_WR = "High") / write (RW_WR = "Low") selection input (R/W). When MI = "Low "(8080-series MPU interfacing), used as write enable input (WR).
E_RD	I	When MI = "High"(6800-series MPU interfacing), used as read/write enable input (E). When MI = "Low "(8080-series MPU interfacing), used as read enable input (RD).
DB0 to DB7	I/O	When 8-bit interface mode, DB0 to DB7 are used as bi-directional data bus pin. When 4-bit interface mode, only DB4 to DB7 are used as data input pin and DB0 to DB3 are not used. When serial mode, DB6 (SCL) is used as serial clock input pin, DB7 (SI) is used as serial data input pin and the others are not used.

LCD DRIVER OUTPUT

Table 3. Pin Description (Continued)

Name	I/O	Description
COM1 to COM64	O	Common signal output for character display
COMI1, COMI2	O	Common signal output for horizontal icon display These are the same signal but the name is different.
SEG1 to SEG128	O	Segment signal output for character display
SEGI1 to SEGI4	O	Segment signal output for vertical icon display

TEST PIN

Table 3. Pin Description (Continued)

Name	I/O	Description
TEST1 to TEST5	I	Test pin Connect these to "Low".

NOTE: **DUMMY - These pins should be opened (floated).**

FUNCTION DESCRIPTION

SYSTEM INTERFACE

KS0040 has two kinds interface type with MPU: bus mode (8- / 4-bit length), serial mode. Serial and bus mode is selected by PS pin.

Table 4. Various Kinds of MPU Interface

PS	MI	IF	CSB	RS	RW_WR	E_RD	DB0-3	DB4-5	DB6	DB7
Bus mode (H)	6800-series (H)	8 bit (H)	CSB	RS	R/$\overline{W}$	E	DB0-3	DB4-5	DB6	DB7
		4 bit (L)	CSB	RS	(L)	E	*	DB4-5	DB6	DB7
	8080-series (L)	8 bit (H)	CSB	RS	$\overline{WR}$	$\overline{RD}$	DB0-3	DB4-5	DB6	DB7
		4 bit (L)	CSB	RS	$\overline{WR}$	(H)/(L)	*	DB4-5	DB6	DB7
Serial mode (L)	(H)/(L)	(H)/(L)	CSB	RS	(H)/(L)	(H)/(L)	*	*	SCL	SI

NOTE: “*” - Don’t care ("High", "Low" or "Open").
(H)/(L): fixed “High” (V_{DD}) or “Low” (V_{SS})
NOTE: Read operation is not permitted to 4-bit or serial interface mode.

PS: "High" = parallel interface mode, "Low" = serial interface mode
MI: "High" = 6800-series MPU interface, "Low" = 8080-series MPU interface mode
IF: "High" = 8-bit interface mode, "Low" = 4-bit interface mode
CSB: "High" = chip not selected, "Low" = chip selected
RS: "High" = data Register select, "Low" = instruction register select
RW_WR: 6800-series read / write select, 8080-series active "High " write enable
E_RD: 6800-series "Low" enable, 8080-series active "Low " read enable
SCL (DB6): serial clock input
SI (DB7): serial data input

Interface with MPU in Parallel Bus Mode (PS = "High")

In parallel interface mode, 6800-series and 8080-series MPU is selected by MI pin, and interface bit length (8- / 4-bit) is selected by IF pin. During write operation, the 16-bit data register (DR) and the 8-bit instruction register (IR) is used. The data register (DR) is used as temporary data storage place from MPU for being written into DDRAM / CGRAM / ICONRAM. The target RAM is selected by RAM selection instruction. The instruction register (IR) is used only to store instruction code transferred from MPU. To select either DR or IR, use the RS input pin in parallel mode or serial mode.

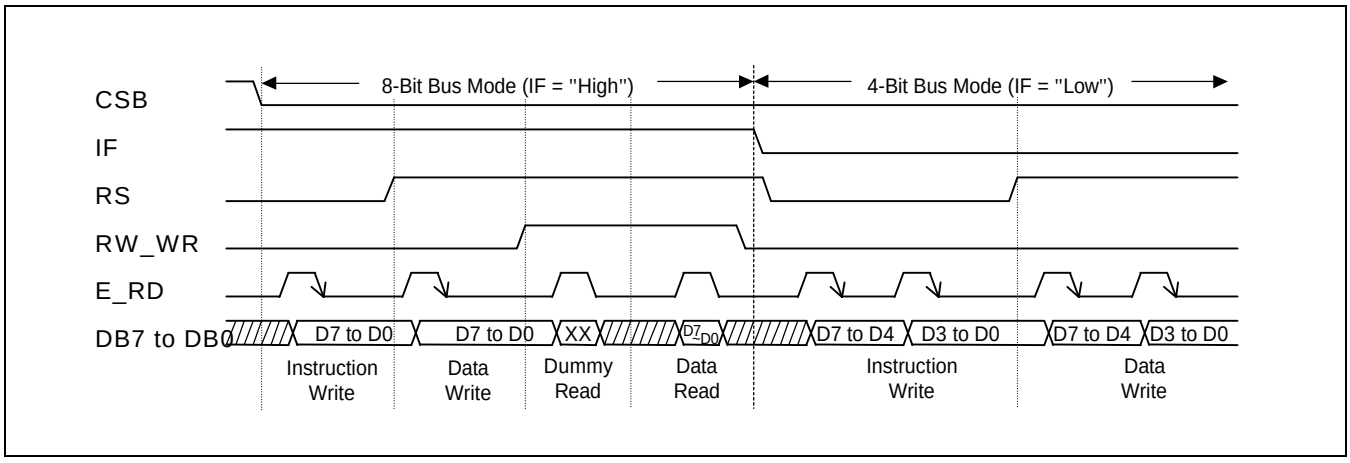


Figure 3. Timing Diagram of 6800-series Bus Mode Data Transfer (MI = "High")

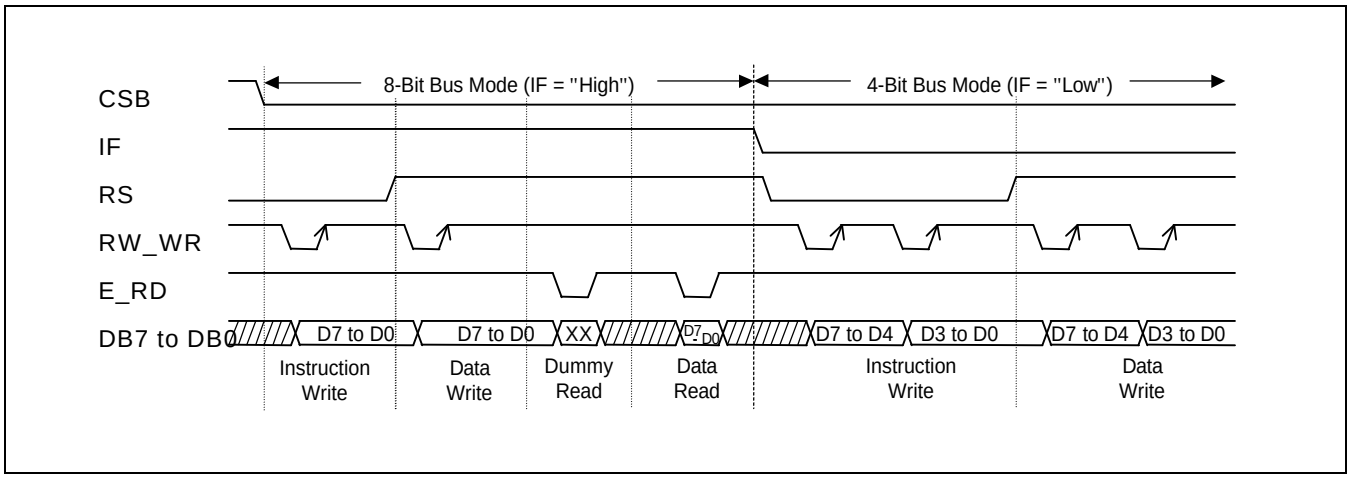


Figure 4. Timing Diagram of 8080-Series Bus Mode Data Transfer (MI = "Low")

Interface with MPU in Serial Bus Mode (PS = "Low")

When PS input pin is "Low", clock synchronized serial interface mode is selected. At this time, the following four ports, SCL (DB6, synchronizing transfer clock input), SI (DB7, serial data input), and RS (register selection input), CSB (chip selection input) are used. By setting CSB to "Low", KS0040 can receive SCL input. If CSB is set to "High", KS0040 initialize the interface circuit (8-bit shift register and 3-bit counter). Serial data is input in the order of "D7, D6, D5, D4, D3, D2, D1, D0" from the serial data input pin (SI = DB7) at the rising edge of serial clock (SCL = DB6).
At the rising edge of the 8th serial clock, the serial data (D7-D0) is converted into 8-bit bus data. The RS input of the DR / IR selection is latched at the rising edge of the 8th serial clock (SCL).

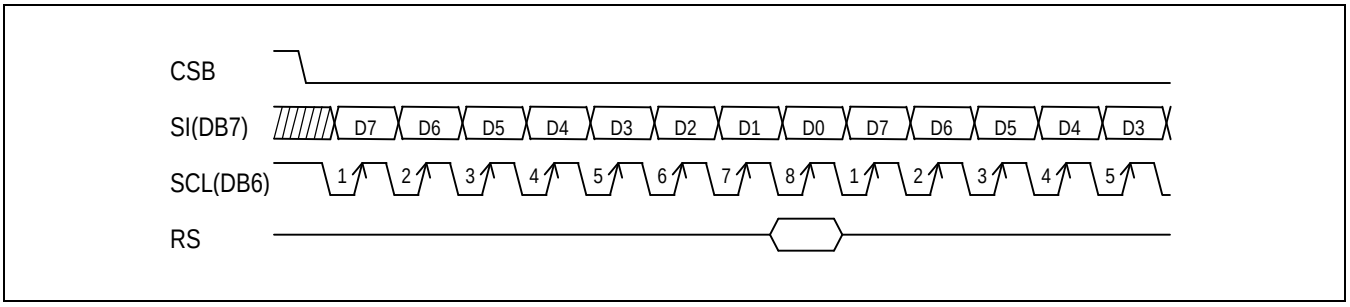


Figure 5. Timing Diagram of Serial Data Transfer

RAM MAP

Internal RAM has total 1,200 bytes, and consist of DDRAM (128 bytes), ICONRAM (48 bytes) and CGRAM (1,024 bytes).

Table 5. RAM Map

R3 R2 R1 R0	Address	RAM data usage (D7~D0)	RAM size
0 0 0 0	00H - 0FH 10H - 1FH 20H - 2FH 30H - 3FH 40H - 4FH 50H - 5FH 60H - 6FH 70H - 7FH	DDRAM (1st line) } EXT = **0** DDRAM (2nd line) DDRAM (3rd line) DDRAM (4th line) DDRAM (5th line) } EXT = **1** DDRAM (6th line) DDRAM (7th line) DDRAM (8th line)	128byte
0 0 0 1	00H - 0FH 10H - 1FH 20H - 2FH	ICONRAM upper 128 icons (C1 ~ C128) ICONRAM lower 128 icons (C129 ~ C256) ICONRAM COMS data (S1 ~ S128)	48byte
1 0 0 0	00H - 1FH 20H - 3FH 40H - 5FH 60H - 7FH	CGRAM 1st 16 x 16 pattern CGRAM 2nd 16 x 16 pattern CGRAM 3rd 16 x 16 pattern CGRAM 4th 16 x 16 pattern	128byte (page 0)
1 0 0 1	00H - 1FH 20H - 3FH 40H - 5FH 60H - 7FH	CGRAM 5th 16 x 16 pattern CGRAM 6th 16 x 16 pattern CGRAM 7th 16 x 16 pattern CGRAM 8th 16 x 16 pattern	128byte (page 1)
1 0 1 0	00H - 1FH 20H - 3FH 40H - 5FH 60H - 7FH	CGRAM 9th 16 x 16 pattern CGRAM 10th 16 x 16 pattern CGRAM 11th 16 x 16 pattern CGRAM 12th 16 x 16 pattern	128byte (page 2)
1 0 1 1	00H - 1FH 20H - 3FH 40H - 5FH 60H - 7FH	CGRAM 13th 16 x 16 pattern CGRAM 14th 16 x 16 pattern CGRAM 15th 16 x 16 pattern CGRAM 16th 16 x 16 pattern	128byte (page 3)
1 1 0 0	00H - 1FH 20H - 3FH 40H - 5FH 60H - 7FH	CGRAM 17th 16 x 16 pattern CGRAM 18th 16 x 16 pattern CGRAM 19th 16 x 16 pattern CGRAM 20th 16 x 16 pattern	128byte (page 4)
1 1 0 1	00H - 1FH 20H - 3FH 40H - 5FH 60H - 7FH	CGRAM 21st 16 x 16 pattern CGRAM 22nd 16 x 16 pattern CGRAM 23rd 16 x 16 pattern CGRAM 24th 16 x 16 pattern	128byte (page 5)
1 1 1 0	00H - 1FH 20H - 3FH 40H - 5FH 60H - 7FH	CGRAM 25th 16 x 16 pattern CGRAM 26th 16 x 16 pattern CGRAM 27th 16 x 16 pattern CGRAM 28th 16 x 16 pattern	128byte (page 6)
1 1 1 1	00H - 1FH 20H - 3FH 40H - 5FH 60H - 7FH	CGRAM 29th 16 x 16 pattern CGRAM 30th 16 x 16 pattern CGRAM 31st 16 x 16 pattern CGRAM 32nd 16 x 16 pattern	128byte (page 7)

NOTE: R3- R0: RAM / system select register

Display Data RAM (DDRAM)

DDRAM stores 16-bits character code in FCGROM / CGRAM and 8-bits character code in HCGROM, and its maximum number is 128-byte (64-word: 64 Characters of full-size fonts or 128 characters of half-size fonts). The displayable area is 64-byte and the other is extended data area. To display extended DDRAM data, set the EXT bit "High" in system register set instruction.

DDRAM address is set by the address counter (AC) as a hexadecimal number.

MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

The Relations of DDRAM Address and Display Position

When DDRAM is set to normal mode (EXT = "Low")

	1st	2nd	3rd	4th	5th	6th	7th	8th
COM1 | COM16	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
COM17 | COM32	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
COM33 | COM48	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
COM49 | COM64	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F

(a) Display Shift is not performed

	1st	2nd	3rd	4th	5th	6th	7th	8th
COM1 | COM16	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
COM17 | COM32	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
COM33 | COM48	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
COM49 | COM64	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

(b) Display Shift Up is performed

	1st	2nd	3rd	4th	5th	6th	7th	8th
COM1 | COM16	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
COM17 | COM32	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
COM33 | COM48	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
COM49 | COM64	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F

(c) Display Shift Down is performed

Figure 6. Normal Mode DDRAM Address (EXT = "Low")

When DDRAM is Set to Extended Mode (EXT = "High")

	1st	2nd	3rd	4th	5th	6th	7th	8th
COM1 | COM16	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
COM17 | COM32	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
COM33 | COM48	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
COM49 | COM64	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F
	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F

(a) Display Shift is not performed

	1st	2nd	3rd	4th	5th	6th	7th	8th
COM1 | COM16	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
COM17 | COM32	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
COM33 | COM48	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
COM49 | COM64	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F
	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

(b) Display Shift-up is performed

	1st	2nd	3rd	4^{th}	5th	6th	7th	8th
COM1 | COM16	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
COM17 | COM32	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
COM33 | COM48	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
COM49 | COM64	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F

(c) Display Shift-down is performed

Figure 7. Extended Mode DDRAM Address (EXT = "High")

SAMSUNG ELECTRONICS

Character Generator RAM (CGRAM)

CGRAM is used for user defined character pattern. It can generate 32,16 X 16 dots full-size fonts include cursor position. The capacity of CGRAM can support bitmap graphics 128 X 64 dot. To use the character pattern in CGRAM write the character code into DDRAM like table 6.

Table 6. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

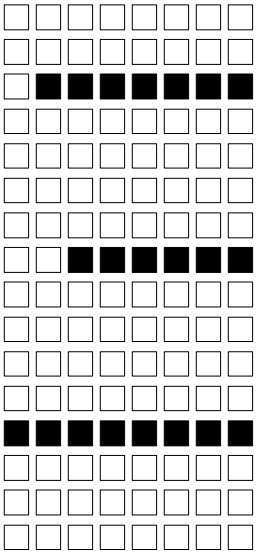
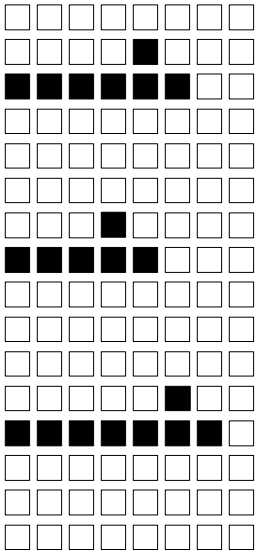
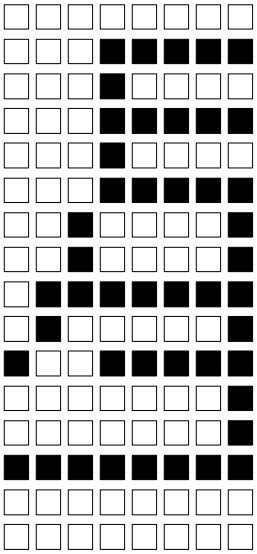
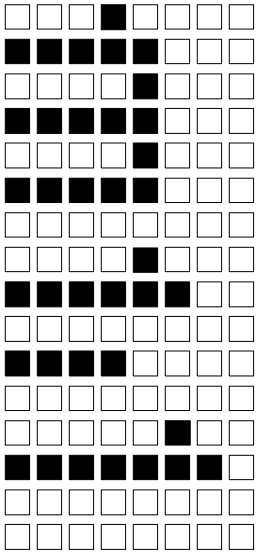
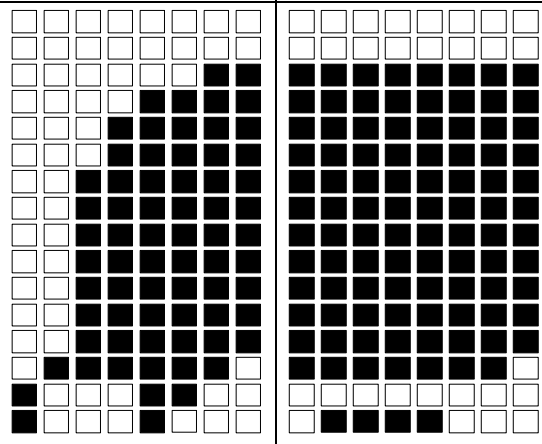
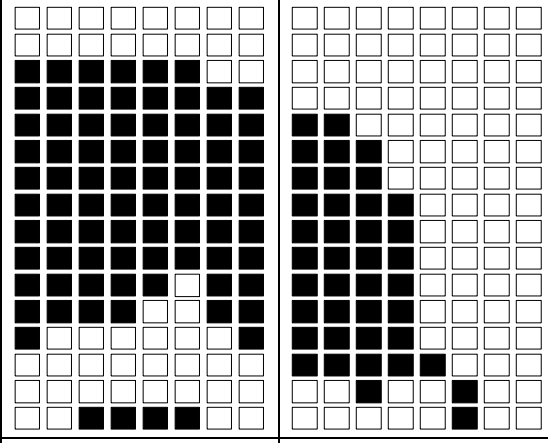
Character code (DDRAM data)	CGRAM address		CGRAM data (A0 = 0)	CGRAM data (A0 = 1)	Pattern number
	R R R R 3 2 1 0	A A A A A A 6 5 4 3 2 1	D D D D D D D D 7 6 5 4 3 2 1 0	D D D D D D D D 7 6 5 4 3 2 1 0	
0000h	1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 1 1 0 0 0 1 0 0 0 0 0 1 0 1 0 0 0 1 1 0 0 0 0 1 1 1 0 0 1 0 0 0 0 0 1 0 0 1 0 0 1 0 1 0 0 0 1 0 1 1 0 0 1 1 0 0 0 0 1 1 0 1 0 0 1 1 1 0 0 0 1 1 1 1			Pattern 1
:	:	:	:	:	:
001Fh	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 0 0 0 1 1 0 0 0 1 1 1 0 0 1 0 1 1 0 0 1 1 1 1 0 1 0 0 1 1 0 1 0 1 1 1 0 1 1 0 1 1 0 1 1 1 1 1 1 0 0 0 1 1 1 0 0 1 1 1 1 0 1 0 1 1 1 0 1 1 1 1 1 1 0 0 1 1 1 1 0 1 1 1 1 1 1 0 1 1 1 1 1 1			Pattern 32

Table 7. Example for Bitmap Graphic by CGRAM

Character code (DDRAM data)	CGRAM address		CGRAM data (A0 = 0)	CGRAM data (A0 = 1)	Pattern number
	R R R R 3 2 1 0	A A A A A A 6 5 4 3 2 1	D D D D D D D D 7 6 5 4 3 2 1 0	D D D D D D D D 7 6 5 4 3 2 1 0	
0000h	1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 1 1 0 0 0 1 0 0 0 0 0 1 0 1 0 0 0 1 1 0 0 0 0 1 1 1 0 0 1 0 0 0 0 0 1 0 0 1 0 0 1 0 1 0 0 0 1 0 1 1 0 0 1 1 0 0 0 0 1 1 0 1 0 0 1 1 1 0 0 0 1 1 1 1			Pattern 1
0001h	1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0	0 1 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0 0 1 0 0 1 1 0 1 0 1 0 0 0 1 0 1 0 1 0 1 0 1 1 0 0 1 0 1 1 1 0 1 1 0 0 0 0 1 1 0 0 1 0 1 1 0 1 0 0 1 1 0 1 1 0 1 1 1 0 0 0 1 1 1 0 1 0 1 1 1 1 0 0 1 1 1 1 1			Pattern 2
:	:	:	:	:	:

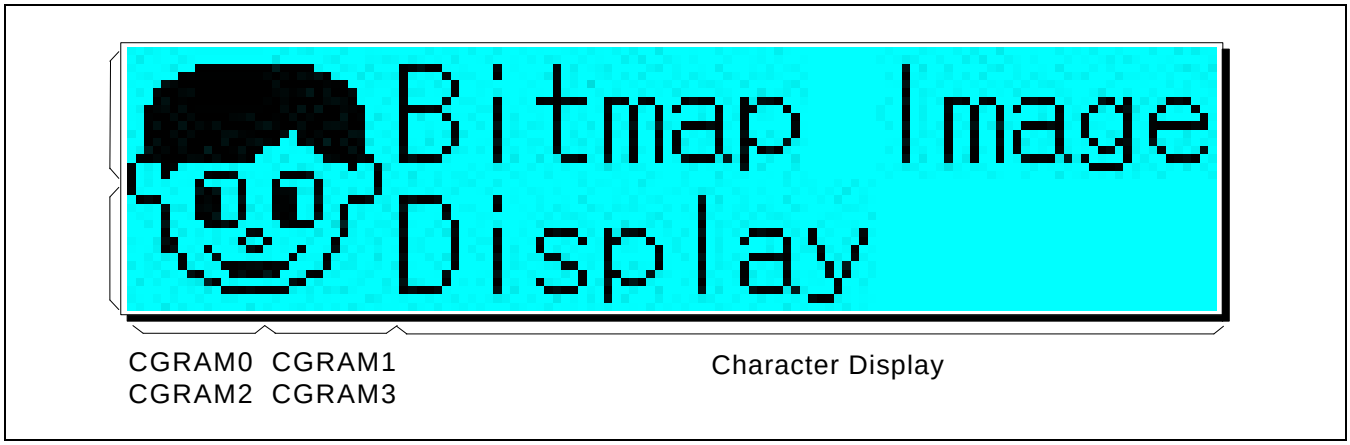


Figure 8. Example for Bitmap Display with Character



Figure 9. Relationship between CGRAM Full Graphic Mode Data Writing and Display Pattern (FG = "High")

During CGROM full graphic mode, CGRAM data is written from (*1) to (*1024) by 8-bit length

Table 8. The Order of CGRAM Data Writing

(*1)	(*2)	(*3)	(*4)	(*5)	(*6)	---	---	---	---	(*15)	(*16)
(*17)	(*18)	(*19)	(*20)	*(21)	(*22)	---	---	---	---	(*31)	(*32)
|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|
(*1009)	(*1010)	(*1011)	(*1012)	(*1013)	(*1014)	---	---	---	(*1022)	(*1023)	(*1024)

Segment & Common Icon RAM (ICONRAM)

ICONRAM has Segment / Common Icon pattern data. COMI1 or COMI2 and SEGI1~4 makes the data of ICONRAM enable to display icons.

Table 9. Relationship between ICONRAM Address and Display Pattern

ICONRAM address		ICONRAM bits								Icons
A5 A4	A3 A2 A1 A0	D7	D6	D5	D4	D3	D2	D1	D0	
0 0	0 0 0 0	VL1	VL2	VR1	VR2	VL3	VL4	VR3	VR4	Upper 128 SEGI icons data (*1)
	0 0 0 1	VL5	VL6	VR5	VR6	VL7	VL8	VR7	VR8	
	:	:								
	1 1 1 0	VL57	VL58	VR57	VR58	VL59	VL60	VR59	VR60	
	1 1 1 1	VL61	VL62	VR61	VR62	VL63	VL64	VR63	VR64	
0 1	0 0 0 0	VL65	VL66	VR65	VR66	VL67	VL68	VR67	VR68	Lower 128 SEGI icons data (*2)
	0 0 0 1	VL69	VL70	VR69	VR70	VL71	VL72	VR71	VR72	
	:	:								
	1 1 1 0	VL121	VL122	VR121	VR122	VL123	VL124	VR123	VR124	
	1 1 1 1	VL125	VL126	VR125	VR126	VL127	VL128	VR127	VR128	
1 0	0 0 0 0	H1	H2	H3	H4	H5	H6	H7	H8	COMI icons data (*3)
	0 0 0 1	H9	H10	H11	H12	H13	H14	H15	H16	
	:	:								
	1 1 1 0	H113	H114	H115	H116	H117	H118	H119	H120	
	1 1 1 1	H121	H122	H123	H124	H125	H126	H127	H128	

NOTE: VLn: vertical left n-th icon, VRn: vertical right n-th icon
Hn: horizontal n-th icon (where n = 1 to 128)

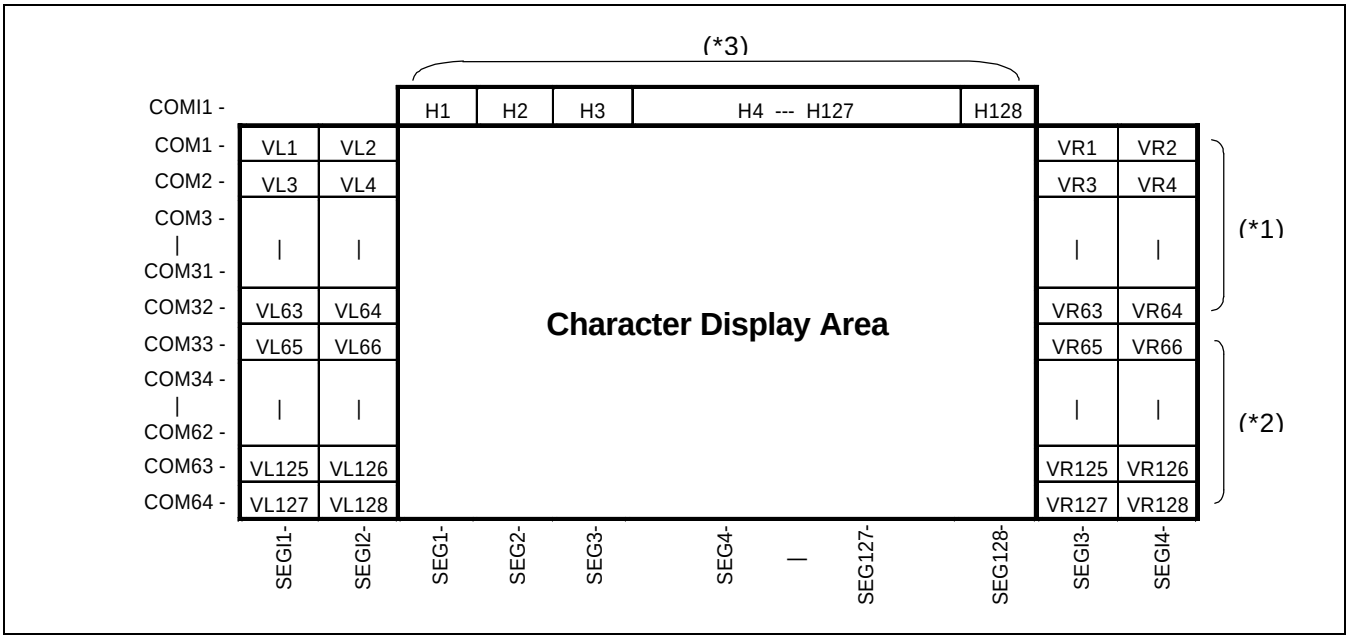


Figure 10. Relationship between Icon Pattern Data and COM / SEG Line (When DIRC = 0, DIRS = 0)

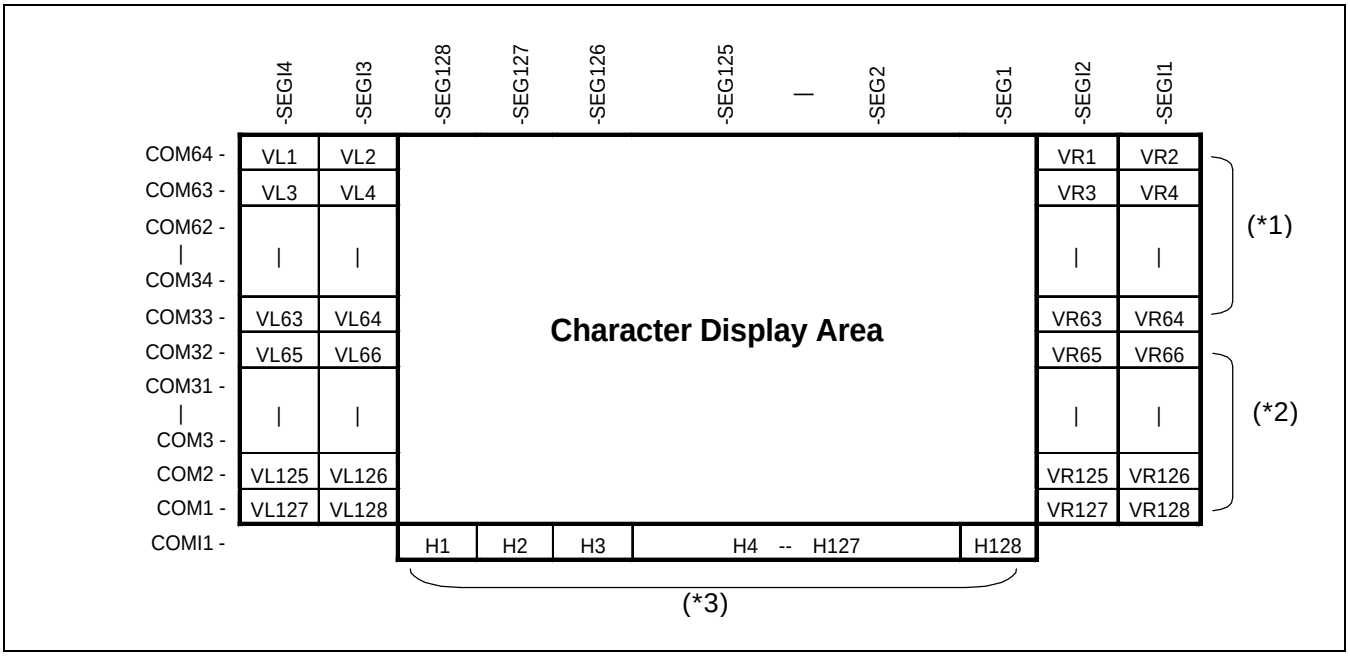


Figure 11. Relationship between Icon Pattern Data and COM / SEG Line (When DIRC = 1, DIRS = 1)

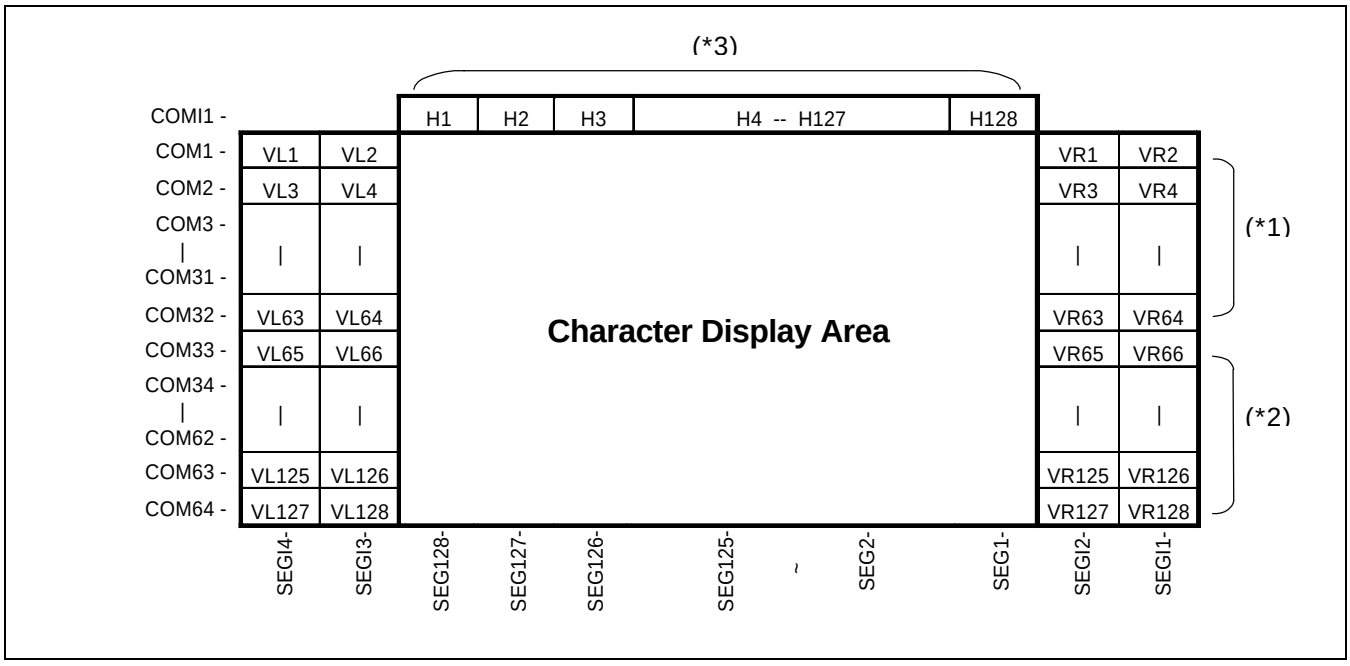


Figure 12. Relationship between Icon Pattern Data and COM / SEG Line (When DIRC = 0, DIRS = 1)

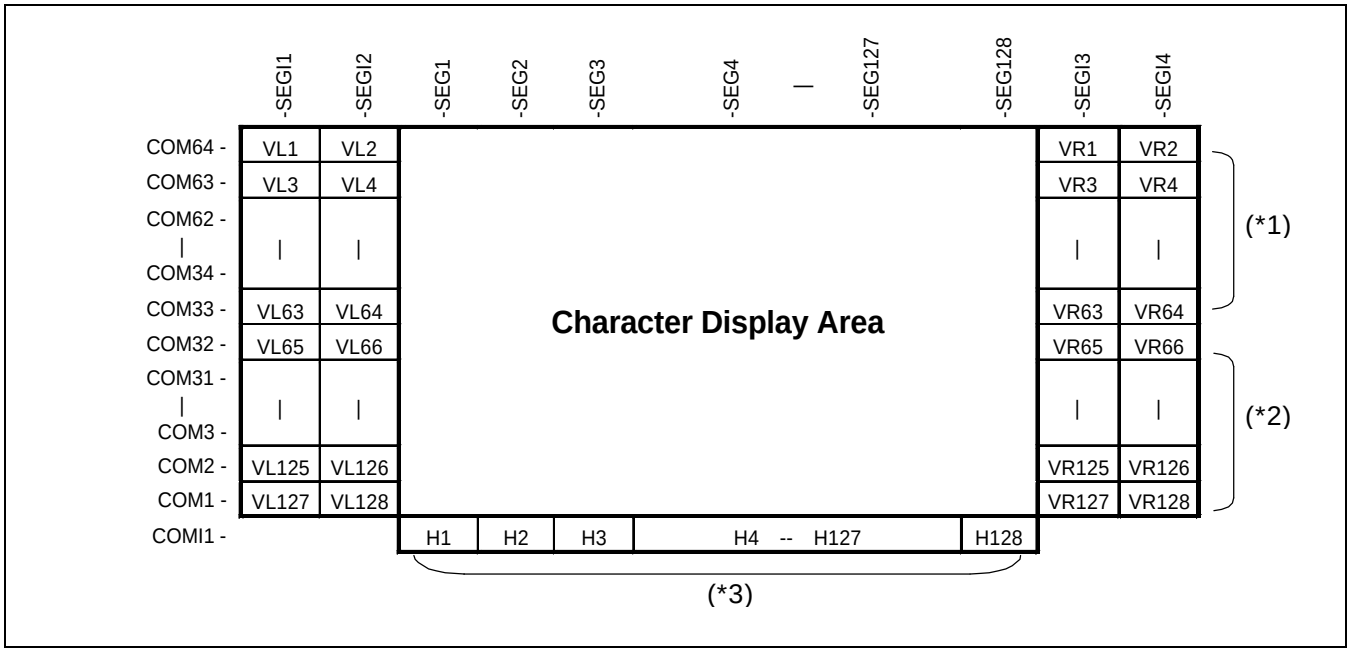


Figure 13. Relationship between Icon Pattern Data and COM / SEG Line (When DIRC = 1, DIRS = 0)

SAMSUNG ELECTRONICS

CHARACTER GENERATOR ROM FOR A FULL-SIZE FONT (FCGROM)

FCGROM generates 16 x 16 characters pattern from Character Generate code in DDRAM. FCGROM has 16 X 16-dot 8,160 character pattern include cursor position for Asian language character font (like Chinese, Japanese Kanji, Korean). If the data in cursor position bit are high, the data are included to the character pattern. So, the selected positions are always ON without regard to cursor position.

CHARACTER GENERATOR ROM FOR A HALF-SIZE FONT (HCGROM)

HCGROM generates 8 x 16 characters pattern from Character Generate code in DDRAM. HCGROM has 8 X 16-dot 128 character pattern include cursor position for half-size font (like alphanumeric characters and symbols). If the data in cursor position bit are high, the data are included to the character pattern. So, the selected positions are always ON without regard to cursor position.

Table 10. Relationship between CGROM Address and Font Pattern (KS0040-00 Font)

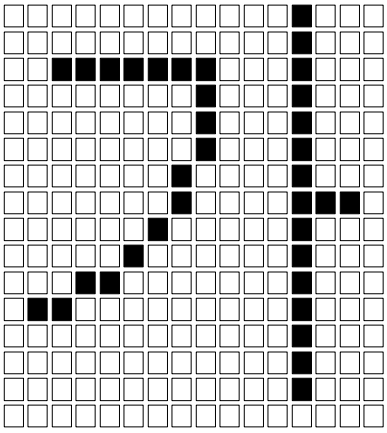
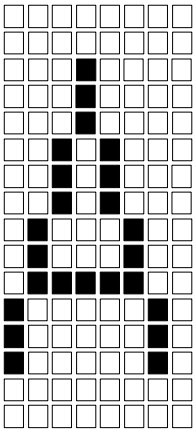
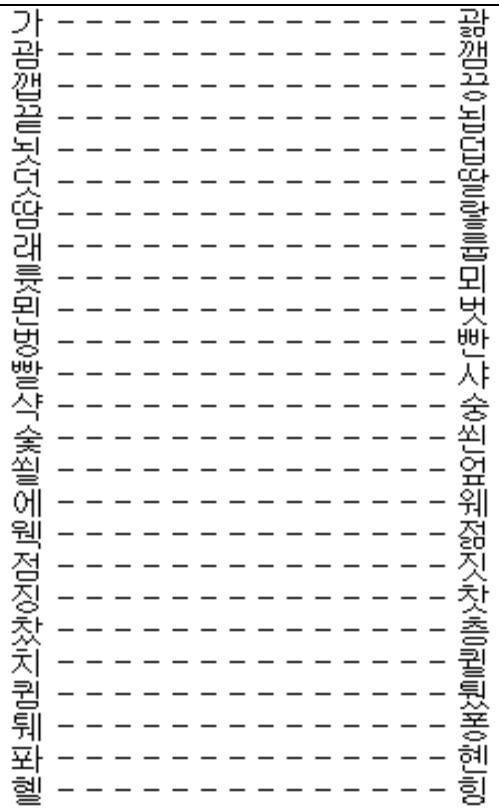
FCGROM address	Font data (D15 ~ D0)	HCGROM address	Font data (D7 ~ D0)
A13 ~ A0	F E F C B A 9 8 7 6 5 4 3 2 1 0	A6 ~ A0	7 6 5 4 3 2 1 0
0380(h)		41(h)	

Table 11. KS0040-00 Font (KSC5601 Code) Map

KSC5601 code	KS0040 FCGROM code	Font data
-	0000 (H) ~ 001F (H)	CGRAM font area
A1A1 (H) ~ ACFE (H)	0020 (H) ~ 037F (H)	Symbol character area
B0A1 (H) ~ B0FE (H) B1A1 (H) ~ B1FE (H) B2A1 (H) ~ B2FE (H) B3A1 (H) ~ B3FE (H) B4A1 (H) ~ B4FE (H) B5A1 (H) ~ B5FE (H) B6A1 (H) ~ B6FE (H) B7A1 (H) ~ B7FE (H) B8A1 (H) ~ B8FE (H) B9A1 (H) ~ B9FE (H) BAA1 (H) ~ BAFE (H) BBA1 (H) ~ BBFE (H) BCA1 (H) ~ BCFE (H) BDA1 (H) ~ BDFE (H) BEA1 (H) ~ BEFE (H) BFA1 (H) ~ BFFE (H) C0A1 (H) ~ C0FE (H) C1A1 (H) ~ C1FE (H) C2A1 (H) ~ C2FE (H) C3A1 (H) ~ C3FE (H) C4A1 (H) ~ C4FE (H) C5A1 (H) ~ C5FE (H) C6A1 (H) ~ C6FE (H) C7A1 (H) ~ C7FE (H) C8A1 (H) ~ C8FE (H)	0380 (H) ~ 03DD (H) 03DE (H) ~ 043B (H) 043C (H) ~ 0499 (H) 049A (H) ~ 04F7 (H) 04F8 (H) ~ 0555 (H) 0556 (H) ~ 05B3 (H) 05B4 (H) ~ 0611 (H) 0612 (H) ~ 066F (H) 0670 (H) ~ 06CD (H) 06CE (H) ~ 072B (H) 072C (H) ~ 0789 (H) 078A (H) ~ 07E7 (H) 07E8 (H) ~ 0845 (H) 0846 (H) ~ 08A3 (H) 08A4 (H) ~ 0901 (H) 0902 (H) ~ 095F (H) 0960 (H) ~ 09BD (H) 09BC (H) ~ 0A1B (H) 0A1C (H) ~ 0A7C (H) 0A7D (H) ~ 0AD7 (H) 0AD8 (H) ~ 0B35 (H) 0B36 (H) ~ 0B93 (H) 0B94 (H) ~ 0BF1 (H) 0BF2 (H) ~ 0C4F (H) 0C50 (H) ~ 0CAD (H)	
CAA1 (H) ~ CAFÉ (H) CBA1 (H) ~ CBFE (H) CCA1 (H) ~ CCFE (H) CDA1 (H) ~ CDFE (H) CEA1 (H) ~ CEFE (H) CFA1 (H) ~ CFFE (H) D0A1 (H) ~ D0FE (H) D1A1 (H) ~ D1FE (H) D2A1 (H) ~ D2FE (H) D3A1 (H) ~ D3FE (H) D4A1 (H) ~ D4FE (H) D5A1 (H) ~ D5FE (H) D6A1 (H) ~ D6FE (H) D7A1 (H) ~ D7FE (H) D8A1 (H) ~ D8FE (H) D9A1 (H) ~ D9FE (H) DAA1 (H) ~ DAFE (H) DBA1 (H) ~ DBFE (H) DCA1 (H) ~ DCFE (H) DDA1 (H) ~ DDFE (H)	0CB0 (H) ~ 0D0D (H) 0D0E (H) ~ 0D6B (H) 0D6C (H) ~ 0DC9 (H) 0DCA (H) ~ 0E27 (H) 0E28 (H) ~ 0E85 (H) 0E86 (H) ~ 0EE3 (H) 0EE4 (H) ~ 0F41 (H) 0F42 (H) ~ 0F9F (H) 0FA0 (H) ~ 0FFD (H) 0FFE (H) ~ 105B (H) 105C (H) ~ 10B9 (H) 10BA (H) ~ 1117 (H) 1118 (H) ~ 1175 (H) 1176 (H) ~ 11D3 (H) 11D4 (H) ~ 1231 (H) 1232 (H) ~ 128F (H) 1290 (H) ~ 12FD (H) 12EE (H) ~ 134B (H) 134C (H) ~ 13A9 (H) 13AA (H) ~ 1407 (H)	

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Table 11. KS0040F00 Font (KSC5601 Code) Map (Continued)

KSC5601 code	KS0040 FCGROM code	Font data
DEA1 (H) ~ DEFE (H)	1408 (H) ~ 1465 (H)	
DFA1 (H) ~ DFFE (H)	1466 (H) ~ 14C3 (H)	
E0A1 (H) ~ E0FE (H)	14C4 (H) ~ 1521 (H)	
E1A1 (H) ~ E1FE (H)	1522 (H) ~ 157F (H)	
E2A1 (H) ~ E2FE (H)	1580 (H) ~ 15DD (H)	
E3A1 (H) ~ E3FE (H)	15DE (H) ~ 163B (H)	
E4A1 (H) ~ E4FE (H)	163C (H) ~ 1699 (H)	
E5A1 (H) ~ E5FE (H)	169A (H) ~ 16F7 (H)	
E6A1 (H) ~ E6FE (H)	16F8 (H) ~ 1755 (H)	
E7A1 (H) ~ E7FE (H)	1756 (H) ~ 17B3 (H)	
E8A1 (H) ~ E8FE (H)	17B4 (H) ~ 1811 (H)	
E9A1 (H) ~ E9FE (H)	1812 (H) ~ 186F (H)	
EAA1 (H) ~ EAFE (H)	1870 (H) ~ 18CD (H)	
EBA1 (H) ~ EBFE (H)	18CE (H) ~ 192B (H)	
ECA1 (H) ~ ECFE (H)	192C (H) ~ 1989 (H)	
EDA1 (H) ~ EDFE (H)	198A (H) ~ 19E7 (H)	
EEA1 (H) ~ EEFE (H)	19E8 (H) ~ 1A45 (H)	
EEA1 (H) ~ EFFE (H)	1A46 (H) ~ 1AA3 (H)	
F0A1 (H) ~ F0FE (H)	1AA4 (H) ~ 1B01 (H)	
F1A1 (H) ~ F1FE (H)	1B02 (H) ~ 1B5F (H)	
F2A1 (H) ~ F2FE (H)	1B60 (H) ~ 1BBD (H)	
F3A1 (H) ~ F3FE (H)	1BBE (H) ~ 1C1B (H)	
F4A1 (H) ~ F4FE (H)	1C1C (H) ~ 1C79 (H)	
F5A1 (H) ~ F5FE (H)	1C7A (H) ~ 1CD7 (H)	
F6A1 (H) ~ F6FE (H)	1CD8 (H) ~ 1D35 (H)	
F7A1 (H) ~ F7FE (H)	1D36 (H) ~ 1D93 (H)	
F8A1 (H) ~ F8FE (H)	1D94 (H) ~ 1DF1 (H)	
F9A1 (H) ~ F9FE (H)	1DF2 (H) ~ 1E4F (H)	
FAA1 (H) ~ FAFE (H)	1E50 (H) ~ 1EAD (H)	
FBA1 (H) ~ FBFE (H)	1EAE (H) ~ 1F0B (H)	
FCA1 (H) ~ FCFE (H)	1F0C (H) ~ 1F69 (H)	
FDA1 (H) ~ FDFE (H)	1F6A (H) ~ 1FC7 (H)	

LOW POWER CONSUMPTION MODE

KS0040 has sleep mode for saving power consumption during standby period. (refer to "INITIALIZING & POWER SAVE MODE SETUP")

Sleep Mode

In the Sleep Mode, the power circuit and the oscillation circuit are turned OFF. This mode helps to save power consumption by reducing current to almost resting current level.

1. Liquid Crystal Display Output
   COM1 to COM64, COMI1, 2: V_{SS} level
   SEG1 to SEG128, SEGI1, 2, 3, 4: V_{SS} level

2. DDRAM, CGRAM, ICONRAM and register written information are saved.

3. Operation mode is retained the same as it was prior to execution of the sleep mode.
   All internal circuits are stopped.

4. Power Circuit and Oscillation Circuit
   The built-in supply circuit and the oscillation circuit are turned OFF automatically by using the sleep command.

LCD DRIVING CIRCUIT

LCD Driver circuit has 65 common and 132 segment signals for LCD driving. The data from CGROM / CGRAM / ICONRAM is transferred to 128-bit segment latch serially by 8-bits unit, and then it is stored to 128-bit shift latch. The data from ICONRAM is stored to 4-bit latch. When each common line is selected by 65-bit common register, segment data and segment icon data also output through segment driver from 128-bit segment latch and 4-bit segment icon latch. KS0040 has common and segment bi-directional function to help various panel applications. (refer to table 12 and table 13)

Table 12. SEG Data Shift Direction

DIRS	SEG data shift direction
Low	SEGI1, SEGI2, SEG1 → - - - - - - - → SEG128, SEGI3, SEGI4
High	SEGI4, SEGI3, SEG128 → - - - - - - - → SEG1, SEGI2, SEGI1

Table 13. COM Data Shift Direction

Duty	DIRC	COM data shift direction
1/17 (1-line mode)	Low	COM1 → - - - - - - - → COM16, COMI1 (COMI2)
	High	COM16 → - - - - - - - → COM1, COMI1 (COMI2)
1/33 (2-line mode)	Low	COM1 → - - - - - - - → COM32, COMI1 (COMI2)
	High	COM32 → - - - - - - - → COM1, COMI1 (COMI2)
1/49 (3-line mode)	Low	COM1 → - - - - - - - → COM48, COMI1 (COMI2)
	High	COM48 → - - - - - - - → COM1, COMI1 (COMI2)
1/65 (4-line mode)	Low	COM1 → - - - - - - - → COM64, COMI1 (COMI2)
	High	COM64 → - - - - - - - → COM1, COMI1 (COMI2)

DISPLAY SHIFT CONTROL

KS0040 has vertical dot-by-dot or character-by-character shift function, which are usable when display panel size is less than 4-line display and want to display the hidden-line data, or when extended DDRAM is set and want to display extended DDRAM data

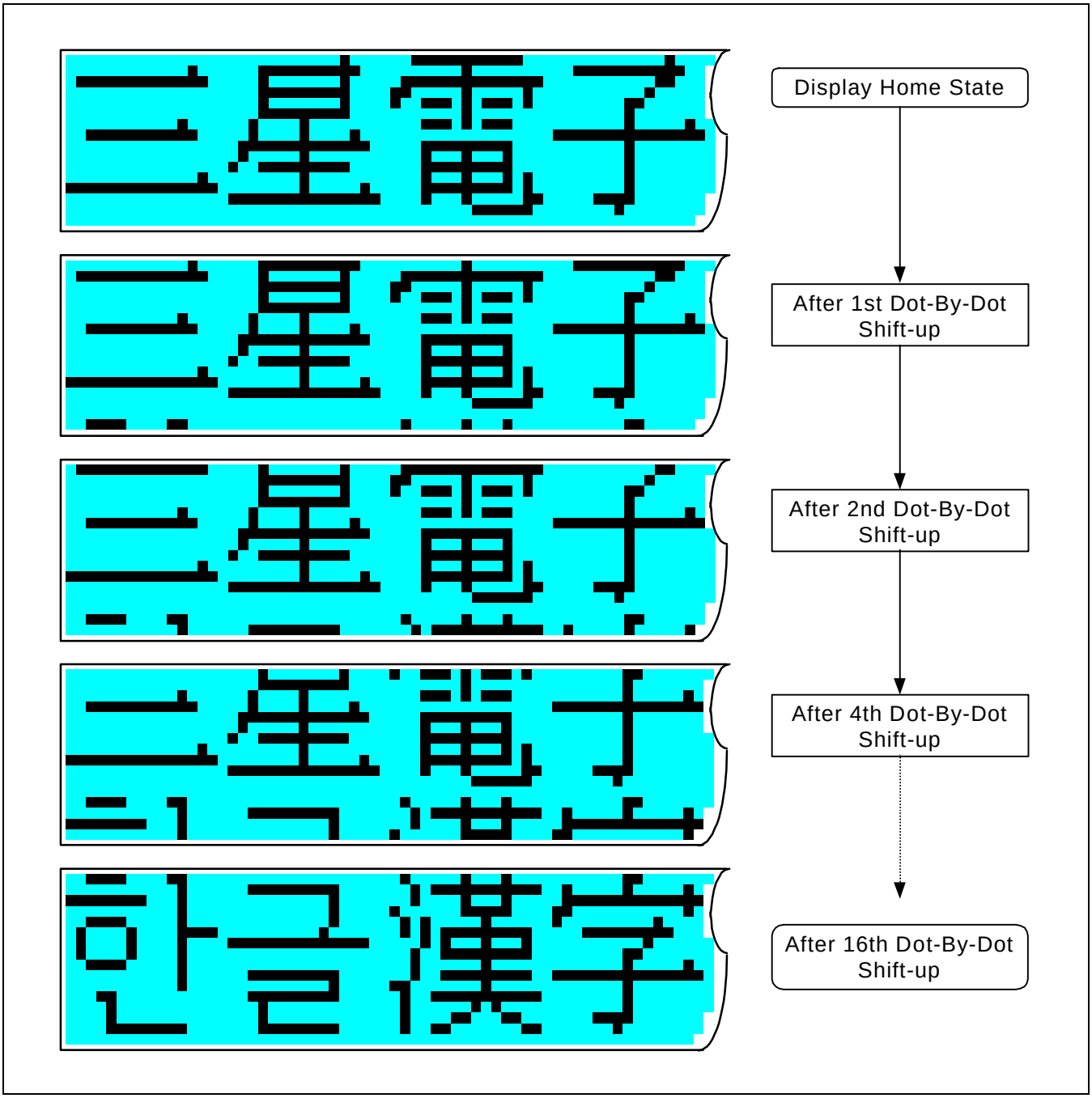


Figure 14. Vertical Dot-by-Dot Shift-up (down) Example

INSTRUCTION DESCRIPTION

Outline

To overcome the speed difference between internal clock of KS0040 and MPU clock, KS0040 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read / write and data bus.

Instruction can be divided four kinds,

(1) System register set instructions (power control, contrast value set, etc.)
(2) Internal RAM access instructions (RAM select, RAM address set, data read / write, etc.)
(3) Display control instructions (vertical shift, double height character, etc.)
(4) Others

The address of internal RAM is automatically increased or decreased by 1.

NOTE: Every instruction takes one cycle execution time, so to execute the next instruction, minimum E cycle time (tc) must be kept.

Table 14. Instruction table

Instruction	Instruction code									Description
	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
NOP	0	0 (Hex)				0	0	0	0	No operation
Return home	0	1 (Hex)				-	-	-	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed
Display control	0	2 (Hex)				D	CC	LC	REV	Display (D), character cursor (CC), line cursor (LC), B/W reverse display (REV) ON / OFF control
Power save mode	0	3 (Hex)				-	-	-	SLP	Sleep mode (SLP) ON / OFF control
Contrast increment / decrement	0	4 (Hex)				-	-	-	CID	Contrast increment (CID = 1) or decrement (CID = 0)
Vertical shift	0	5 (Hex)				-	-	CD	UD	Vertical character (CD = 1), dot (CD = 0) shift -up (UD = 1), down (UD = 0)
Double height character	0	6 (Hex)				-	EN	DH1	DH0	Double height character enable (EN) at selected line (DH1, DH0).
RAM select / system register set	0	7 (Hex)				R3	R2	R1	R0	R3 R2 R1 R0 / Selected RAM / register 0 0 0 0 / DDRAM 0 0 0 1 / ICONRAM 1 0 0 0 / CGRAM page 0 - / - 1 1 1 1 / CGRAM page 7 0 1 0 0 / Power control register 0 1 0 1 / Contrast control register 0 1 1 0 / Environment control register 0 1 1 1 / Function control register
RAM address set	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	DD / CG / ICON RAM address setting, one of 3 RAM is selected by RAM select instruction.
Write data	1	D7	D6	D5	D4	D3	D2	D1	D0	DD / CG / ICON RAM and system register data write
Read data	1	D7	D6	D5	D4	D3	D2	D1	D0	DD / CG / ICON RAM and system register data read

NOTE: "-" - Don't care

Table 15. System Register Values

Register select bit				Selected system register	Register value map							
R3	R2	R1	R0		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	*1) Power control register	OSC	VC	VR	VF	INTR	RR2	RR1	RR0
0	1	0	1	*2) Contrast control register	-	-	C5	C4	C3	C2	C1	C0
0	1	1	0	*3) Environment control register	-	-	DT1	DT0	DIRC	DIRS	EXT	ID
0	1	1	1	*4) Function control register	-	-	-	FG	CM	FL1	B1	B0

NOTE: "-" - Don't care

*1) **OSC**: internal oscillator ON (OSC = 1), OFF (OSC = 0) control bit
VC: voltage converter ON (VC = 1), OFF (VF = 1) control bit
VR: voltage regulator ON (VR = 1), OFF (VR = 0) control bit
VF: voltage follower ON (VF = 1), OFF (VF = 0) control bit
INTR: use the internal voltage regulating resisters ON (INTR = 1), OFF (INTR = 0) control bit
RR2 to RR0: internal voltage adjusting resisters set control register bits (refer to table 18)
*2) **C5 to C0**: electronic contrast control register bits. (refer to figure 21)
*3) **DT1, DT0**: duty select bits (refer to table 15)
DIRC, DIRS: common data direction (DIRC), segment data direction (DIRS) select bit (refer to table 12 and table 13)
EXT: DDRAM extended mode ON (EXT = 1), OFF (EXT = 0) control bit
ID: DDRAM / CGRAM / ICONRAM address increment (ID = 1), decrement (ID = 0) control bit
*4) **FG**: CGRAM full graphic mode ON (FG = 1), OFF (FG = 0) control bit
CM: center display mode ON (CM = 1), OFF (CM = 0) control bit
FL1: first line fix mode ON (FL1 = 1), OFF (FL1 = 0) control, during vertical shift
B1, B0: cursor attribute control bit

Return Home

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	-	-	-	-

Set DDRAM address to "00h" into the address counter. If the display position has shifted, it return to the original positions. When cursor or blinking is displayed on, bring the cursor to the left edge on first line of the display. The data in DDRAM does not change.

Display Control

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	D	CC	LC	REV

Display control bit ON / OFF instruction

D: Display ON / OFF Control
When D = "High", entire display is turned ON
When D = "Low", entire display is turned OFF, but display data is remained in DDRAM (default)

CC: Character Cursor ON / OFF Control Bit
When CC = "High", character cursor is turned ON.
When CC = "Low", character cursor is disappeared in current display (default).

LC: Line Cursor ON / OFF Control Bit
When LC = "High", line cursor is turned on according to the most significant 2-bits (ADDR[6], ADDR[5]) of current DDRAM address (ADDR [6:0]). When LC = "Low", line cursor is disappeared in current display (default)

REV: Black / White Reverse Display ON / OFF Control Bit
When REV= "High", all the display area except icon area are black / white reversed.
When REV= "Low", normal display status (default)

Power Save Mode

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	-	-	-	SLP

Power Save mode is used to making KS0040 sleep mode.

SLP: Sleep Mode ON / OFF Control Bit
When SLP = "High", sleep mode is set (default).
When SLP = "Low", sleep mode is reset.
(refer to "LOW POWER CONSUMPTION MODE" and "INITIALIZING & POWER SAVE MODE SETUP")

Contrast Increment / Decrement

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	-	-	-	CID

Contrast control register value increment / decrement instruction

CID: Contrast Increment / Decrement Enable Bit
When CID = “High”: contrast register value increased by 1 until 63.
When CID = “Low”: contrast register value decreased by 1 until 0.

Vertical Shift-up / down

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	-	-	CD	UD

Vertical dot-by-dot display shift-up / down instruction (refer to figure 14, 16)

CD: Character / Dot Shift Select Bit
When CD = "High": display shift-up / down by character is selected (It’s the same as 16-time dot shift).
When CD = "Low": display shift-up / down by dot is selected.

UD: Vertical Display Shift Direction Select
When UD = "High": display shift-up is performed.
When UD = "Low": display shift-down is performed.

Double Height Character

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	-	EN	DH1	DH0

Double height character instruction (refer to figure 15)

EN: Double Height Character Mode Enable Bit
When EN = "High": double height character mode is enabled.
When EN = "Low": double height character mode is disabled (default).

DH1, DH0: Double Height Character Line Select
When [DH1, DH0] = [Low, Low]: 1, 2-line becomes double height character
= [Low, High]: 2, 3-line becomes double height character
= [High, Low]: 3, 4-line becomes double height character
= [High, High]: 1 to 4-line becomes double height character

RAM Select / System Register Set

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	R3	R2	R1	R0

RAM selection (DDRAM / CGRAM / ICONRAM) or system register set instruction. R3 / R2 / R1 / R0: RAM or system register selection bits

Select bits	Selected RAM or registers	Data length / value map							
R3 R2 R1 R0		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0 0 0 0	DDRAM	1-byte (half-size font) 2-byte (full-size font)							
0 0 0 1	ICONRAM	1-byte							
1 0 0 0	CGRAM page0	2-byte							
1 0 0 1	CGRAM page1	2-byte							
1 0 1 0	CGRAM page2	2-byte							
1 0 1 1	CGRAM page3	2-byte							
1 1 0 0	CGRAM page4	2-byte							
1 1 0 1	CGRAM page5	2-byte							
1 1 1 0	CGRAM page6	2-byte							
1 1 1 1	CGRAM page7	2-byte							
0 1 0 0	Power control register	OSC	VC	VR	VF	INTR	RR2	RR1	RR0
0 1 0 1	Contrast control register	-	-	C5	C4	C3	C2	C1	C0
0 1 1 0	Environment control register	-	-	DT1	DT0	DIRC	DIRS	EXT	ID
0 1 1 1	Function control register	-	-	-	FG	CM	FL1	B1	B0

NOTE: "-" - Don't care
For writing 2-byte data into RAM, data write instruction must be performed twice.

OSC: oscillator circuit ON (OSC = "High"), OFF (OSC = "Low": default) control
VC / VR / VF: voltage converter / regulator / follower circuit ON (VC / VR / VF = "High"), OFF (VC / VR / VF = "Low": default) control
INTR: Use the internal voltage regulating resistors on (INTR = "High"), off (INTR = "Low": default) control bit
RR2~RR0: internal voltage adjusting resistors set control register bits ([0,0,0]: default). (refer to table 18)
C5 to C0: electronic contrast control register ([0, 0, 0, 0, 0, 0]: default) (refer to figure 21)
DT1, DT0: duty select register ([1, 1]: default) (refer to table 18)
DIRC, DIRS: common data shift direction (DIRC), segment data shift direction (DIRS) flag register ([0, 0]: default) (refer to table 12 and table 13)
EXT: DDRAM extended mode ON (EXT = "High"), OFF (EXT = "Low": default) control
ID: RAM address increment (ID = "High": default), decrement (ID = "Low") mode set
FG: CGRAM full graphic mode ON / OFF control register (FG = "Low": default). (refer to figure 18)
CM: center display mode ON / OFF control register (CM = "Low": default). (refer to figure 17)
FL1: first line fix mode, during vertical scroll instruction, ON / OFF control register (FL1 = "Low": default). (refer to figure 16)
B1, B0: character / line cursor attribute select register ([0, 0]: default) (refer to table 17)

RAM Address Set

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

DDRAM / CGRAM / ICONRAM address set instruction. Each RAM is selected by RAM select instruction.

Write Data

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	D7	D6	D5	D4	D3	D2	D1	D0

DDRAM / CGRAM / ICONRAM data or system register value write instruction. Each RAM and system register is selected by RAM select / system register set instruction. After write operation, the address is increased/decreased by 1 automatically, according to function control register set. When writing full-size character address in FCGROM to DDRAM, RAM data write instruction must be written twice, because the FCGROM address is 13-bits long. (refer to figure 15)

Read Data (8-bit Bus Mode MPU Interface only)

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	D7	D6	D5	D4	D3	D2	D1	D0

DDRAM / CGRAM / ICONRAM data or system register value read instruction. Each RAM and system register is selected by RAM select / system register set instruction. If you read RAM data after RAM address set instruction, you can get correct RAM data from the second. The first data would be incorrect, because there is no timing margin for transfer RAM data to output register. After write or read operation, the address is increased/decreased by 1 automatically, according to function control register set. When reading full size character address in FCGROM from DDRAM, RAM data read instruction must be executed twice, because the FCGROM address is 13-bits long. (refer to figure 15)

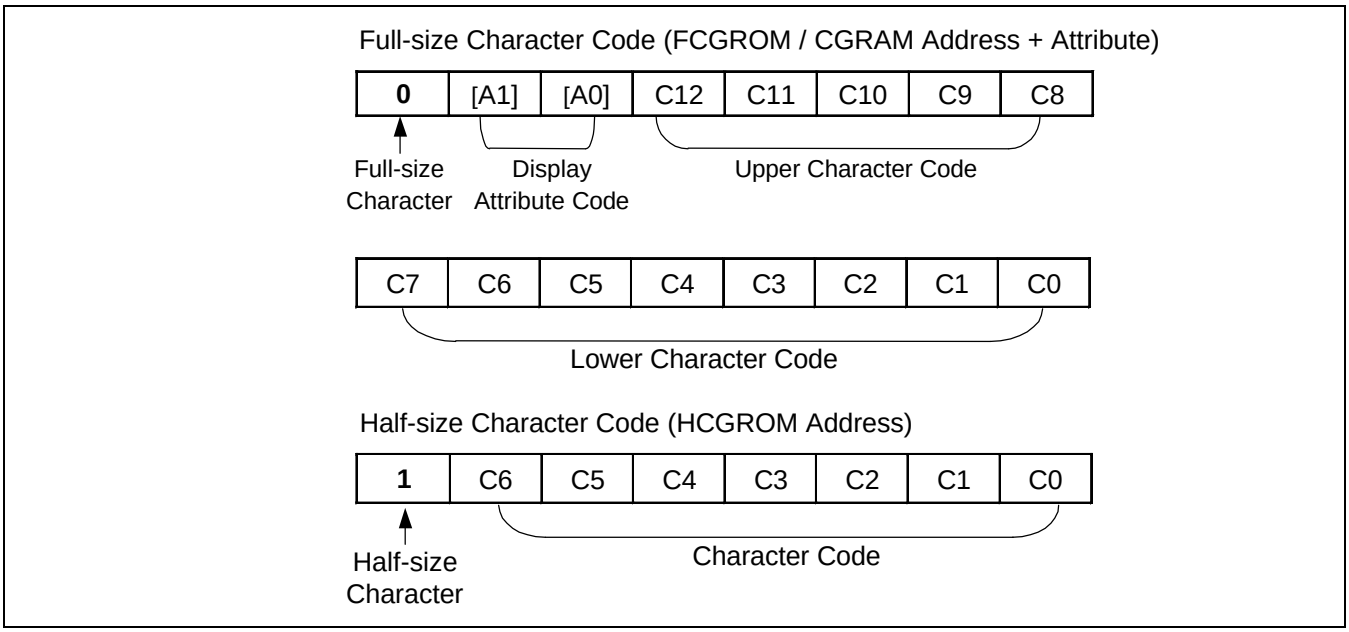


Figure 15. DDRAM Data (FCGROM / HCGROM / CGRAM Address) Format

Table 16. Display Attributes

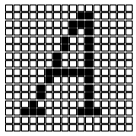
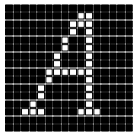
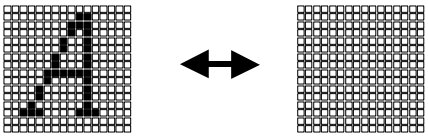
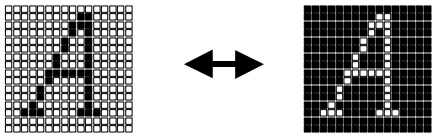
[A1] [A0]	Display state (when cursor / blink OFF)	
0 0	Normal display	
0 1	B/W reversed display	
1 0	Character blink mode 1	
1 1	Character blink mode 2	

Table 17 Cursor Attributes

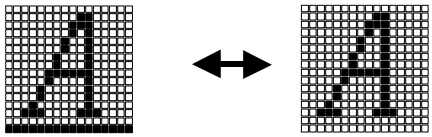
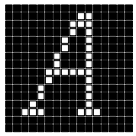
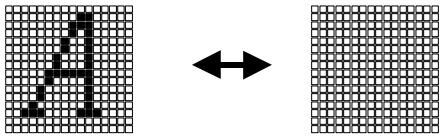
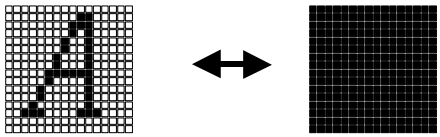
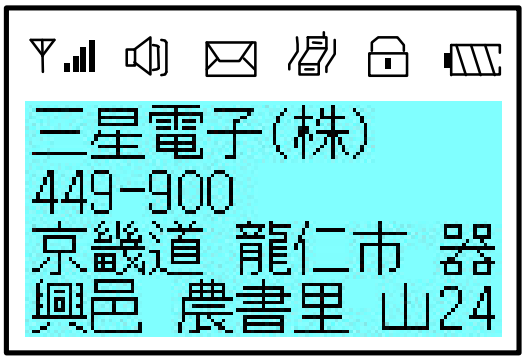
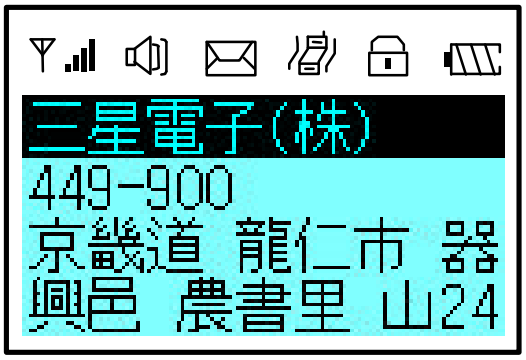
[B1] [B0]	Display state (at cursor position)	
0 0	Underline cursor	
0 1	B/W reverse cursor	
1 0	Blink cursor 1	
1 1	Blink cursor 2	

Table 18. The Relationship between Duty and Environment Set

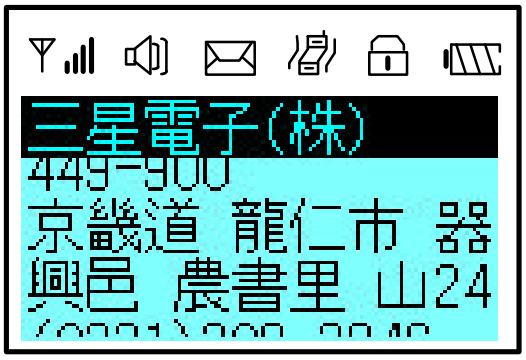
DT1 DT0	Duty	Bias	fosc (kHz)	Display line number
0 0	1/17	1/5	24.5	1-line display
0 1	1/33	1/7	47.6	2-line display
1 0	1/49	1/8	68.3	3-line display
1 1	1/65	1/9	93.7	4-line display



Normal Display
- Line Cursor (LC) OFF
- First Line Fix Mode (FL1) OFF
- Vertical Shift OFF



Normal Display & Line Cursor
- Line Cursor (LC) ON (B1, B0 = [0, 1])
- First Line Fix Mode (FL1) OFF
- Vertical Shift OFF

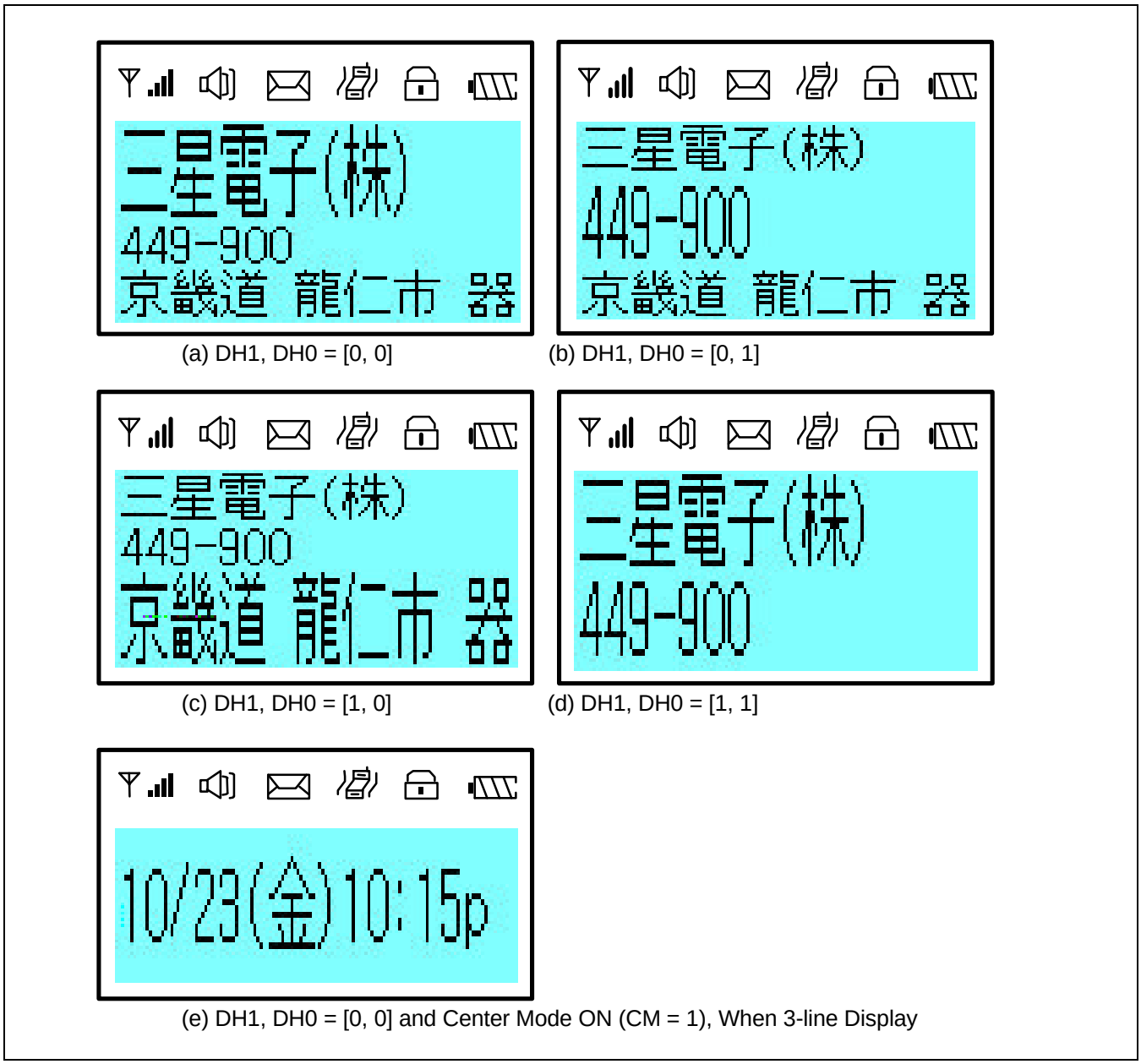


Vertical Shifted Display
(in First Line Fix Mode)
Line Cursor (LC) ON (B1, B0 = [0, 1])
- First Line Fix Mode (FL1) ON
- Vertical Shift-up by Dot 6 times



Vertical Shifted Display
(in First Line Fix Mode)
- Line Cursor (LC) ON (B1,B0 = [0, 1])
- First Line Fix Mode (FL1) ON
- Vertical Shift Up by Dot 16 times
  or Vertical Shift-up by Character once

Figure 16. The Examples of Vertical Shift and First Line Fix Mode



(a) DH1, DH0 = [0, 0]

(b) DH1, DH0 = [0, 1]

(c) DH1, DH0 = [1, 0]

(d) DH1, DH0 = [1, 1]

(e) DH1, DH0 = [0, 0] and Center Mode ON (CM = 1), When 3-line Display

Figure 17. The Examples of Double Height Character Display

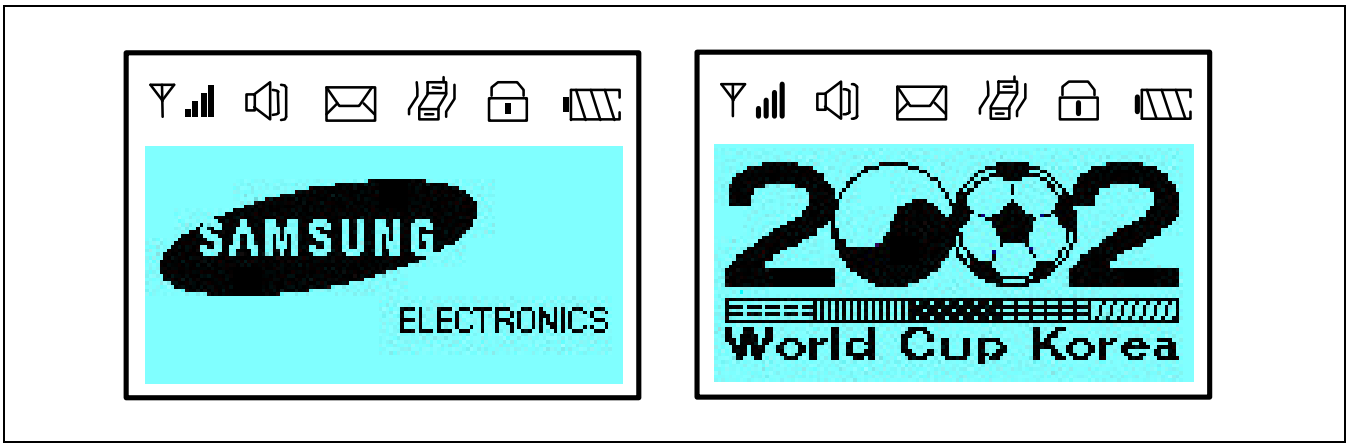


Figure 18. The Examples of Full Graphic Mode Display (FG = 1)

INITIALIZING & POWER SAVE MODE SETUP

HARDWARE RESET

When RESET pin = "Active (rising or falling)", KS0040 can be initialized the following state.

Return Home

Address counter = 00H

Control Display ON / OFF Instruction

D = 0: display OFF
CC, LC = [0, 0]: character / line cursor OFF
REV = 0: reverse display OFF (normal display)

Power Save Mode Instruction

SLP = 1: sleep mode ON

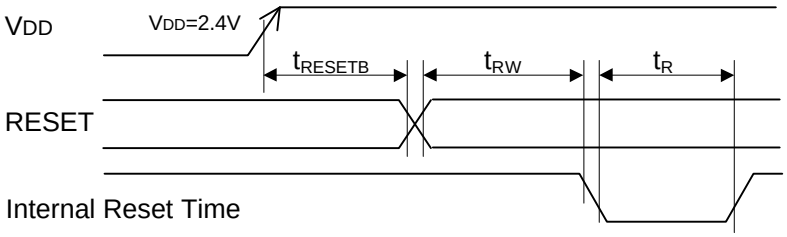
RAM Select Instruction

R3 to R0 = [0, 0, 0, 0]: DDRAM is selected.

System Register Set Instruction

OSC = 0: oscillator OFF
VC, VR, VF = [0, 0, 0]: voltage converter / regulator / follower OFF
INTR = 0: internal voltage regulating resister OFF
RR2 to RR0 = [0, 0, 0]: Internal voltage adjusting resistors set control register value are set to 000.
C5 to C0= [0, 0, 0, 0, 0, 0]: Electronic contrast control register values are set to 00H.
DT1, DT0 = [1, 1]: 4-line display mode
DIRC = 0: normal direction of common outputs (COM1 to COM64, COMI1 (COMI2))
DIRS = 0: normal direction of segment outputs (SEGI1, SEGI2, SEG1 to SEG128, SEGI3, SEGI4)
EXT = 0: Normal DDRAM mode is selected.
ID = 1: RAM address increment condition
FG = 0: CGRAM full graphic mode OFF
CM = 0: center display mode OFF
FL1 = 0: first line fix mode OFF
B1, B0 = [0, 0]: under line cursor attribute is selected.

NOTE**:** If initialization is not done by RESET pin, unstable condition might result. So, for initializing the RESET input pin must be active at first.

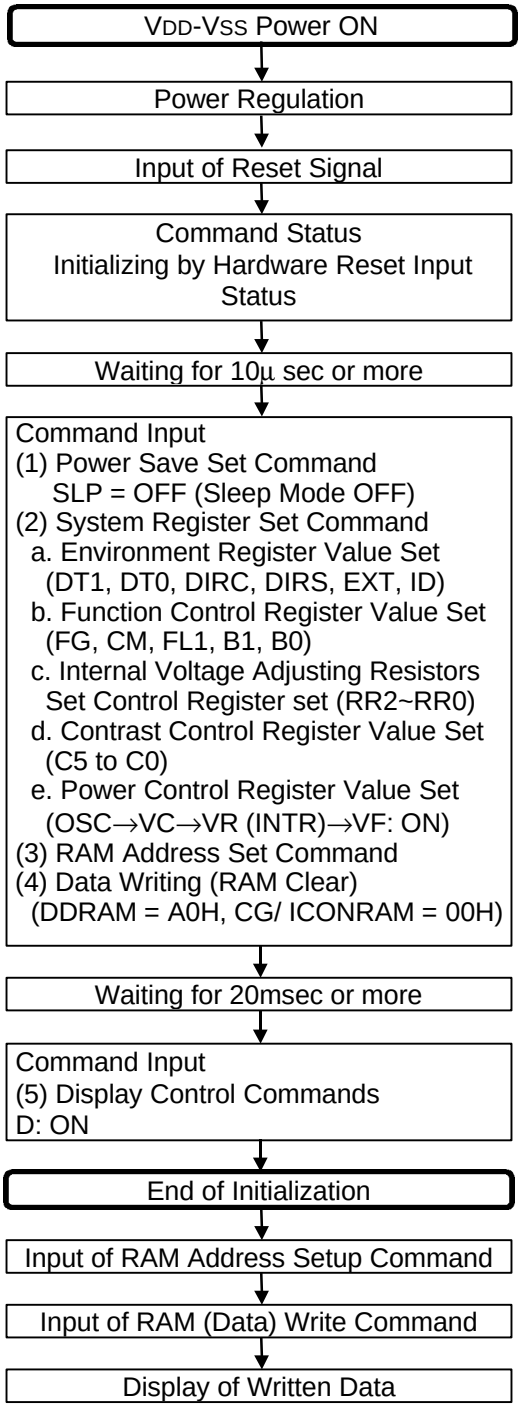


Reset Start Time	t_{RESETB}	50ns
Reset Pulse Width	t_{RW}	1.0µs
Reset Time	t_R	1.0µs

Figure 19. Reset Timing

NOTE: t_{RW} indicates the minimum RESET duration for activating internal reset signal.
t_R indicates reset completion time of internal circuit from the edge of the internal reset signal.

INITIALIZING BY INSTRUCTION



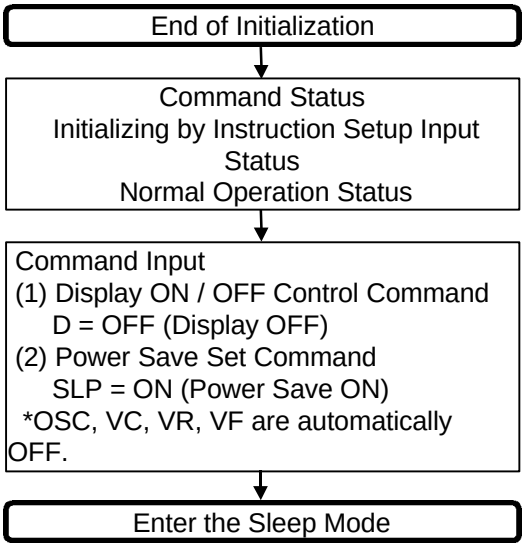
NOTE: Commands (3) and (4) initialize the RAM.
The non-display area must satisfy the following conditions (for RAM clear).

DDRAM: Write the A0H data. (Half character flag "1" and space character code "20H": "1" "0100000")
CGRAM: Write the 00H data (blank data)
ICONRAM: Write the 00H data (off data)

As the RAM data is unstable during reset signal input (after power ON), blank data must be written. If not, unexpected display may result.

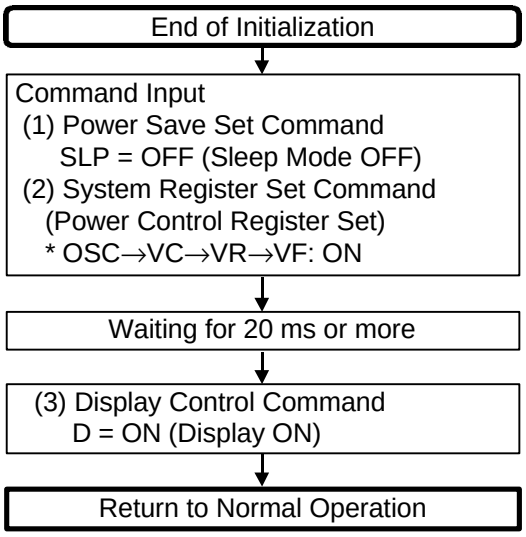
SLEEP MODE SET OR RELEASE BY INSTRUCTION

Sleep Mode Setting



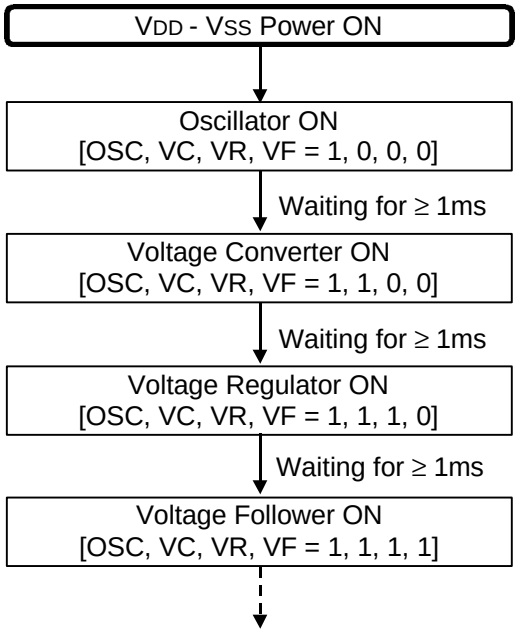
Internal voltage regulating resistor control bit (INTR) and voltage adjusting resistors set control register bits (RR2 - RR0) are not changed in sleep mode.

Sleep Mode Releasing

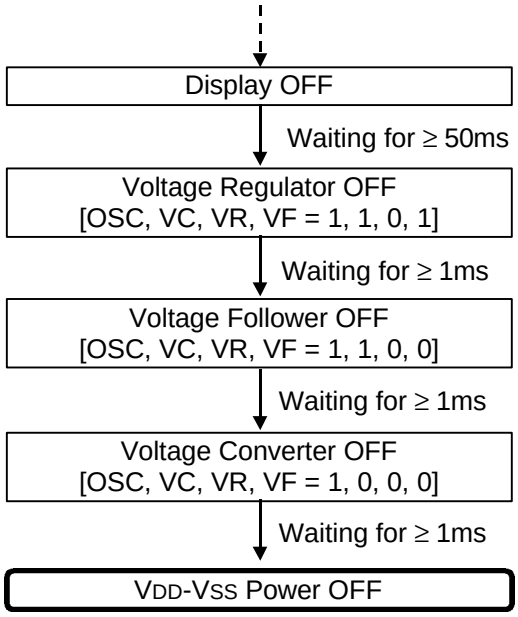


RECOMMENDATION OF POWER ON / OFF SEQUENCE

Power ON Sequence (Power Control Register Set)



Power OFF Sequence



LCD DRIVING POWER SUPPLY CIRCUIT

This Power Supply circuit generating voltages to drive LCD consists of voltage converter, voltage regulator, and voltage follower. Voltage converter boosts up logic voltage (V_{DD}) 2, 3 and 4 times and this boosted voltage (V_{OUT}) is delivered to the voltage regulator. Voltage regulator adjusts V0 between V_{OUT} and V_{SS} and this adjusted voltage is sent to the voltage follower. V_{LCD} voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the voltage follower for increasing drive capability. Power Supply circuit is controlled by the Power Control instruction. There can be eight combination states according to instruction sets (VC, Vr and VF). Table 19 shows useful combinations which are recommended, and the remaining combination states are impractical, not recommended to be used.

Table 19. Recommended Power Supply Combination

VC VR VF	Voltage converter	Voltage regulator	Voltage follower	VOUT	VO,VR	V1, V2, V3, V4
1 1 1	Enable	Enable	Enable	Internal voltage output	Used for voltage adjustment	Internal voltage output
0 1 1	Disable	Enable	Enable	External voltage input	Used for voltage adjustment	Internal voltage output
0 0 1	Disable	Disable	Enable	Open	VO: External voltage input VR: open	Internal voltage output
0 0 0	Disable	Disable	Disable	Open	VO: External voltage input VR: open	External voltage input

NOTE**:** SEC recommendation is to use only the case listed above table.

VOLTAGE CONVERTER

This circuit boosts up the electric potential between VDD and VSS to 2, 3 or 4 times toward positive side and boosted voltage come out through VOUT terminal.

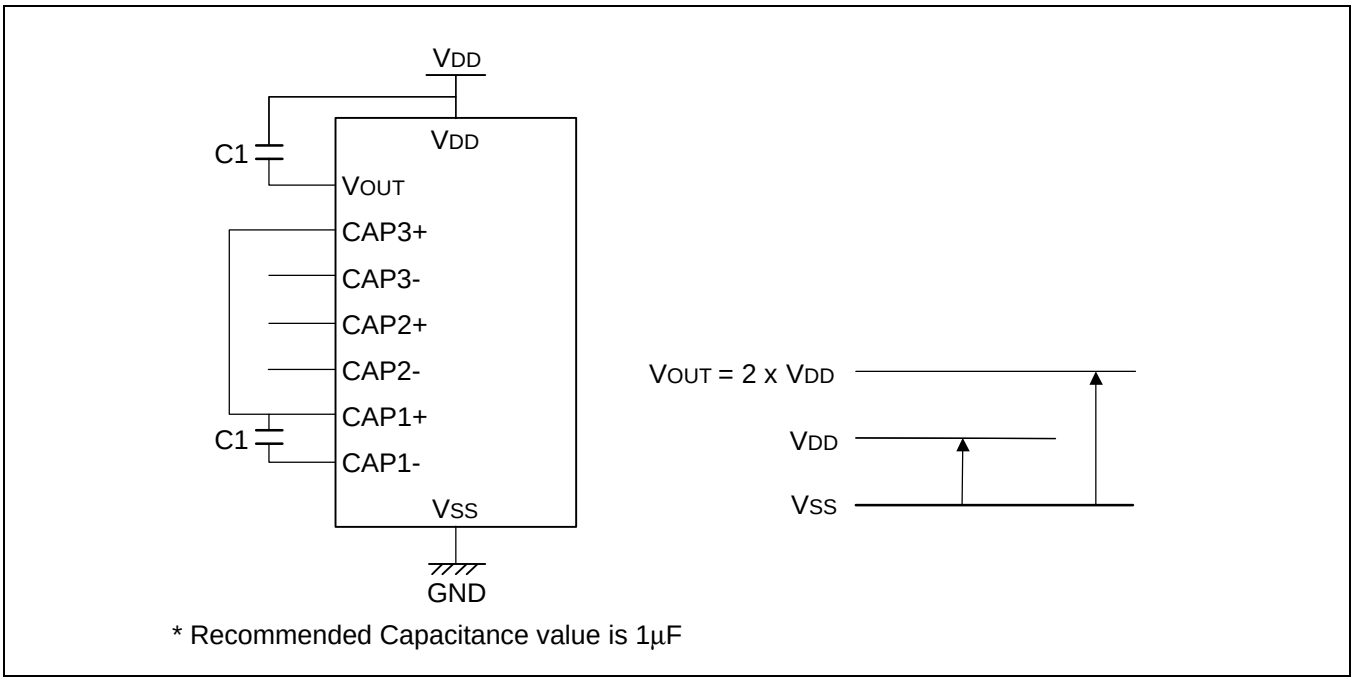


Figure 20. Two Times Boosting

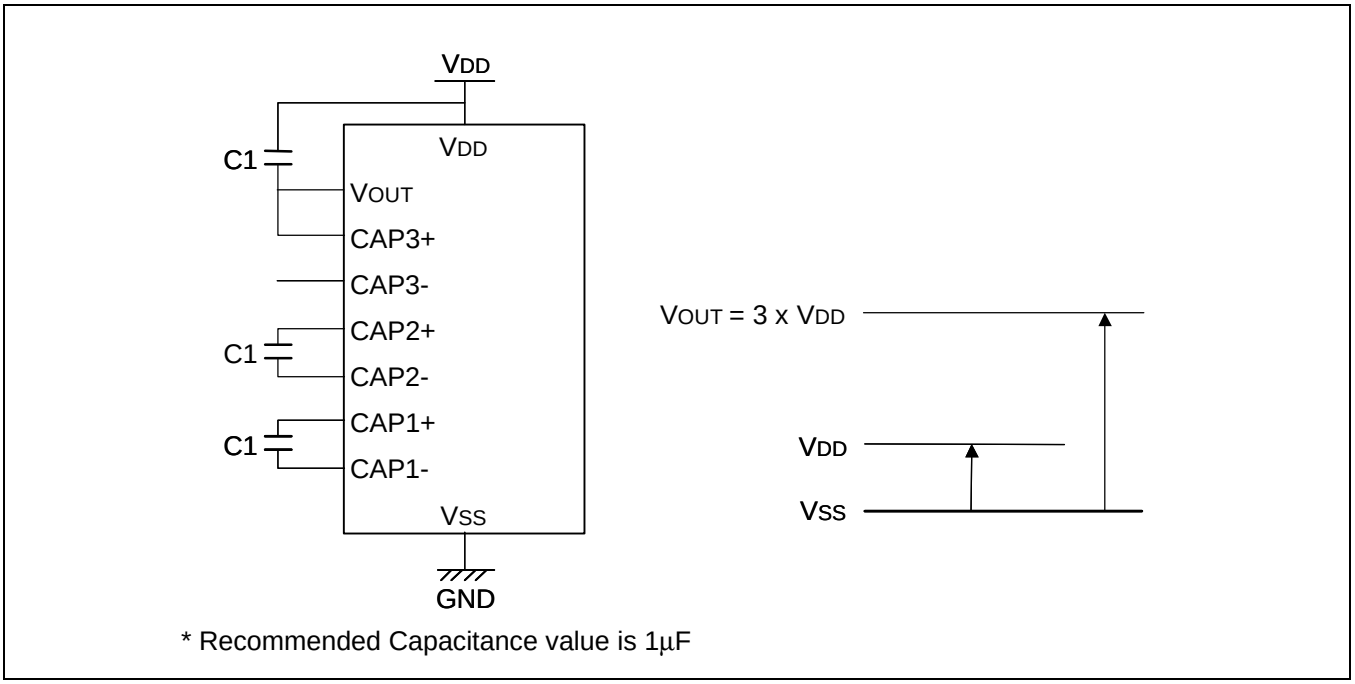


Figure 21. Three Times Boosting

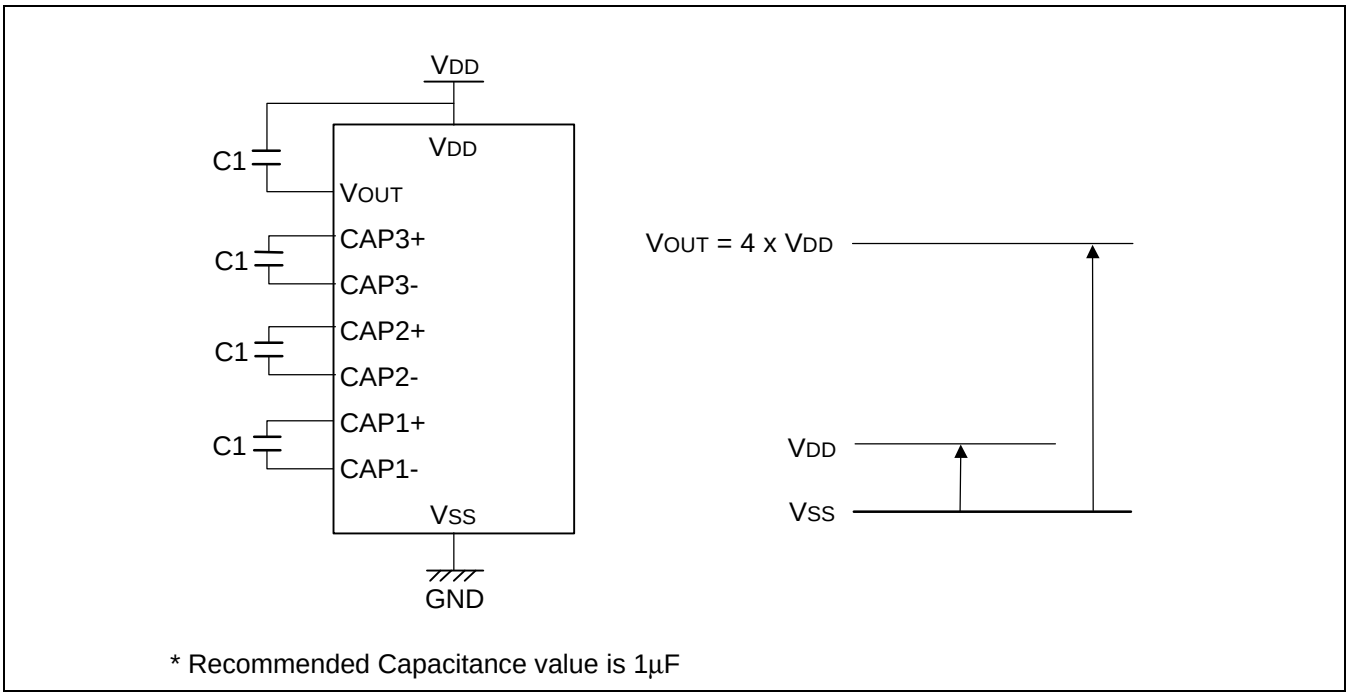


Figure 22. Four Times Boosting

VOLTAGE REGULATOR

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator. The Voltage Regulator determines V0 LCD driver voltage by adjusting resistor Ra and Rb within the range of |V0| < |V_{OUT}|. This V0 is determined by equation (1), where Ra and Rb are internal or external resistors and V_{REF} is determined by equation (2) as the voltage source of the IC. The electric potential of V_{REF} is set to one of 64 levels by setting 6-bit reference voltage register.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \ [V] \qquad \text{------ (1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{300}\right) \times Vs \ [V] \qquad \text{------- (2)}$$

where α = value of 6-bit reference voltage register (0 to 63)
when REF = "High", Vs = V_{DD}
REF = "Low", Vs = V_{REF} (internal reference voltage) = 2V

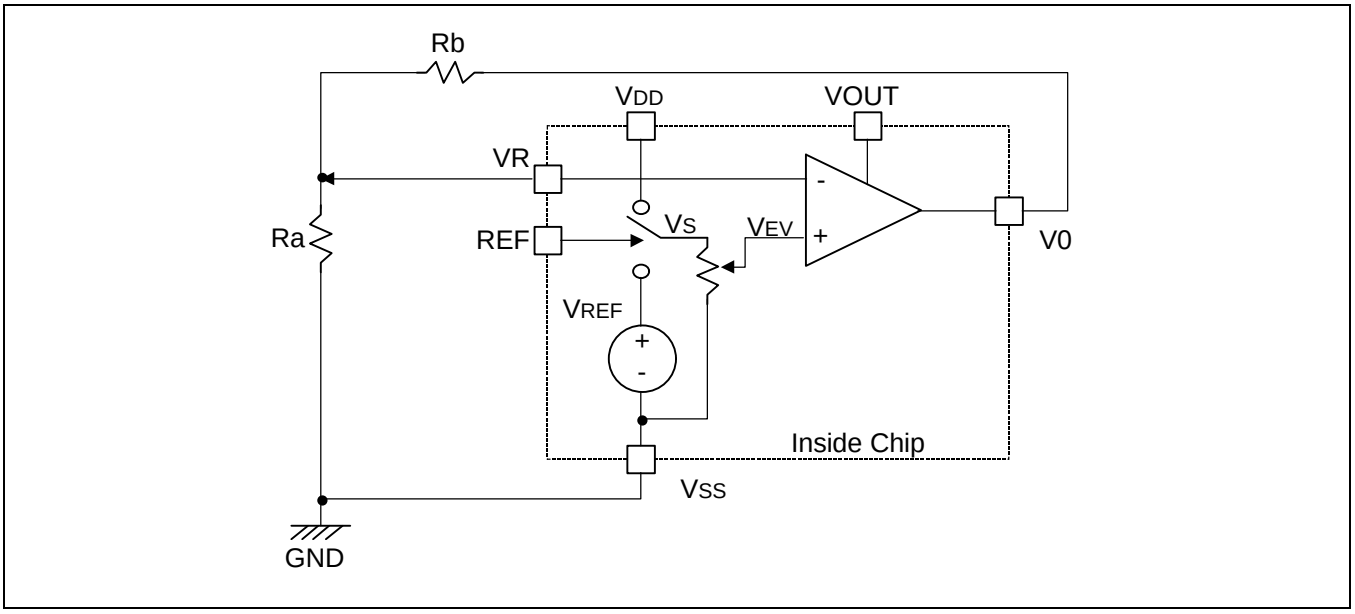


Figure 23. Voltage Regulator Circuit

When Using Internal Resistors, Ra and Rb (INTR = "High")

When INTR bit is set to "High", resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 20. Internal Rb / Ra Ratio Depending on 3-bit Data (RR2 RR1 RR0)

	3-bit data settings (RR2 RR1 RR0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1+(Rb / Ra)	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers at Ta = 25 °C (temperature coefficient = -0.05%/°C).

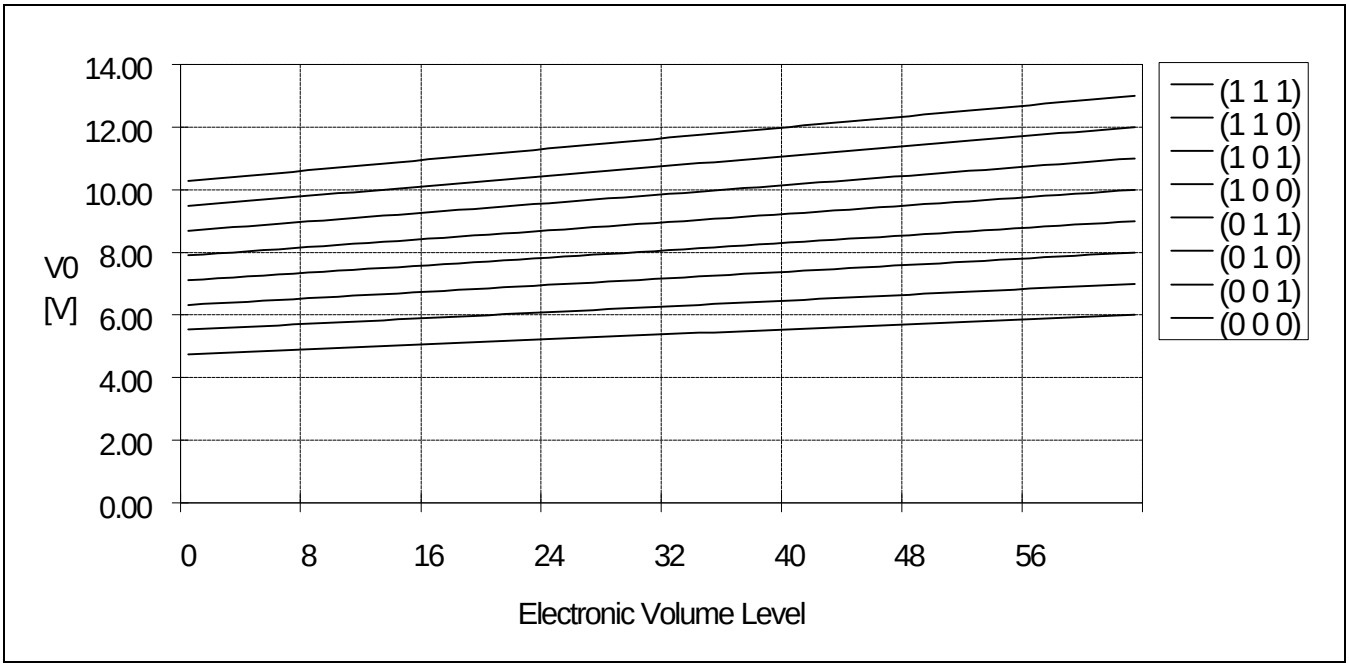


Figure 24. Electronic Volume Level (Temperature Coefficient = -0.05% / °C)

Table 21. The Relationship between Electronic Volume Constant, α, and 6-bit Voltage Reference Register (C5, C4, C3, C2, C1, C0)

C5	C4	C3	C2	C1	C0	α
1	1	1	1	1	1	63
1	1	1	1	1	0	62
. .	. .	. .	. .	. .	. .	. .
0	0	0	0	0	1	1
0	0	0	0	0	0	0

Table 22. The Change Ratio of V_{REF} and V0 by α is as Following Table

(REF = L, [RR2, RR1, RR0] = [1, 0, 0], Ta = 25°C)

	α								
	0	**1**	**- - -**	**30**	**31**	**32**	**- - -**	**62**	**63**
V0	7.90	7.93	-	8.90	8.93	8.97	-	9.97	10.00

When Using External Resistors, Ra and Rb (INTR = "Low")

When INTR bit is set to "Low", it is necessary to connect external regulator resistor Ra between VR and V_{SS}, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 1, 1, 1, 1, 1)
3. Maximum current flowing Ra, Rb = 1μA

From equation (1)

$$V0 = 10\ [V] = \left(1 + \frac{Rb}{Ra}\right) \times V_{REF} \qquad \text{------ (2)}$$

From equation (2)

$$V_{REF} = \left(1 - \frac{0}{300}\right) \times Vs = Vs = 2V \text{ or } V_{DD} \qquad \text{------ (3)}$$

where $\alpha = 63$
Vs = 2V or V_{DD}

From requirement 3.

$$\frac{10}{Ra + Rb} = 1\ [\mu A] \quad \text{------ (4)}$$

From equations (2), (3) and (4)

A. When Vs = 2V (REF = "Low")
Ra = 2 [MΩ]
Rb = 8 [MΩ]

B. When Vs = V_{DD} = 3V (REF = "High")
Ra = 3 [MΩ]
Rb = 7 [MΩ]

LCD BIAS RESISTOR & FOLLOWER

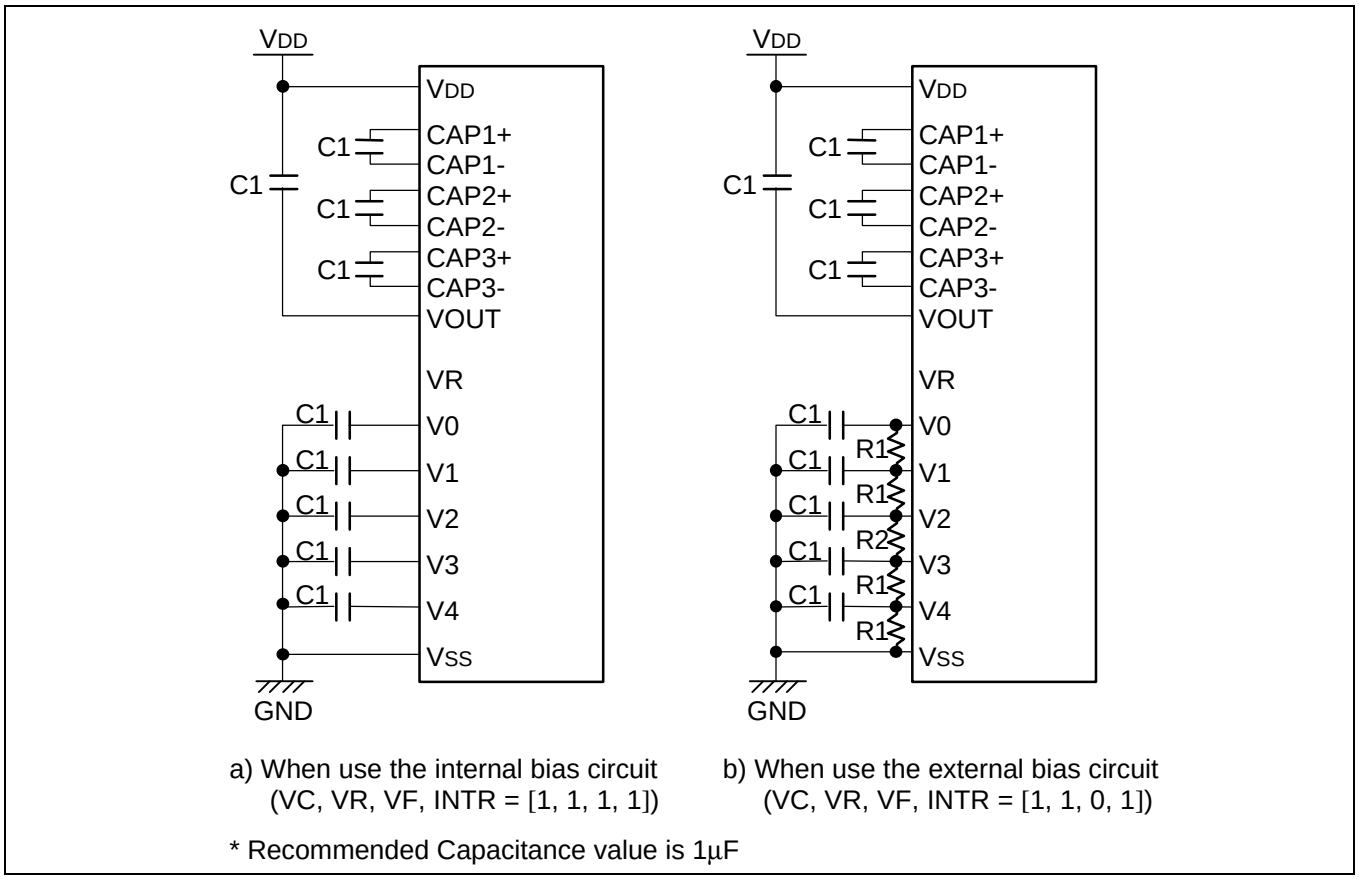


Figure 25. LCD Bias Circuit

Table 23. Duty Select Input & Internal Bias Circuit

DT1	DT0	Duty	Internal bias
Low	Low	1/17	1/5
Low	High	1/33	1/7
High	Low	1/49	1/8
High	High	1/65	1/9

USE THE EXTERNAL POWER SUPPLY

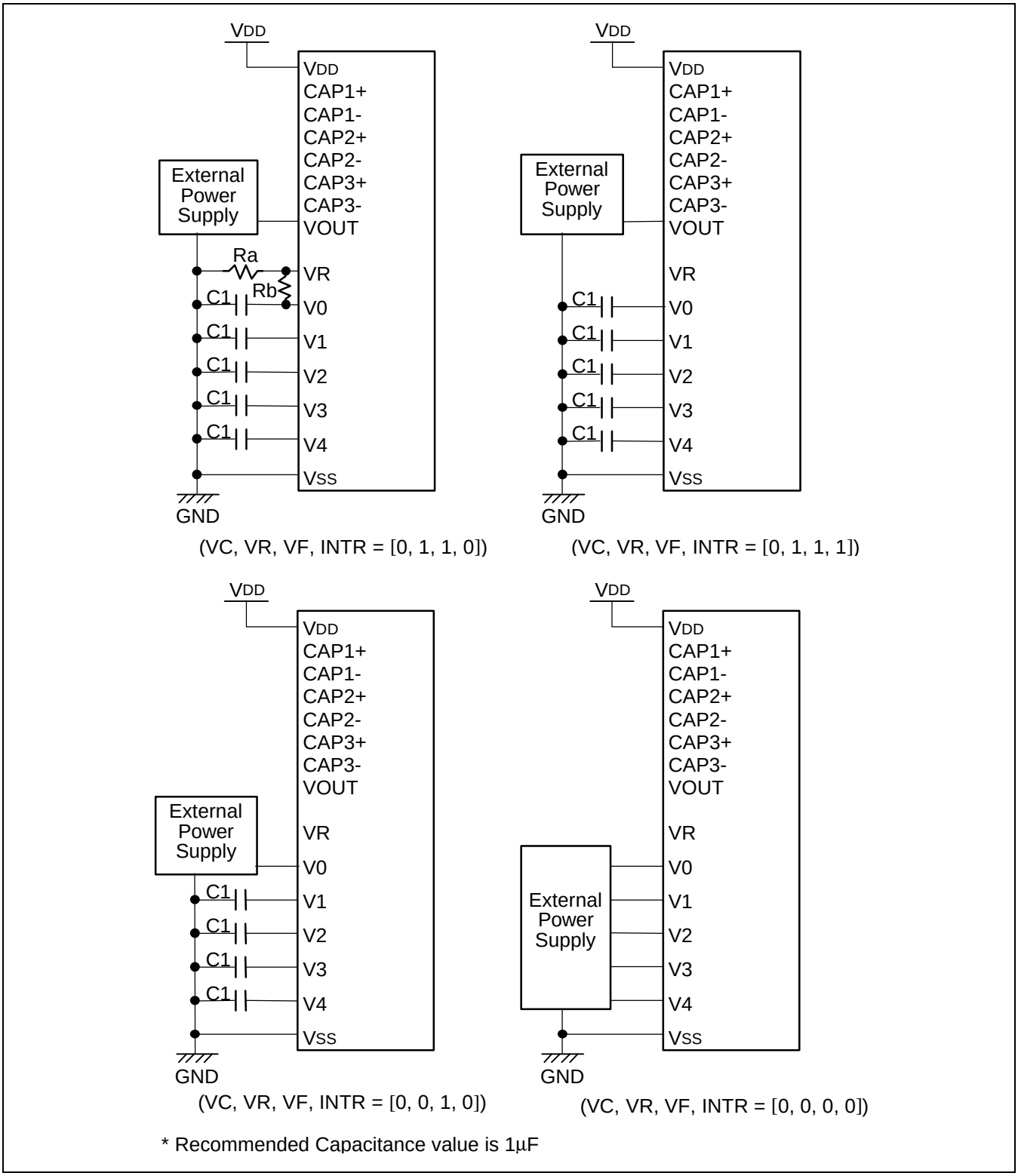


Figure 26. When External Power Supply is used

APPLICATION INFORMATION

MPU INTERFACE METHOD

Parallel Interfacing with 8080-series Microprocessors

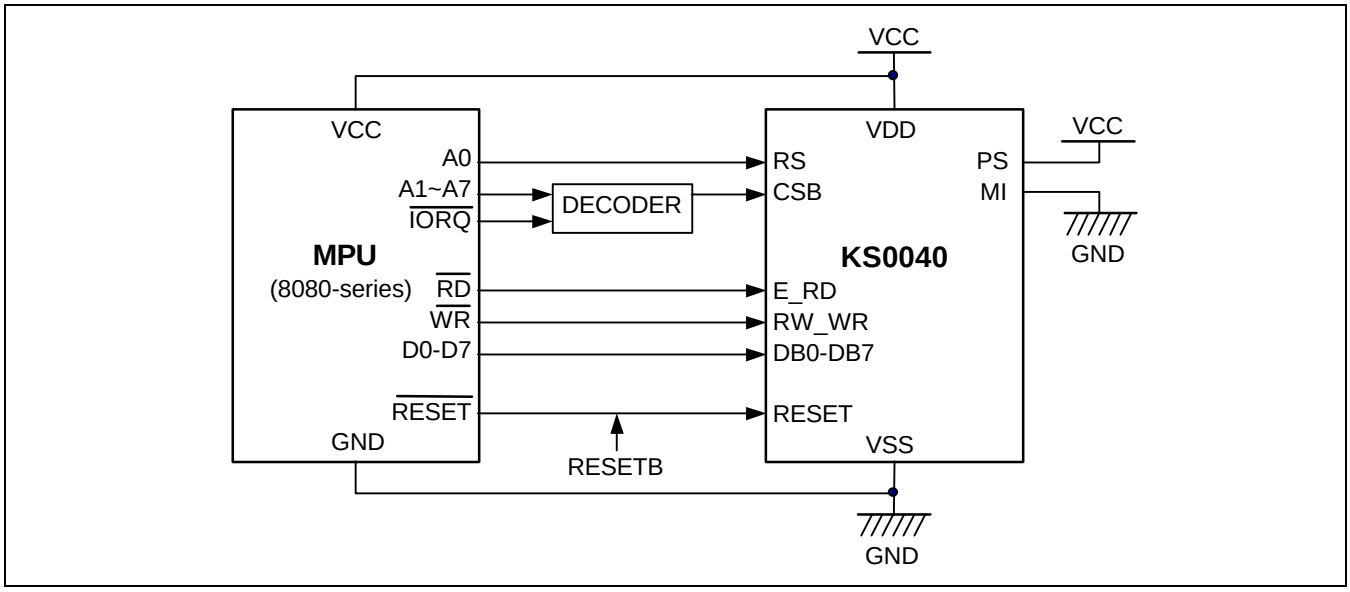


Figure 27. 8080-series MPU Interface

Parallel Interfacing with 6800-series Microprocessors

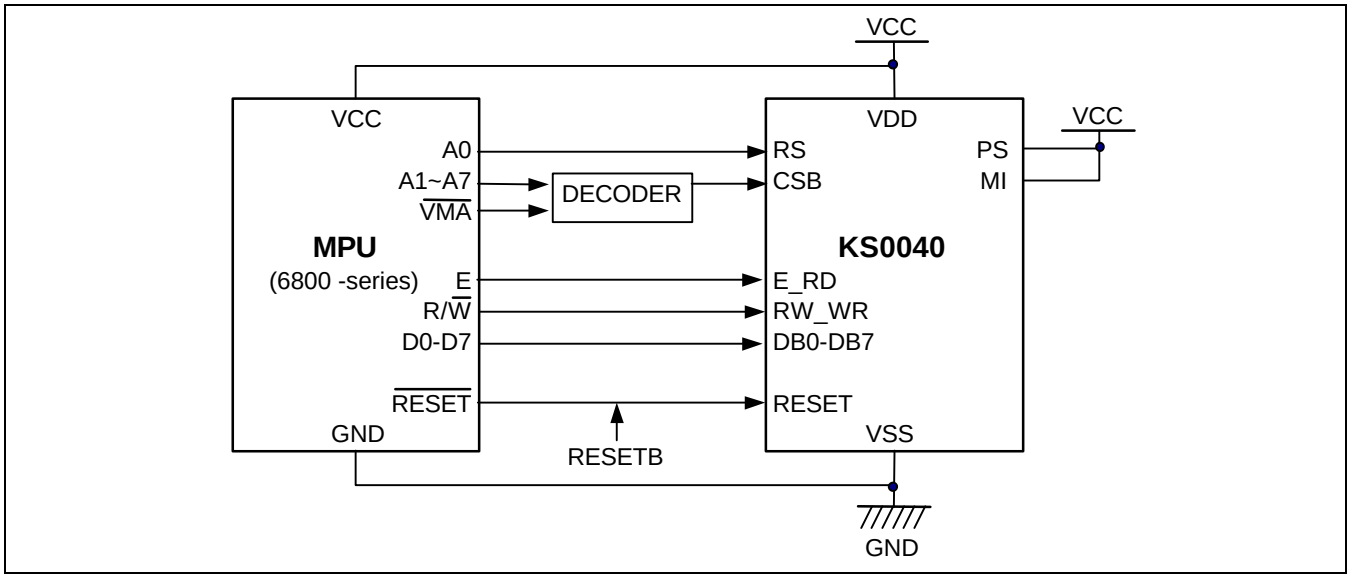


Figure 28. 6800-series MPU Interface

Clock Synchronized Serial Interfacing with any Microprocessors

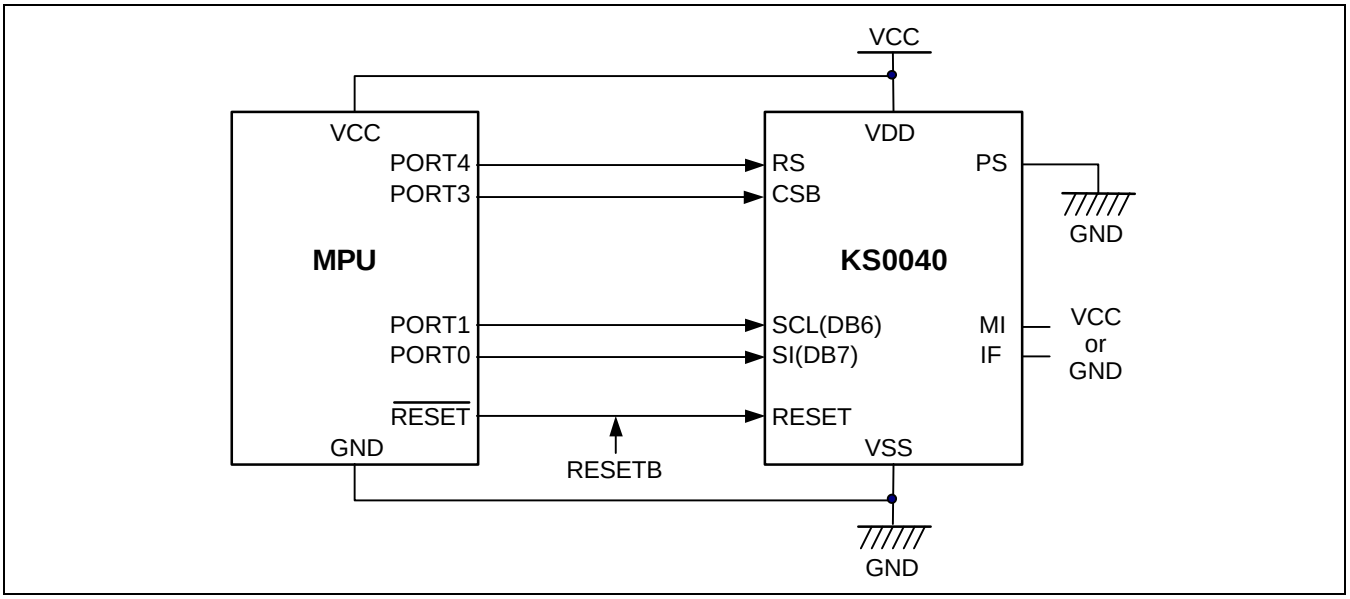


Figure 29. 4-Pin Serial Interface

LCD PANEL CONNECTION METHOD (1/65 DUTY CONFIGURATION)

Chip Bottom & Lower View (DIRS = 0, DIRC = 0)

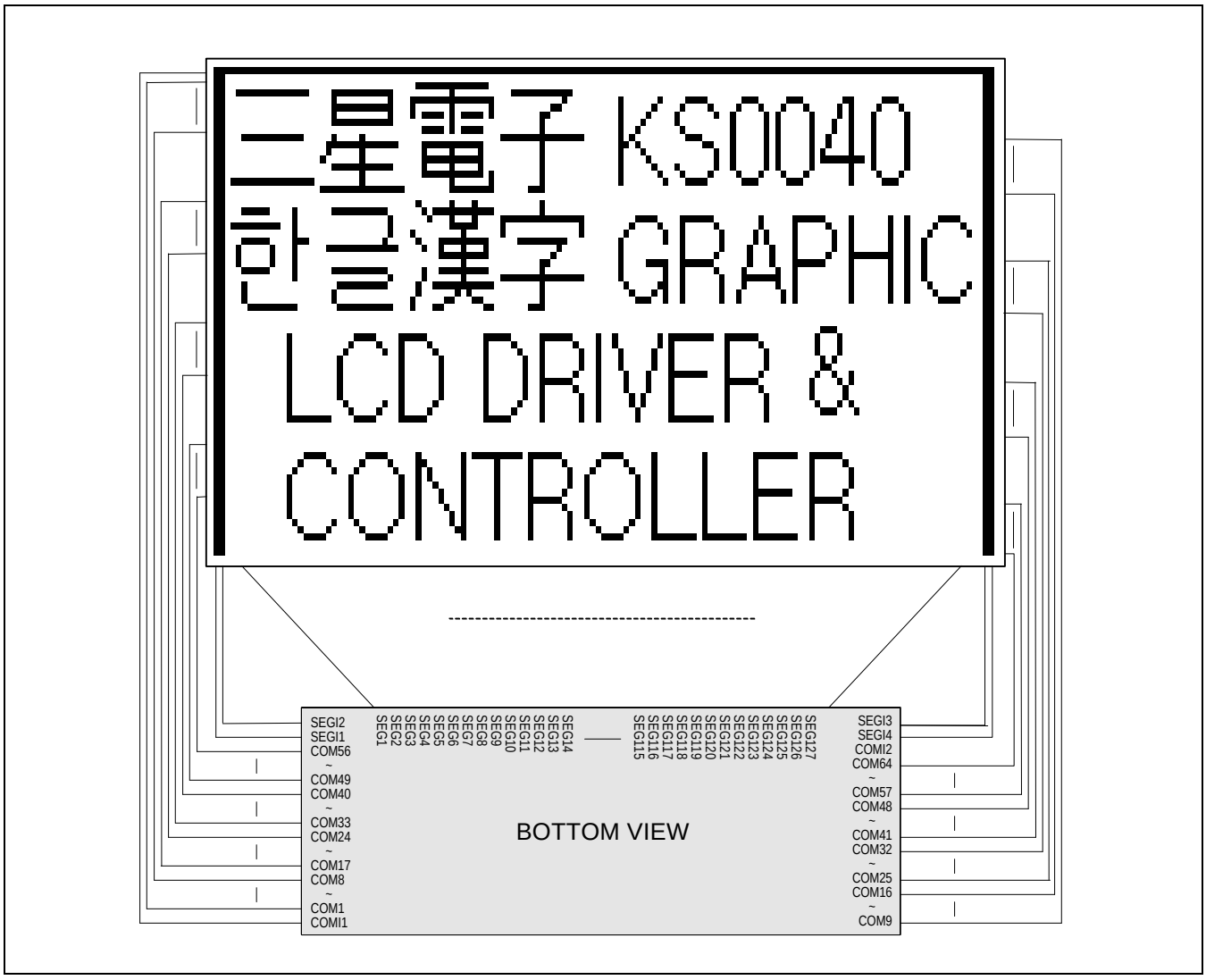


Figure 30. Chip Bottom & Lower View (DIRS = 0, DIRC = 0)

Chip Bottom & Upper View (DIRS = 1, DIRC = 1)

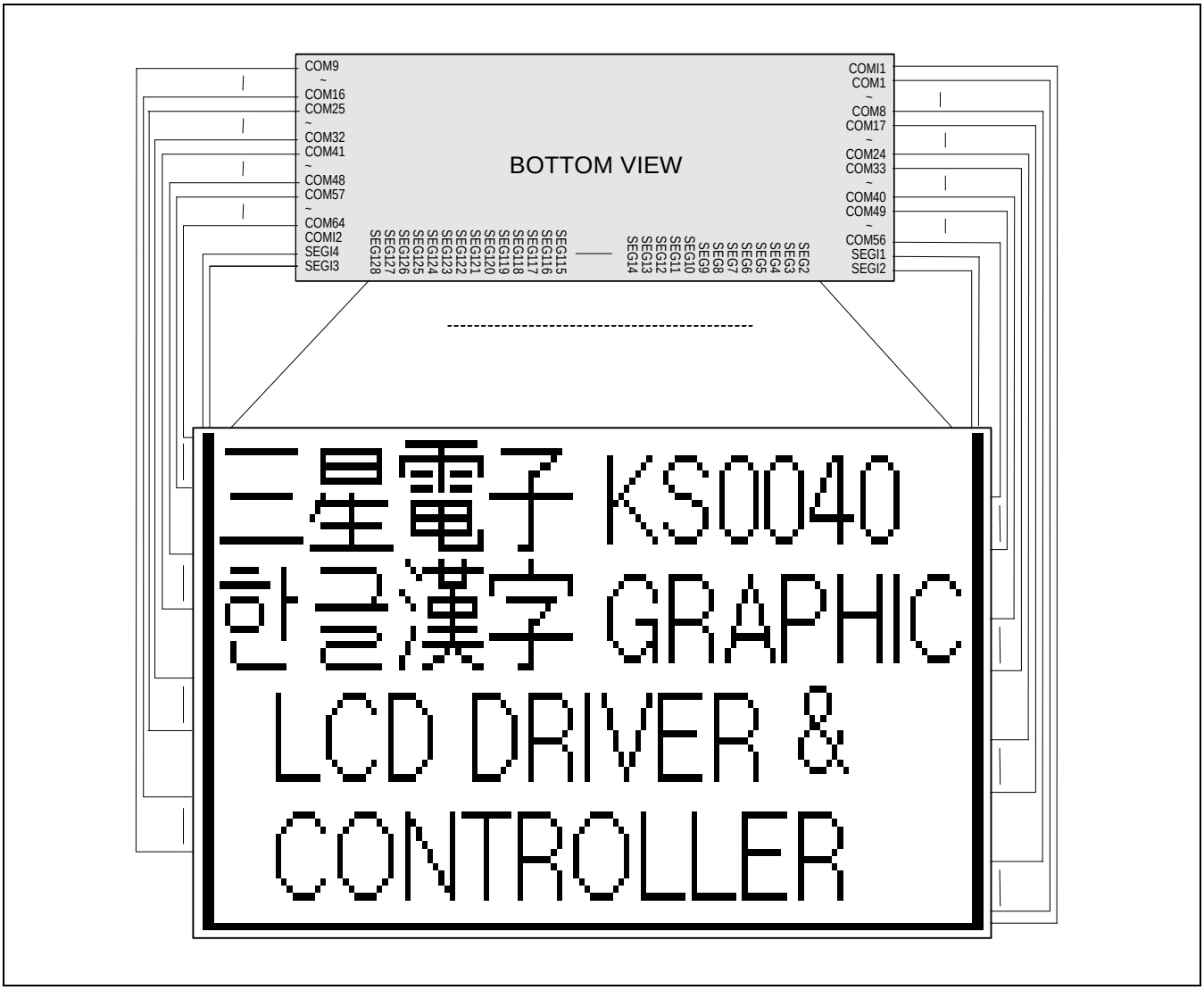


Figure 31. Chip Bottom & Lower View (DIRS = 1, DIRC = 1)

Chip Top & Lower View (DIRS = 1, DIRC = 0)

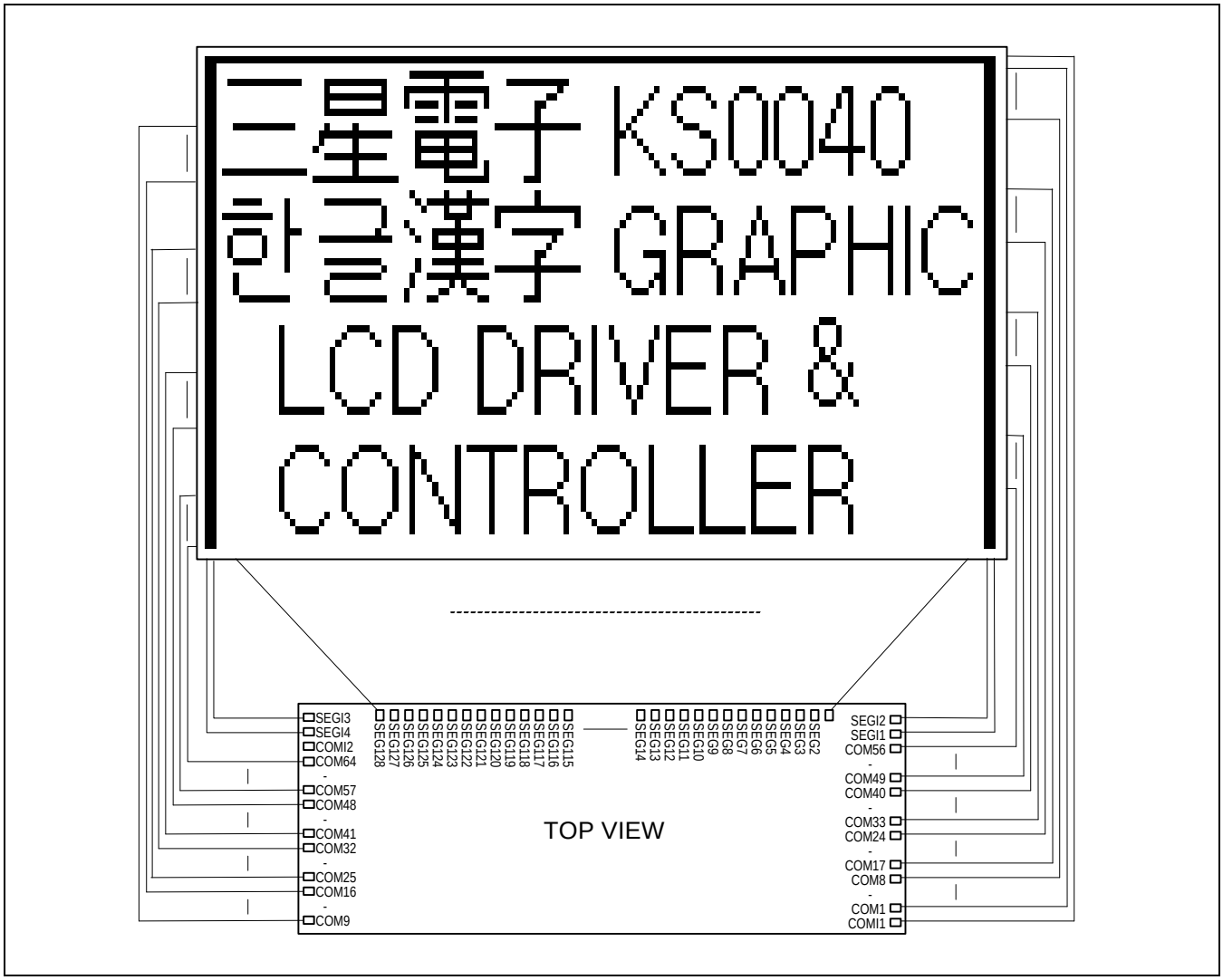


Figure 32. Chip Top & Lower View (DIRS = 1, DIRC = 0)

Chip Top & Upper View (DIRS = 0, DIRC = 1)

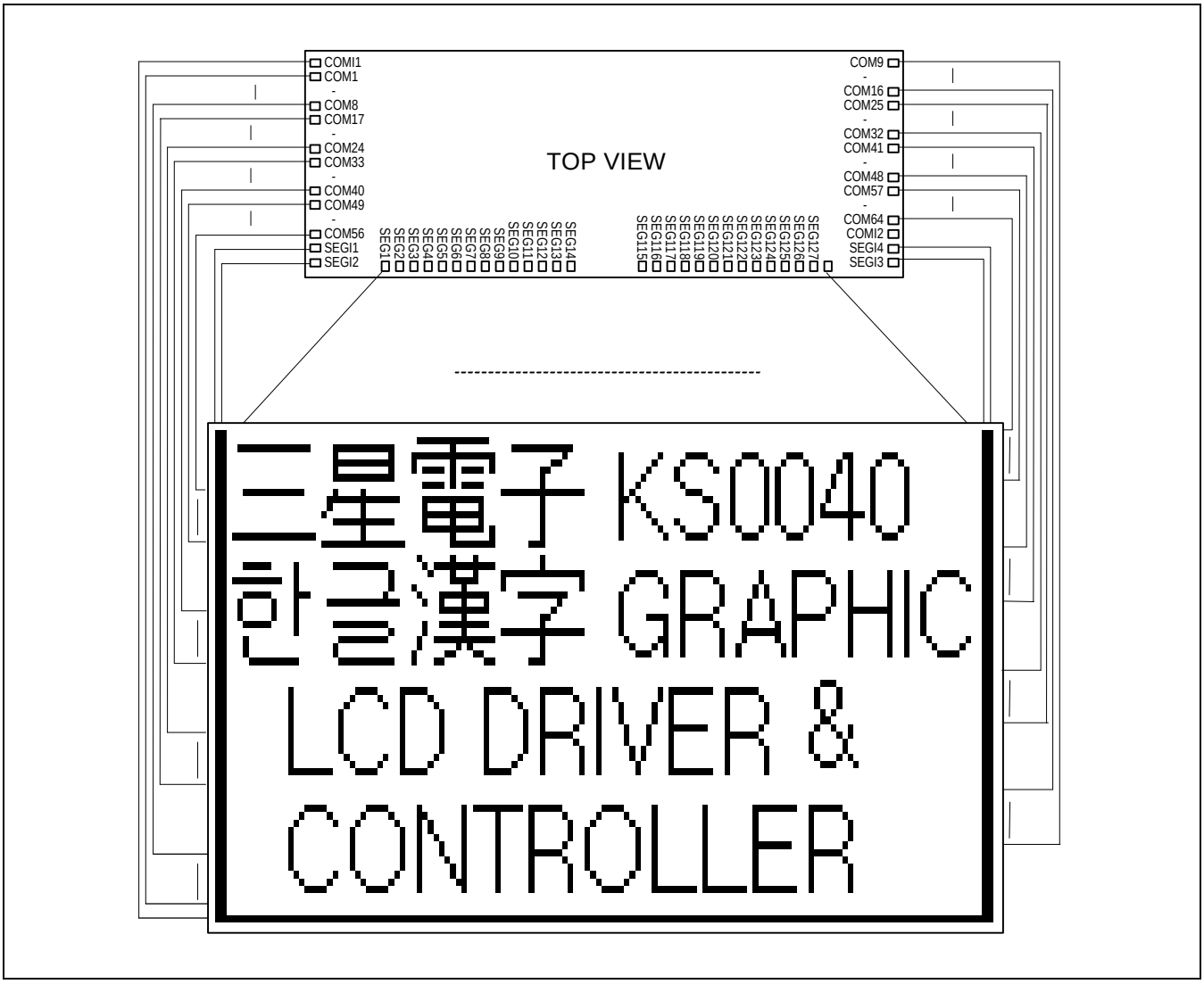
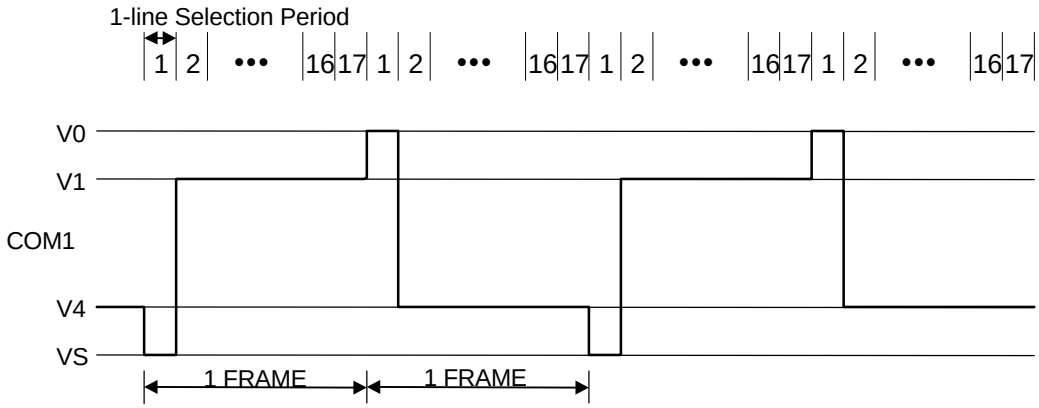


Figure 33. Chip Top & Lower View (DIRS = 0, DIRC = 1)

FRAME FREQUENCY

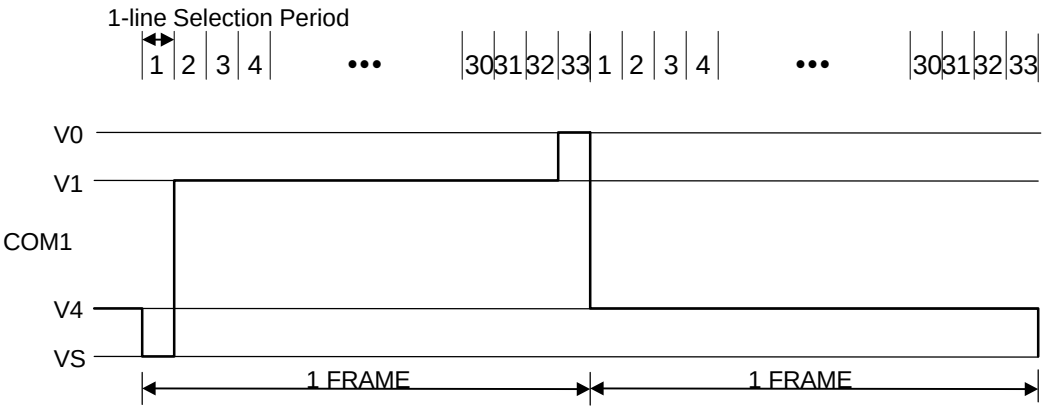
1/17 Duty (DT1, DT0 = [0, 0])



1-line Selection Period = 17 Clock Pulses
One Frame = 17 x 17 x 40.8μs = 11.8ms (1 Clock=40.8μs at fosc=24.5kHz)
Frame Frequency = 1 / 11.8ms = 85Hz

Figure 34. Frame Frequency (1/17 Duty)

1/33 Duty (DT1, DT0 = [0, 1])



1-line Selection Period = 17 Clock Pulses
One Frame = 17 x 33 x 21.0μs = 11.8ms (1 Clock=21.0μs at fosc=47.6kHz)
Frame Frequency = 1 / 11.8ms = 85Hz

Figure 35. Frame Frequency (1/33 Duty)

1/49 Duty (DT1, DT0 = [1, 0])

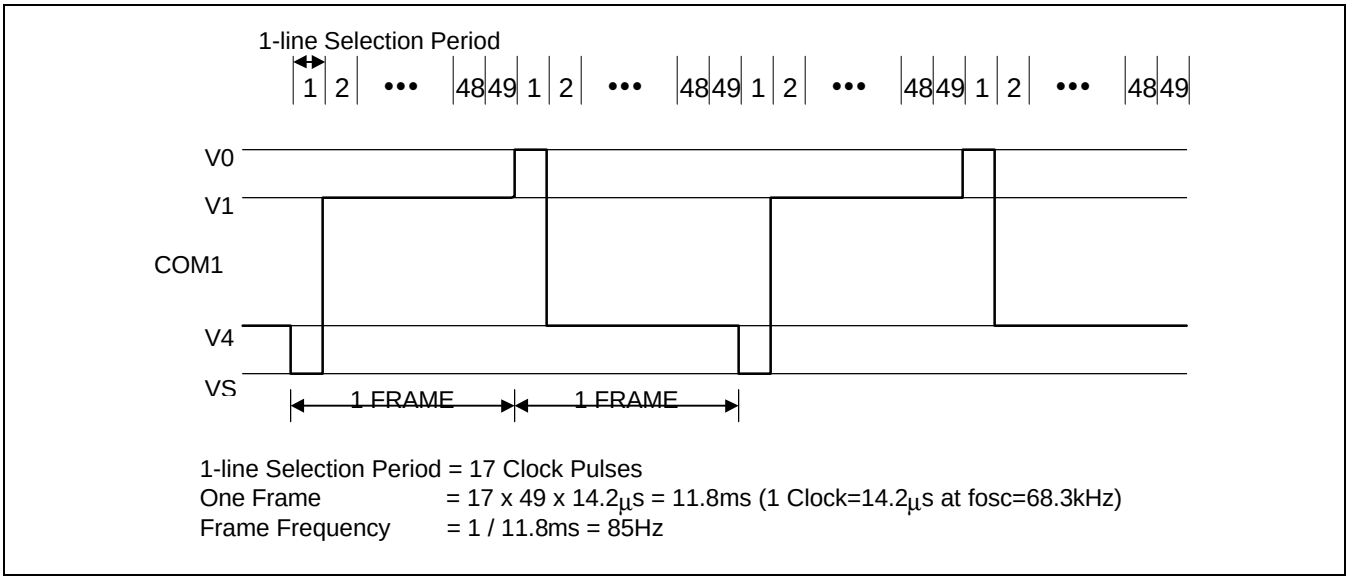


Figure 36. Frame Frequency (1/49 Duty)

1/65 Duty (DT1, DT0 = [1, 1])

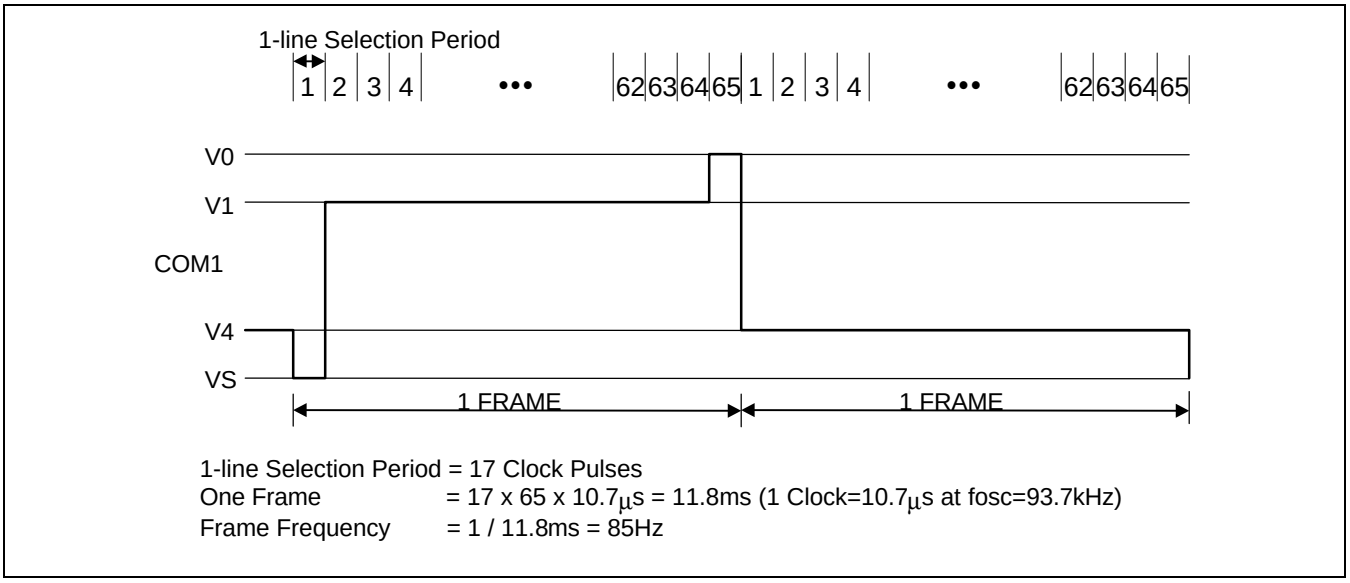


Figure 37. Frame Frequency (1/65 Duty)

Table 24. Duty Select Input & Display Window Size

DT1	DT0	Duty	Display window size
Low	Low	1/17	1-line x 8-character
Low	High	1/33	2-line x 8-character
High	Low	1/49	3-line x 8-character
High	High	1/65	4-line x 8-character

MAXIMUM ABSOLUTE RATE

Table 25. Absolute Maximum Ratings

Characteristics	Symbol	Value	Unit
Power supply voltage (1)	V_{DD}	-0.3 to +7.0	V
Power supply voltage (2)	V0, V_{OUT}	-0.3 to + 15	V
Input voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating temperature	T_{OPR}	-30 to +85	°C
Storage temperature	T_{STG}	-55 to +125	°C

NOTE1: All the voltage levels are based on VSS = 0V

NOTE2: Voltage greater than above may damage to the circuit

Voltage level: $V_{OUT} \geq V0 \geq VSS$. (V_{LCD} = V0 - VSS)

Voltage level: $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{SS}$

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Table 26. DC Characteristics

(V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	2.4	-	3.6	V
Supply current (V_{DD} = 3V, Ta = 25°C)	I_{DD1}	Display operation (checker pattern) V0 = 9V without load No access from MPU	-	-	180	µA
	I_{DD2}	Sleep operation without load Oscillator OFF	-	-	5	
	I_{DD3}	Access operation from MPU fcyc = 200kHz	-	-	500	
Input voltage	V_{IH}	-	0.8V_{DD}	-	V_{DD}	V
	V_{IL}	-	V_{SS}	-	0.2V_{DD}	
Input leakage current	I_{LEAK}	V_{IN} = 0V to V_{DD}	-1	-	1	µA
R_{ON} resistance	R_{COM}	Io = ± 50µA	-	-	5	kΩ
	R_{SEG}	Io = ± 50µA	-	-	10	
Frame frequency	f_{FR}	V_{DD} = 3V, Ta = 25°C	60	85	110	Hz
External clock frequency	f_{CK}	Display of 1-line mode	-	24.5	-	kHz
		Display of 2-line mode	-	47.6	-	
		Display of 3-line mode	-	68.3	-	
		Display of 4-line mode	-	93.7	-	
Voltage converter V_{DD} 2 / 3 / 4 times	V_{OUT}	Ta = 25°C, C = 1µF without load	95	99	-	%
Voltage regulator reference voltage	V_{REF}	Ta = 25°C, REF = L, VR pad EV value (α) = 63 without load	1.94	2.0	2.06	V
LCD driving voltage	V_{LCD}	V_{LCD} = V0 – V_{SS}	4.0	-	13.0	

Table 26. DC Characteristics (Continued)

(V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DD}	-	3.6	-	5.5	V
Supply current (V_{DD} = 5V, Ta = 25°C)	I_{DD1}	Display operation (checker pattern) V0 = 9V without load no access from MPU	-	-	280	µA
	I_{DD2}	Sleep operation without load oscillator OFF	-	-	10	
	I_{DD3}	Access operation from MPU fcyc = 200kHz	-	-	1000	
Input voltage	V_{IH}	-	0.8V_{DD}	-	V_{DD}	V
	V_{IL}	-	V_{SS}	-	0.2V_{DD}	
Input leakage current	I_{LEAK}	V_{IN} = 0V to V_{DD}	-1	-	1	µA
R_{ON} resistance	R_{COM}	Io = ± 50µA	-	-	5	KΩ
	R_{SEG}	Io = ± 50µA	-	-	10	
Frame frequency	f_{FR}	V_{DD} = 5V, Ta = 25°C	60	85	110	Hz
External clock frequency	f_{CK}	Display of 1-line mode	-	24.5	-	kHz
		Display of 2-line mode	-	47.6	-	
		Display of 3-line mode	-	68.3	-	
		Display of 4-line mode	-	93.7	-	
*Voltage converter V_{DD} 2 / 3 times	V_{OUT}	Ta = 25°C, C = 1µF without load	95	99	-	%
Voltage regulator reference voltage	V_{REF}	Ta = 25°C, REF = L, VR pad EV value (α) = 63 without load	1.94	2.0	2.06	V
LCD driving voltage	V_{LCD}	V_{LCD} = V0 – V_{SS}	4.0	-	13.0	

NOTE**:** When power supply (VDD) range is 3.6V to 5.5V, the 4 times boosting is not allowed.

AC CHARACTERISTICS

6800-series MPU Interface & Write Instruction

Table 27. AC Characteristics (6800-series Write Instruction)

Condition	Characteristic	Symbol	Min.	Typ.	Max.	Unit
V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C	E cycle time	t_C	650		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	E pulse width high	t_{WH}	450	-	-	
	E pulse width low	t_{WL}	150	-	-	
	RS and CSB setup time	t_{SU1}	60	-	-	
	RS and CSB hold time	t_{H1}	30	-	-	
	DB setup time	t_{SU2}	100	-	-	
	DB hold time	t_{H2}	50	-	-	
V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C	E cycle time	t_C	350		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	E pulse width high	t_{WH}	250	-	-	
	E pulse width low	t_{WL}	100	-	-	
	RS and CSB setup time	t_{SU1}	40	-	-	
	RS and CSB hold time	t_{H1}	10	-	-	
	DB setup time	t_{SU2}	40	-	-	
	DB hold time	t_{H2}	10	-	-	

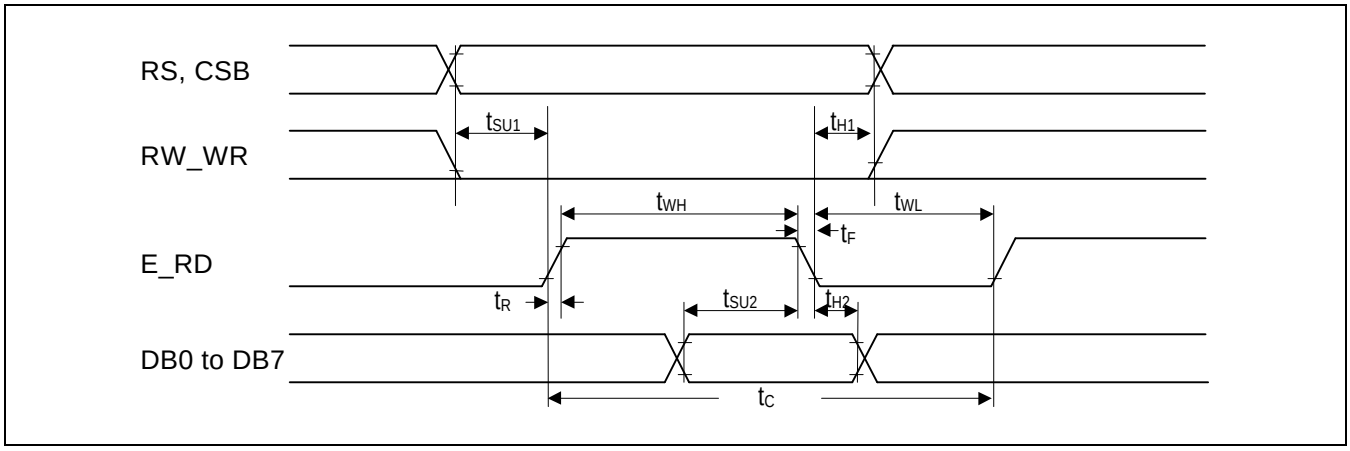


Figure 17. Write Bus Mode Timing (6800-series MPU Interface)

8080-series MPU Interface & Write Instruction

Table 28. AC Characteristics (8080-series Write Instruction)

Condition	Characteristic	Symbol	Min.	Typ.	Max.	Unit
V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C	WR cycle time	t_C	650		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	WR pulse width high	t_{WH}	150	-	-	
	WR pulse width low	t_{WL}	450	-	-	
	RS and CSB setup time	t_{SU1}	60	-	-	
	RS and CSB hold time	t_{H1}	30	-	-	
	DB setup time	t_{SU2}	100	-	-	
	DB hold time	t_{H2}	50	-	-	
V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C	WR cycle time	t_C	350		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	WR pulse width high	t_{WH}	100	-	-	
	WR pulse width low	t_{WL}	250	-	-	
	RS and CSB setup time	t_{SU1}	40	-	-	
	RS and CSB hold time	t_{H1}	10	-	-	
	DB setup time	t_{SU2}	40	-	-	
	DB hold time	t_{H2}	10	-	-	

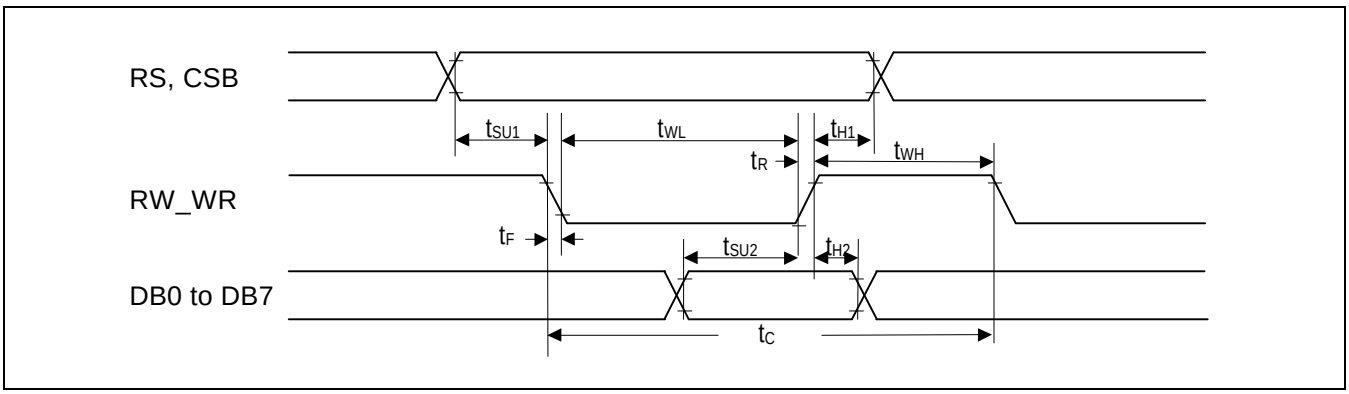


Figure 18. Write Bus Mode Timing (8080-series MPU Interface)

6800-series MPU Interface & Read Instruction

Table 29. AC Characteristics (6800-series Read Instruction)

Condition	Characteristic	Symbol	Min.	Typ.	Max.	Unit
V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C	E cycle time	t_C	650		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	E pulse width high	t_{WH}	450	-	-	
	E pulse width low	t_{WL}	150	-	-	
	RS and CSB setup time	t_{SU}	60	-	-	
	RS and CSB hold time	t_H	30	-	-	
	DB output delay time	t_D	-	-	360	
	DB output hold time	t_{DH}	20	-	-	
V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C	E cycle time	t_C	350		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	E pulse width high	t_{WH}	250	-	-	
	E pulse width low	t_{WL}	100	-	-	
	RS and CSB setup time	t_{SU}	40	-	-	
	RS and CSB hold time	t_H	10	-	-	
	DB output delay time	t_D	-	-	120	
	DB output hold time	t_{DH}	10	-	-	

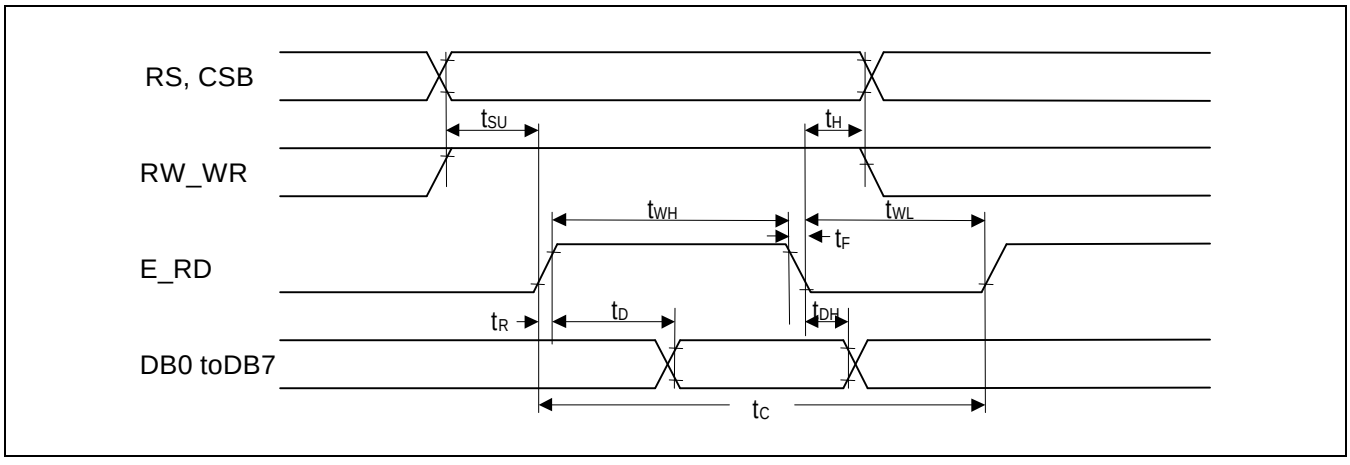


Figure 19. Read Bus Mode Timing (6800-series MPU Interface)

8080-series MPU Interface & Read Instruction

Table 30. AC Characteristics (8080-series Read Instruction)

Condition	Characteristic	Symbol	Min.	Typ.	Max.	Unit
V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C	RD cycle time	t_C	650		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	RD pulse width high	t_{WH}	150	-	-	
	RD pulse width low	t_{WL}	450	-	-	
	RS and CSB setup time	t_{SU}	60	-	-	
	RS and CSB hold time	t_H	30	-	-	
	DB output delay time	t_D		-	360	
	DB output hold time	t_{DH}	20	-	-	
V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C	RD cycle time	t_C	350		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	RD pulse width high	t_{WH}	100	-	-	
	RD pulse width low	t_{WL}	250	-	-	
	RS and CSB setup time	t_{SU}	40	-	-	
	RS and CSB hold time	t_H	10	-	-	
	DB output delay time	t_D	-	-	120	
	DB output hold time	t_{DH}	10	-	-	

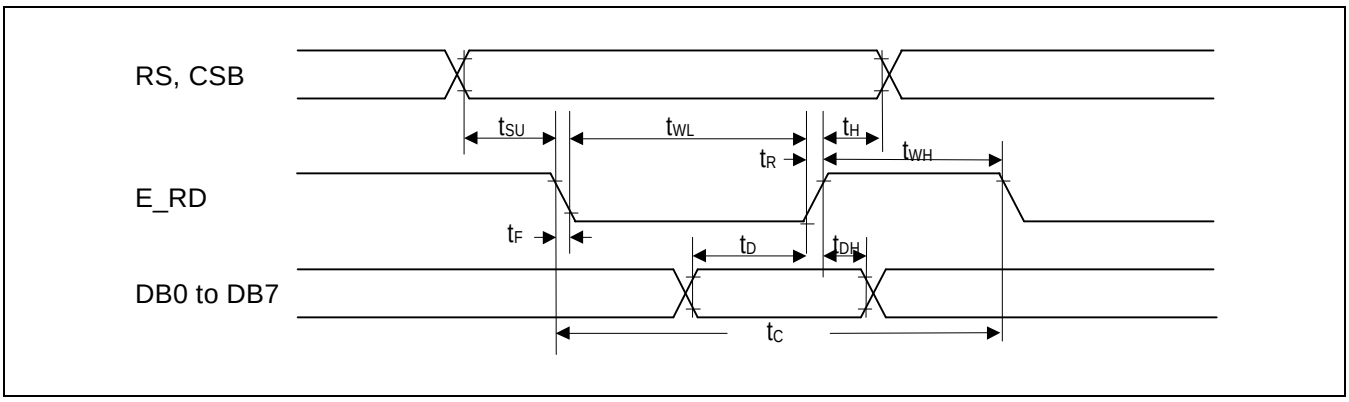


Figure 20. Read Bus Mode Timing (8080-series MPU Interface)

Clock Synchronized Serial Mode

Table 31. AC Characteristics (Serial Mode)

Condition	Characteristic	Symbol	Min.	Typ.	Max.	Unit
V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C	SCL clock cycle time	t_C	1000		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	SCL clock width (H / L)	t_W	300	-	-	
	CSB setup time	t_{SU1}	150	-	-	
	CSB hold time	t_{H1}	700	-	-	
	RS data setup time	t_{SU2}	50	-	-	
	RS data hold time	t_{H2}	300	-	-	
	SI data setup time	t_{SU3}	50	-	-	
	SI data hold time	t_{H3}	50	-	-	
V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C	SCL clock cycle time	t_C	600		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	SCL clock width (H / L)	t_W	200	-	-	
	CSB setup time	t_{SU1}	100	-	-	
	CSB hold time	t_{H1}	400	-	-	
	RS data setup time	t_{SU2}	40	-	-	
	RS data hold time	t_{H2}	200	-	-	
	SI data setup time	t_{SU3}	40	-	-	
	SI data hold time	t_{H3}	40	-	-	

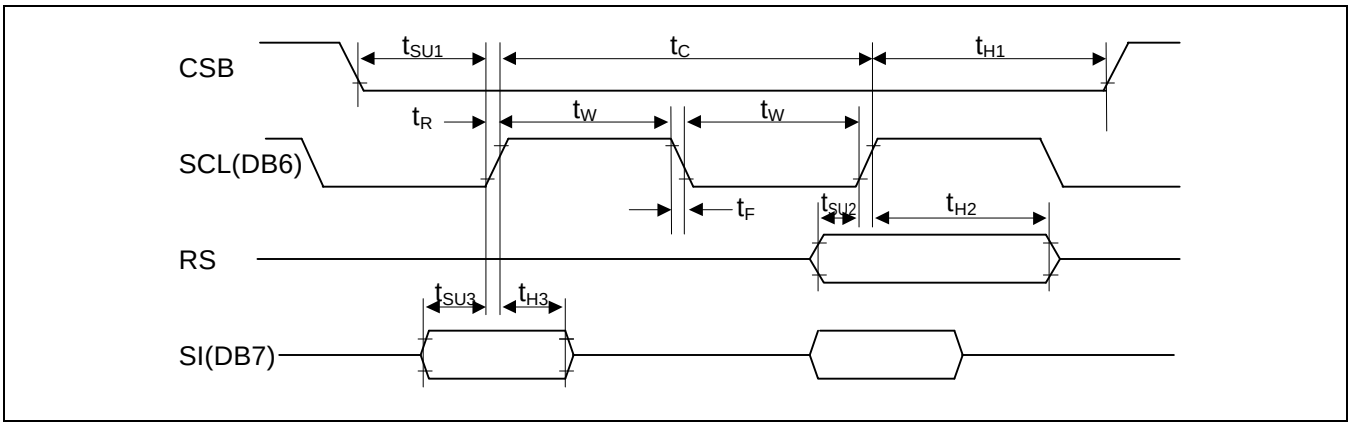


Figure 32. Clock Synchronized Serial Interface Mode Timing Diagram