GENERAL DESCRIPTION

The ST16C2552 (2552) is a dual universal asynchronous receiver and transmitter (UART). The ST16C2552 is an improved version of the PC16552 UART. The 2552 provides enhanced UART functions with 16 byte FIFOs, a modem control interface, and data rates up to 4 Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements. Indepedendent programmable baud rate generators are privded to select transmit and receive clock rates from 50 Bps to 4 Mbps. The baud rate generator can be configured for either crystal or external clock input. An internal loop-back capability allows onboard diagnostics. The 2552 provides block mode data transfers (DMA) through FIFO controls. DMA transfer monitoring is provided through the signals TXRDY# and RXRDY#. An Alternate Function Register provides the user with the ability to initialize both UARTs concurrently. The 2552 is available in the 44-PLCC package.

APPLICATIONS

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

FEATURES

Added feature in devices with top marking "A2 YYWW" and newer:

- 5 Volt Tolerant Inputs

- Pin-to-pin and functionally compatible to National PC16552 and Exar's XR16L2752 and XR16C2852
- 4 Mbps transmit/receive operation (64 MHz External Clock Frequency)
- 2 Independent UART Channels
  - Register Set Compatible to 16C550
  - 16 byte Transmit FIFO to reduce the bandwidth requirement of the external CPU
  - 16 byte Receive FIFO with error tags to reduce the bandwidth requirement of the external CPU
  - 4 selectable RX FIFO Trigger Levels
  - Fixed Transmit FIFO interrupt trigger level
  - Full Modem Interface (CTS#, RTS#, DSR#, DTR#, RI#, CD#)
- DMA operation and DMA monitoring via TXRDY# and RXRDY# pins
- UART internal register sections A & B may be written to concurrently
- Multi-Function output allows more package functions with few I/O pins
- Programmable character lengths (5, 6, 7, 8) with even, odd, or no parity
- Crystal oscillator or external clock input

FIGURE 1. ST16C2552 BLOCK DIAGRAM

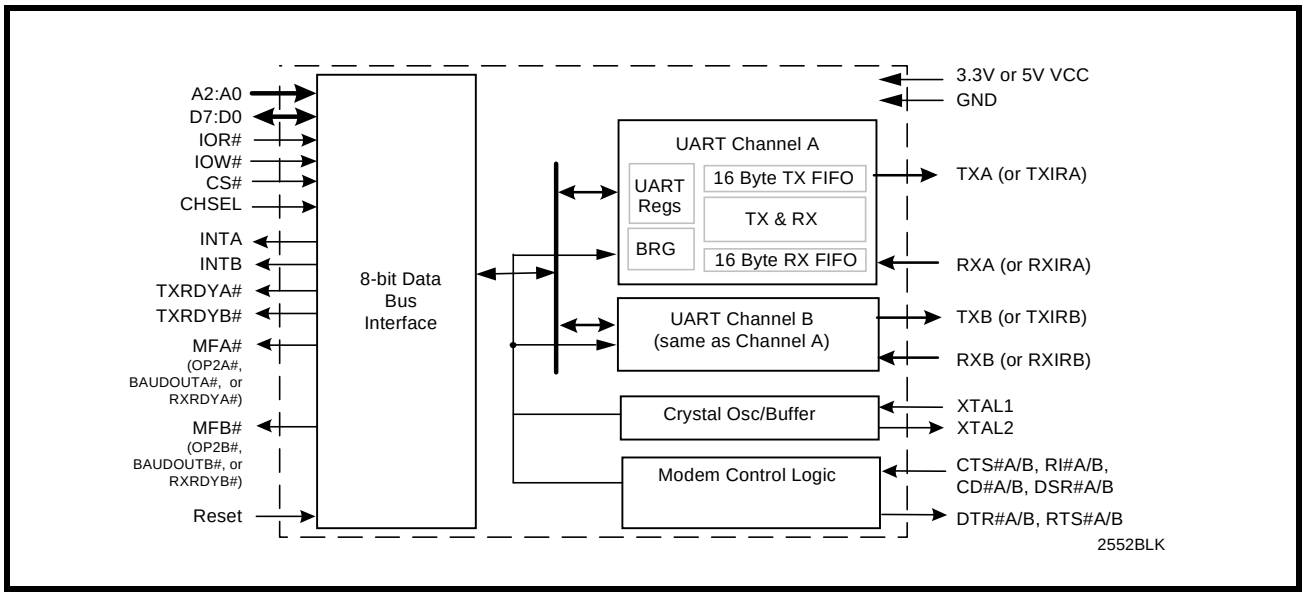
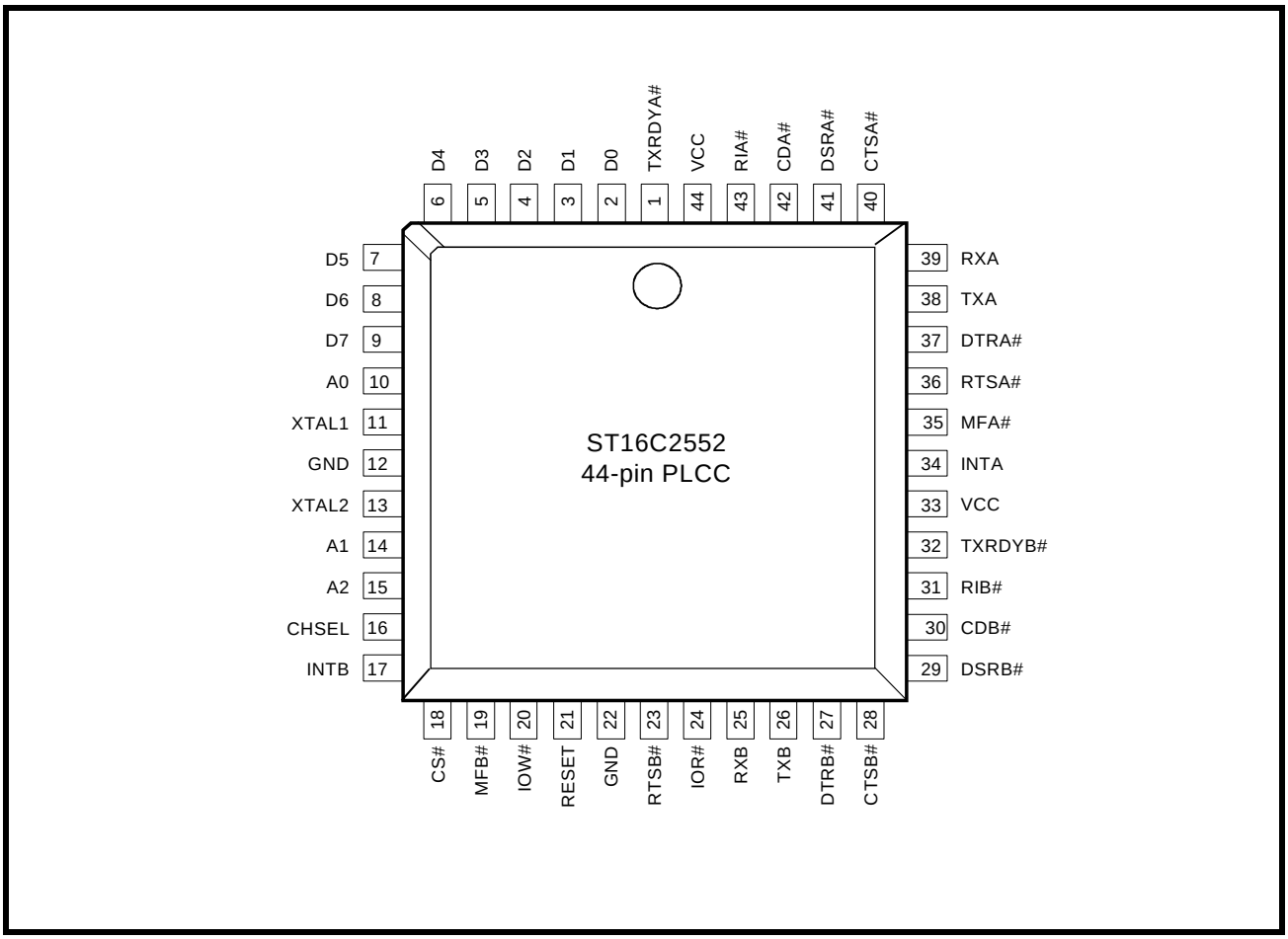


FIGURE 2. PIN OUT ASSIGNMENT



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
ST16C2552CJ	44-Lead PLCC	0°C to +70°C	Active
ST16C2552IJ	44-Lead PLCC	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Description

NAME	44-PLCC PIN #	TYPE	DESCRIPTION
DATA BUS INTERFACE			
A2 A1 A0	15 14 10	I	Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channel A/B during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	9 8 7 6 5 4 3 2	I/O	Data bus lines [7:0] (bidirectional).
IOR#	24	I	Input/Output Read Strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed to by the address lines [A2:A0]. The data byte is placed on the data bus to allow the host processor to read it on the rising edge.
IOW#	20	I	Input/Output Write Strobe (active low). The falling edge instigates an internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines.
CS#	18	I	UART chip select (active low). This function selects channel A or B in accordance with the logical state of the CHSEL pin. This allows data to be transferred between the user CPU and the 2552.
CHSEL	16	I	Channel Select - UART channel A or B is selected by the logical state of this pin when the CS# pin is a logic 0. A logic 0 on the CHSEL selects the UART channel B while a logic 1 selects UART channel A. Normally, CHSEL could just be an address line from the user CPU such as A3. Bit-0 of the Alternate Function Register (AFR) can temporarily override CHSEL function, allowing the user to write to both channel register simultaneously with one write cycle when CS# is low. It is especially useful during the initialization routine.
INTA	34	O	UART channel A Interrupt output (active high). A logic high indicates channel A is requesting for service. For more details, see Figures 16- 21.
INTB	17	O	UART channel B Interrupt output (active high). A logic high indicates channel B is requesting for service. For more details, see Figures 16- 21.
TXRDYA#	1	O	UART channel A Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel A. If it is not used, leave it unconnected.
TXRDYB#	32	O	UART channel B Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel B. If it is not used, leave it unconnected.
MODEM OR SERIAL I/O INTERFACE			

Pin Description

NAME	44-PLCC PIN #	TYPE	DESCRIPTION
MFA#	35	O	Multi-Function Output Channel A. This output pin can function as the OP2A#, BAUDOUTA#, or RXRDYA# pin. One of these output signal functions can be selected by the user programmable bits 1-2 of the Alternate Function Register (AFR). These signal functions are described as follows: 1) OP2A# - When OP2A# (active low) is selected, the MF# pin is a logic 0 when MCR bit-3 is set to a logic 1 (see MCR bit-3). MCR bit-3 defaults to a logic 1 condition after a reset or power-up. 2) BAUDOUTA# - When BAUDOUTA# function is selected, the 16X Baud rate clock output is available at this pin. 3) RXRDYA# - RXRDYA# (active low) is intended for monitoring DMA data transfers. See Table 2 for more details. If it is not used, leave it unconnected.
MFB#	19	O	Multi-Function Output ChannelB. This output pin can function as the OP2B#, BAUDOUTB#, or RXRDYB# pin. One of these output signal functions can be selected by the user programmable bits 1-2 of the Alternate Function Register (AFR). These signal functions are described as follows: 1) OP2B# - When OP2B# (active low) is selected, the MF# pin is a logic 0 when MCR bit-3 is set to a logic 1 (see MCR bit-3). MCR bit-3 defaults to a logic 1 condition after a reset or power-up. 2) BAUDOUTB# - When BAUDOUTB# function is selected, the 16X Baud rate clock output is available at this pin. 3) RXRDYB# - RXRDYB# (active low) is intended for monitoring DMA data transfers. See Table 2 for more details. If it is not used, leave it unconnected.
TXA	38	O	UART channel A Transmit Data. If it is not used, leave it unconnected.
RXA	39	I	UART channel A Receive Data. Normal receive data input must idle at logic 1 condition. If it is not used, tie it to VCC or pull it high via a 100k ohm resistor.
RTSA#	36	O	UART channel A Request-to-Send (active low) or general purpose output. If it is not used, leave it unconnected.
CTSA#	40	I	UART channel A Clear-to-Send (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
DTRA#	37	O	UART channel A Data-Terminal-Ready (active low) or general purpose output. If it is not used, leave it unconnected.
DSRA#	41	I	UART channel A Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CDA#	42	I	UART channel A Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.

Pin Description

NAME	44-PLCC PIN #	TYPE	DESCRIPTION
RIA#	43	I	UART channel A Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
TXB	26	O	UART channel B Transmit Data. If it is not used, leave it unconnected.
RXB	25	I	UART channel B Receive Data. Normal receive data input must idle at logic 1 condition. If it is not used, tie it to VCC or pull it high via a 100k ohm resistor.
RTSB#	23	O	UART channel B Request-to-Send (active low) or general purpose output. If it is not used, leave it unconnected.
CTSB#	28	I	UART channel B Clear-to-Send (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
DTRB#	27	O	UART channel B Data-Terminal-Ready (active low) or general purpose output. If it is not used, leave it unconnected.
DSRB#	29	I	UART channel B Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CDB#	30	I	UART channel B Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RIB#	31	I	UART channel B Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
ANCILLARY SIGNALS			
XTAL1	11	I	Crystal or external clock input.
XTAL2	13	O	Crystal or buffered clock output.
RESET	21	I	Reset (active high) - A longer than 40 ns logic 1 pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held at logic 1, the receiver input will be ignored and outputs are reset during reset period (see External Reset Conditions).
VCC	44, 33	Pwr	3.3V to 5V power supply. All inputs are 5V tolerant for devices with top marking of "A2 YYWW" and newer.
GND	22, 12	Pwr	Power supply common, ground.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The 2552 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The 2552 represents such an integration with greatly enhanced features. The 2552 is fabricated with an advanced CMOS process.

The 2552 is an upward solution that provides a dual UART capability with 16 bytes of transmit and receive FIFO memory, instead of none in the 16C2450. The 2552 is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 2552 by the transmit and receive FIFO's. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C2450 without a receive FIFO, will require unloading of the RHR in 93 microseconds (This example uses a character length of 11 bits, including start/stop bits at 115.2 Kbps). This means the external CPU will have to service the receive FIFO less than every 100 microseconds. However with the 16 byte FIFO in the 2552, the data buffer will not require unloading/loading for 1.53 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the 4 selectable receive FIFO trigger interrupt levels is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The 2552 is capable of operation up to 4 Mbps with a 64 MHz clock. With a crystal or external clock input of 14.7456 MHz the user can select data rates up to 921.6 Kbps.

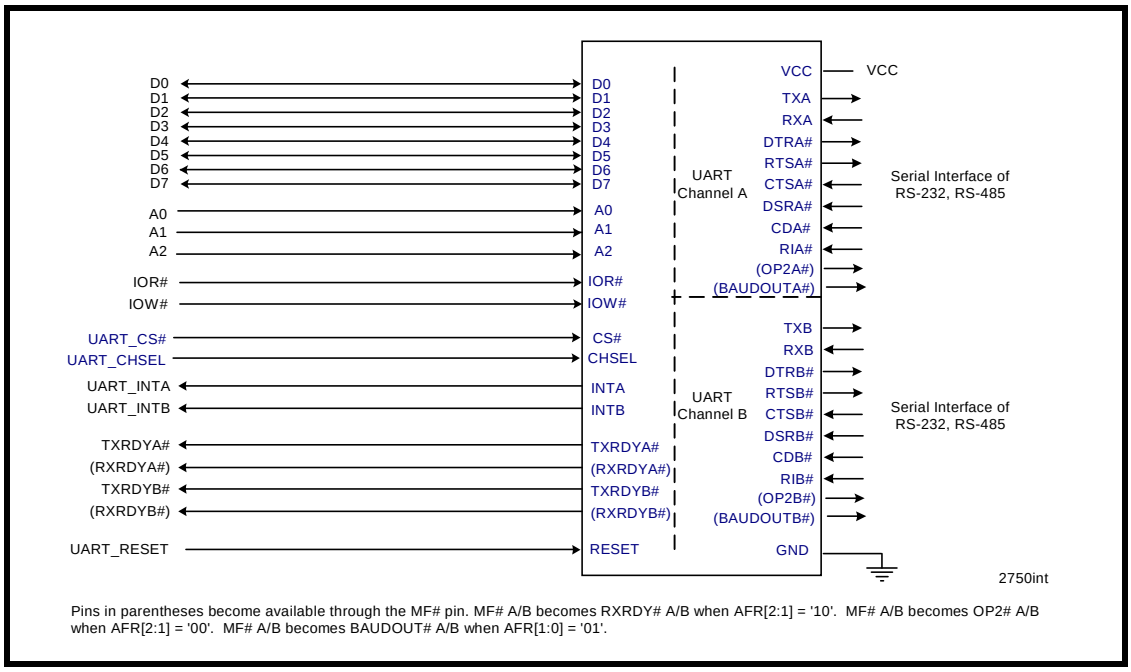
The rich feature set of the 2552 is available through internal registers. Selectable receive FIFO trigger levels, selectable TX and RX baud rates, and modem interface controls are all standard features. Following a power on reset or an external reset, the 2552 is software compatible with the 16L2752 and 16C2852.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The 2552 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS#, IOR# and IOW# signals. Both UART channels share the same data bus for host operations. The data bus interconnections are shown in Figure 3.

FIGURE 3. ST16C2552 DATA BUS INTERCONNECTIONS



Pins in parentheses become available through the MF# pin. MF# A/B becomes RXRDY# A/B when AFR[2:1] = '10'. MF# A/B becomes OP2# A/B when AFR[2:1] = '00'. MF# A/B becomes BAUDOUT# A/B when AFR[1:0] = '01'.

2.2 Device Reset

The RESET input resets the internal registers and the serial interface outputs in both channels to their default state (see the Table 11). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.3 Channel A and B Selection

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. A logic 0 on chip select pin (CS#) allows the user to select the UART and then using the channel select (CHSEL) pin, the user can select channel A or B to configure, send transmit data and/or unload receive data to/from the UART. Individual channel select functions are shown in Table 1.

TABLE 1: CHANNEL A AND B SELECT

CS#	CHSEL	FUNCTION
1	X	UART de-selected
0	1	Channel A selected
0	0	Channel B selected

2.4 Channel A and B Internal Registers

Each UART channel in the 2552 has a set of enhanced registers for controlling, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550 and dual ST16C2550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible scratchpad register (SPR).

Beyond the general 16C2550 features and capabilities, the 2552 offers the Alternate Function Register which allows simultaneous writes to both channels. All the register functions are discussed in full detail later in "Section 3.0, UART INTERNAL REGISTERS" on page 15.

2.5 Simultaneous Write to Channel A and B

During a write mode cycle, the setting of Alternate Function Register (AFR) bit-0 to a logic 1 will override the CHSEL selection and allows a simultaneous write to both UART channel sections. This functional capability allow the registers in both UART channels to be modified concurrently, saving individual channel initialization time. Caution should be exercised, however, when using this capability. Any in-process serial data transfer may be disrupted by changing an active channel's mode.

2.6 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document doesn't mean "direct memory access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A/B (MF# A/B becomes RXRDY# A/B output when AFR[2:1] = '10') and TXRDY# A/B output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 2552 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. The following table show their behavior. Also see Figures 16 through 21.

TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
RXRDY# A/B	0 = 1 byte. 1 = no data.	0 = at least 1 byte in FIFO 1 = FIFO empty.	1 to 0 transition when FIFO reaches the trigger level, or timeout occurs. 0 to 1 transition when FIFO empties.
TXRDY# A/B	0 = THR empty. 1 = byte in THR.	0 = FIFO empty. 1 = at least 1 byte in FIFO.	0 = FIFO has at least 1 empty location. 1 = FIFO is full.

2.7 INTA and INTB Ouputs

The INTA and INTB interrupt outputs change according to the operating mode and enahnced features setup. Tables 3 and 4 summarize the operating behavior for the transmitter and receiver. Also see Figures 16 through 21.

TABLE 3: INTA AND INTB PINS OPERATION FOR TRANSMITTER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INTA/B Pin	0 = a byte in THR 1 = THR empty	0 = at least 1 byte in FIFO 1 = FIFO empty

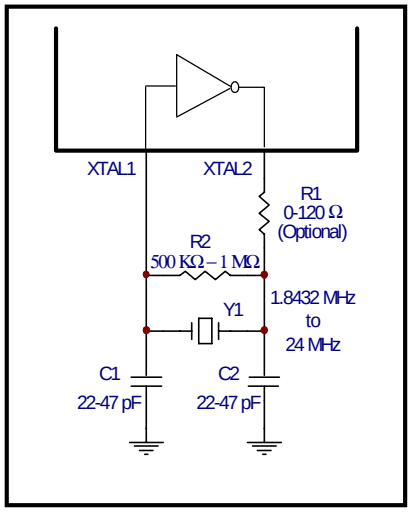
TABLE 4: INTA AND INTB PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INTA/B Pin	0 = no data 1 = 1 byte	0 = FIFO below trigger level 1 = FIFO above trigger level

2.8 Crystal Oscillator or Ext. Clock Input

The 2552 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. See "Programmable Baud Rate Generator" on page 10.

FIGURE 4. TYPICAL OSCILLATOR CONNECTIONS

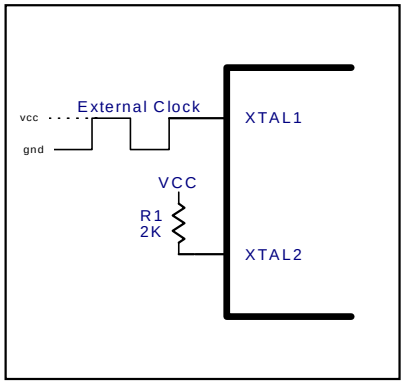


The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see Figure 2), with an external 500kΩ to 1 MΩ resistor across it. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typical oscillator connections are shown in Figure 4. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

2.9 Programmable Baud Rate Generator

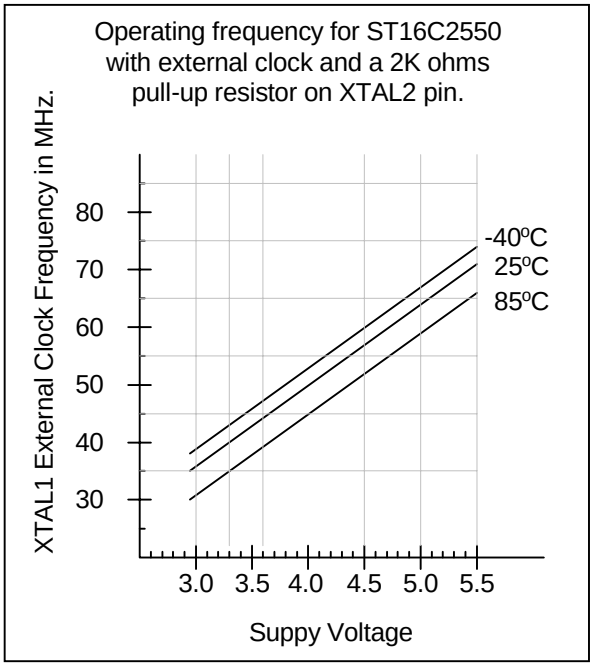
A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of operating with a crystal frequency of up to 24 MHz. However, with an external clock input on XTAL1 pin and a 2K ohms pull-up resistor on XTAL2 pin (as shown in Figure 5) it can extend its operation up to 64 MHz (4Mbps serial data rate) at room temperature and 5.0V.

FIGURE 5. EXTERNAL CLOCK CONNECTION FOR EXTENDED DATA RATE



To obtain maximum data rate, it is necessary to use full rail swing on the clock input. See external clock operating frequency over power supply voltage chart in Figure 6.

FIGURE 6. OPERATING FREQUENCY CHART. REQUIRES A 2K OHMS PULL-UP RESISTOR ON XTAL2 PIN TO INCREASE OPERATING SPEED.



The 2552 divides the basic external clock by 16. The basic 16X clock provides table rates to support standard and custom applications using the same system design. The Baud Rate Generator divides this 16X clock by any divisor from 1 to 2^{16} -1. The rate table is configured via the DLL and DLM internal register functions. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Table 5 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X sampling rate. When using a non-standard frequency crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 or External clock frequency) / (serial data rate x 16)

TABLE 5: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=0	DIVISOR FOR 16X Clock (Decimal)	DIVISOR FOR 16X Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
400	2304	900	09	00	0
2400	384	180	01	80	0
4800	192	C0	00	C0	0
9600	96	60	00	60	0
19.2k	48	30	00	30	0
38.4k	24	18	00	18	0
76.8k	12	0C	00	0C	0
153.6k	6	06	00	06	0
230.4k	4	04	00	04	0
460.8k	2	02	00	02	0
921.6k	1	01	00	01	0

2.10 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 16 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

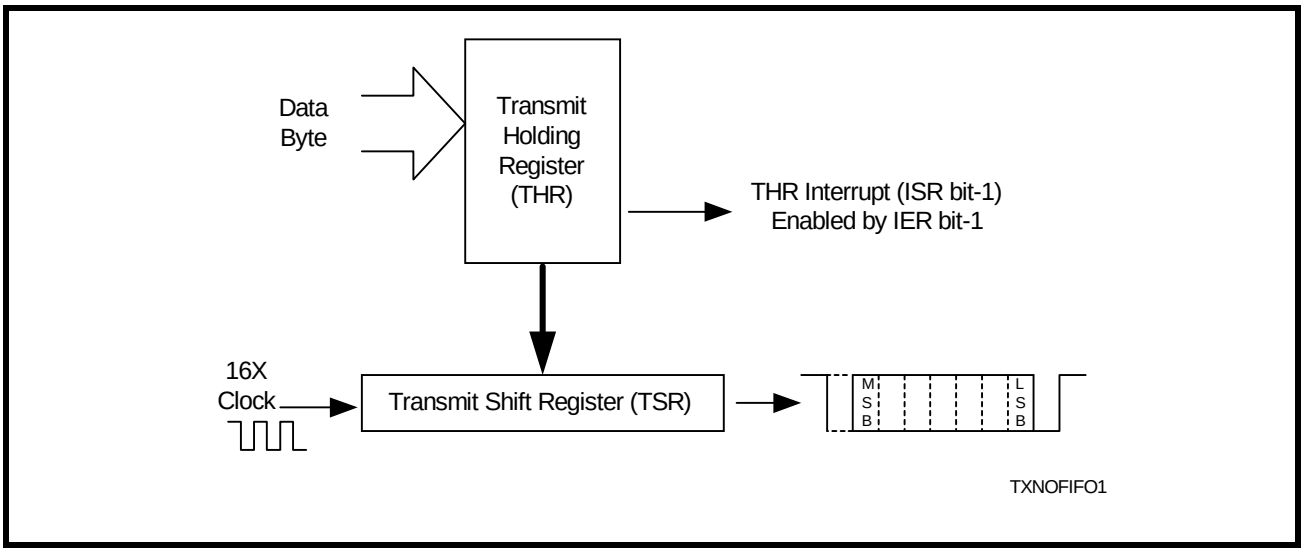
2.10.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 16 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.10.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

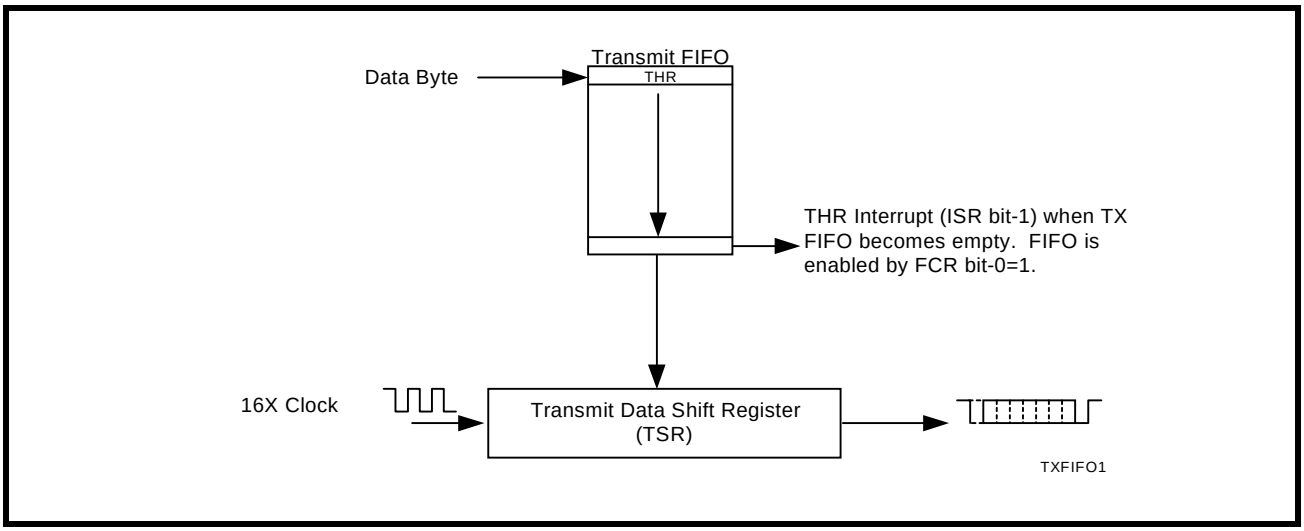
FIGURE 7. TRANSMITTER OPERATION IN NON-FIFO MODE



2.10.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 16 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when the FIFO and the TSR become empty.

FIGURE 8. TRANSMITTER OPERATION IN FIFO MODE



2.11 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 16 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are

reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.11.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 16 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 9. RECEIVER OPERATION IN NON-FIFO MODE

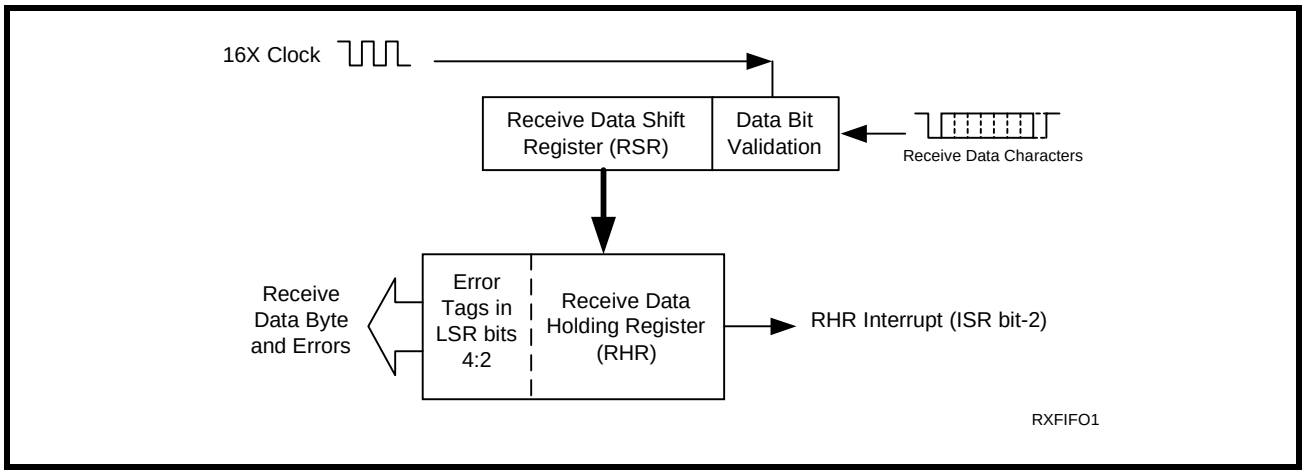
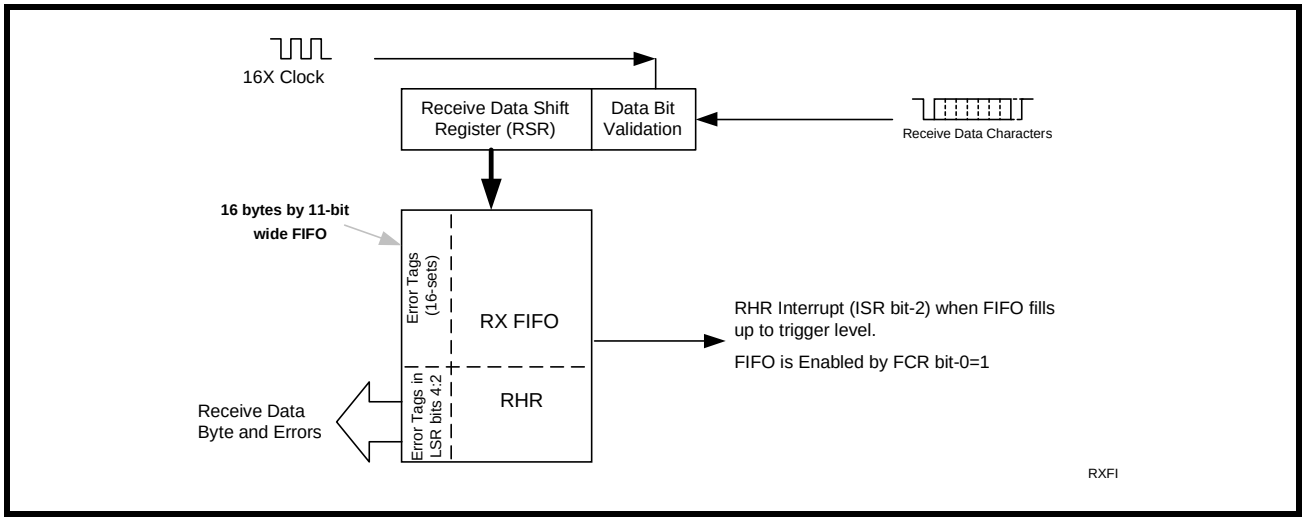


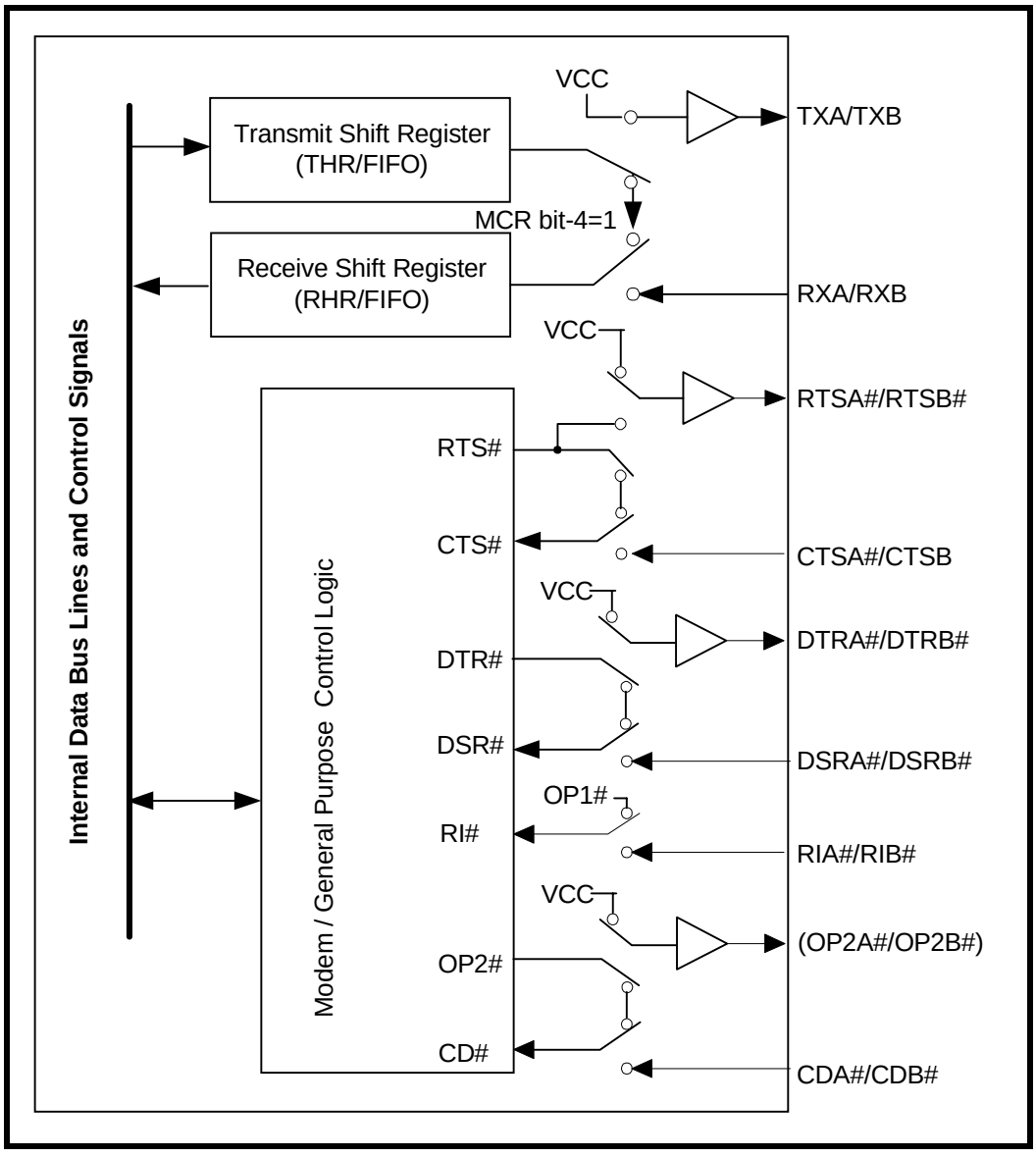
FIGURE 10. RECEIVER OPERATION IN FIFO MODE



2.12 Internal Loopback

The 2552 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 11 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

FIGURE 11. INTERNAL LOOP BACK IN CHANNEL A AND B



3.0 UART INTERNAL REGISTERS

Each of the UART channel in the 2552 has its own set of configuration registers selected by address lines A0, A1 and A2 with CS# and CHSEL selecting the channel. The registers are 16C550 compatible. The complete register set is shown in Table 6 and Table 7.

TABLE 6: UART CHANNEL A AND B UART INTERNAL REGISTERS

A2,A1,A0 ADDRESSES	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Div Latch Low Byte	Read/Write	LCR[7] = 1
0 0 1	DLM - Div Latch High Byte	Read/Write	LCR[7] = 1
0 1 0	AFR - Alternate Function Register	Read/Write	LCR[7] = 1
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR[7] = 0
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	
1 0 1	LSR - Line Status Register Reserved	Read-only Write-only	
1 1 0	MSR - Modem Status Register Reserved	Read-only Write-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	

.

TABLE 7: INTERNAL REGISTERS DESCRIPTION.

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0	0	0	0	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0	0	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0 1 0	FCR	WR	RXFIFO Trigger Bit-1	RXFIFO Trigger Bit-0	0	0	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Par-ity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0	0	0	Internal Loop-back Enable	OP2# Output Control	Rsvd (OP1#)	RTS# Output Control	DTR# Output Control	
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Over-run Error	RX Data Ready	
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 1 0	AFR	RD/WR	0	0	0	0	0	RXRDY# Select	Baudout# Select	Concur-rent Write	

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

See “Receiver” on page 12.

4.2 Transmit Holding Register (THR) - Write-Only

See “Transmitter” on page 11.

4.3 Baud Rate Generator Divisors (DLL and DLM) - Read/Write

The Baud Rate Generator (BRG) is a 16-bit counter that generates the data rate for the transmitter. The rate is programmed through registers DLL and DLM which are only accessible when LCR bit-7 is set to '1'. See "Programmable Baud Rate Generator" on page 10. for more details.

4.4 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.4.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.4.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the ST16C2552 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates transmit FIFO is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the TX FIFO becomes empty.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt when the character with errors is read out of the FIFO.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[7:4]: Reserved

4.5 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 8, shows the data values (bits 0-3) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

4.5.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty.
- MSR is by any of the MSR bits 0, 1, 2 and 3.

4.5.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.

TABLE 8: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS				SOURCE OF INTERRUPT
	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	1	1	0	LSR (Receiver Line Status Register)
2	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	MSR (Modem Status Register)
-	0	0	0	1	None (default)

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Interrupt Source Table 8).

ISR[5:4]: Reserved

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.6 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No receive FIFO reset (default)
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

Controls the behavior of the TXRDY# and RXRDY# pins. See DMA operation section for details.

- Logic 0 = Normal Operation (default).
- Logic 1 = DMA Mode.

FCR[5:4]: Reserved

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1)

These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. Table 9 shows the complete selections.

TABLE 9: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION

FCR BIT-7	FCR BIT-6	RECEIVE TRIGGER LEVEL	COMPATIBILITY
0	0	1 (default)	Table-A. 16C550, 16C2550, 16C2552, 16C554, 16C580 compatible.
0	1	4	
1	0	8	
1	1	14	

4.7 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 10 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR[5] = logic 0, parity is not forced (default).
- LCR[5] = logic 1 and LCR[4] = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR[5] = logic 1 and LCR[4] = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

TABLE 10: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, “1”
1	1	1	Forced parity to space, “0”

LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a “space’, logic 0, state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a “space”, logic 0, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL/DLM) enable.

- Logic 0 = Data registers are selected. (default)
- Logic 1 = Divisor latch registers are selected.

4.8 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force DTR# output to a logic 1 (default).
- Logic 1 = Force DTR# output to a logic 0.

MCR[1]: RTS# Output

The RTS# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# output to a logic 1 (default).
- Logic 1 = Force RTS# output to a logic 0.

MCR[2]: OP1# Output

OP1# is not available as an output pin on the 2552. But it is available for use during Internal Loopback Mode. In the Loopback Mode, this bit is used to write the state of the modem RI# interface signal.

MCR[3]: OP2# Output

OP2# is available as an output pin on the 2552 when AFR[2:1] = '00'. In the Loopback Mode, MCR[3] is used to write the state of the modem CD# interface signal. Also see pin descriptions for MF# pins.

- Logic 0 = Forces OP2# output to a logic 1 (default).
- Logic 1 = Forces OP2# output to a logic 0.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and Figure 11.

MCR[7:5]: Reserved

4.9 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[2]: Receive Data Parity Error Tag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Tag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[4]: Receive Break Tag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication remains until the RX input returns to the idle condition, "mark" or logic 1.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. This bit indicates that the transmitter is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the host when the THR interrupt enable is set. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to a logic 1 whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in the FIFO.

4.10 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface signals, or other peripheral device that the UART is connected. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used as general purpose inputs/outputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

Normally MSR bit-4 bit is the compliment of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

Normally this bit is the compliment of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

Normally this bit is the compliment of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

Normally this bit is the compliment of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

4.11 Scratch Pad Register (SPR) - Read/Write

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

4.12 Baud Rate Generator Registers (DLL and DLM) - Read/Write

The concatenation of the contents of DLM and DLL gives the 16-bit divisor value which is used to calculate the baud rate:

- Baud Rate = (Clock Frequency / 16) / Divisor

See MCR bit-7 and the baud rate table also.

4.13 Alternate Function Register (AFR) - Read/Write

This register is used to select specific modes of MF# operation and to allow both UART register sets to be written concurrently.

AFR[0]: Concurrent Write Mode

When this bit is set, the CPU can write concurrently to the same register in both UARTs. This function is intended to reduce the dual UART initialization time. It can be used by the CPU when both channels are initialized to the same state. The external CPU can set or clear this bit by accessing either register set. When this bit is set, the channel select pin still selects the channel to be accessed during read operations. The user should ensure that LCR Bit-7 of both channels are in the same state before executing a concurrent write to the registers at address 0, 1, or 2.

- Logic 0 = No concurrent write (default).
- Logic 1 = Register set A and B are written concurrently with a single external CPU I/O write operation.

AFR[2:1]: MF# Output Select

These bits select a signal function for output on the MF# A/B pins. These signal function are described as: OP2#, BAUDOUT#, or RXRDY#. Only one signal function can be selected at a time.

BIT-2	BIT-1	MF# FUNCTION
0	0	OP2# (default)
0	1	BAUDOUT#
1	0	RXRDY#
1	1	Reserved

AFR[7:3]: Reserved

All are initialized to logic 0.

TABLE 11: UART RESET CONDITIONS FOR CHANNEL A AND B

REGISTERS	RESET STATE
DLL	Bits 7-0 = 0xXX
DLM	Bits 7-0 = 0xXX
AFR	Bits 7-0 = 0x00
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = Logic 0 Bits 7-4 = Logic levels of the inputs inverted
SPR	Bits 7-0 = 0xFF
I/O SIGNALS	**RESET STATE**
TX	Logic 1
MF#	Logic 1
RTS#	Logic 1
DTR#	Logic 1
TXRDY#	Logic 0
INT	Logic 0

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	7 Volts
Voltage at Any Pin	GND-0.3 V to VCC+0.3 V
Operating Temperature	-40^{O} to +85^{O}C
Storage Temperature	-65^{O} to +150^{O}C
Package Dissipation	500 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (44-PLCC)	theta-ja = 50^{O}C/W, theta-jc = 21^{O}C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97V TO 5.5V

SYMBOL	PARAMETER					TOP MARKING "A2 YYWW" AND NEWER				UNITS	
		LIMITS 3.3V		LIMITS 5.0V		LIMITS 3.3V		LIMITS 5.0V			CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V_{ILCK}	Clock Input Low Level	-0.3	0.6	-0.5	0.6	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock Input High Level	2.4	VCC	3.0	VCC	2.4	5.5	3.0	5.5	V	
V_{IL}	Input Low Voltage	-0.3	0.8	-0.5	0.8	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	VCC	2.2	VCC	2.0	5.5	2.2	5.5	V	
V_{OL}	Output Low Voltage				0.4				0.4	V	I_{OL} = 6 mA
V_{OL}	Output Low Voltage		0.4				0.4			V	I_{OL} = 4 mA
V_{OH}	Output High Voltage			2.4				2.4		V	I_{OH} = -6 mA
V_{OH}	Output High Voltage	2.0				2.0				V	I_{OH} = -1 mA
I_{IL}	Input Low Leakage Current		±10		±10		±10		±10	uA	
I_{IH}	Input High Leakage Current		±10		±10		±10		±10	uA	
C_{IN}	Input Pin Capacitance		5		5		5		5	pF	
I_{CC}	Power Supply Current		1.2		3		1.2		3	mA	

AC ELECTRICAL CHARACTERISTICS

TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97 TO 5.5V

70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 3.3		LIMITS 5.0		UNIT
		MIN	MAX	MIN	MAX	
-	Crystal Frequency		20		24	MHz
CLK	Clock Pulse Duration	17		8		ns
OSC	External Clock Frequency		30		64	MHz
T_{AS}	Address Setup Time	5		0		ns
T_{AH}	Address Hold Time	10		5		ns
T_{CS}	Chip Select Width	66		50		ns
T_{RD}	IOR# Strobe Width	35		25		ns
T_{DY}	Read Cycle Delay	40		30		ns
T_{RDV}	Data Access Time		35		25	ns
T_{DD}	Data Disable Time	0	25	0	15	ns
T_{WR}	IOW# Strobe Width	40		25		ns
T_{DY}	Write Cycle Delay	40		30		ns
T_{DS}	Data Setup Time	20		15		ns
T_{DH}	Data Hold Time	5		5		ns
T_{WDO}	Delay From IOW# To Output		50		40	ns
T_{MOD}	Delay To Set Interrupt From MODEM Input		40		35	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		40		35	ns
T_{SSI}	Delay From Stop To Set Interrupt		1		1	Bclk
T_{RRI}	Delay From IOR# To Reset Interrupt		45		40	ns
T_{SI}	Delay From Start To Interrupt		45		40	ns
T_{INT}	Delay From Initial INT Reset To Transmit Start	8	24	8	24	Bclk
T_{WRI}	Delay From IOW# To Reset Interrupt		45		40	ns
T_{SSR}	Delay From Stop To Set RXRDY#		1		1	Bclk
T_{RR}	Delay From IOR# To Reset RXRDY#		45		40	ns
T_{WT}	Delay From IOW# To Set TXRDY#		45		40	ns
T_{SRT}	Delay From Center of Start To Reset TXRDY#		8		8	Bclk
T_{RST}	Reset Pulse Width	40		40		ns

AC ELECTRICAL CHARACTERISTICS

TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97 TO 5.5V

70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 3.3 MIN	LIMITS 3.3 MAX	LIMITS 5.0 MIN	LIMITS 5.0 MAX	UNIT
N	Baud Rate Divisor	1	2^{16}-1	1	2^{16}-1	-
Bclk	Baud Clock	16X of data rate				Hz

FIGURE 12. CLOCK TIMING

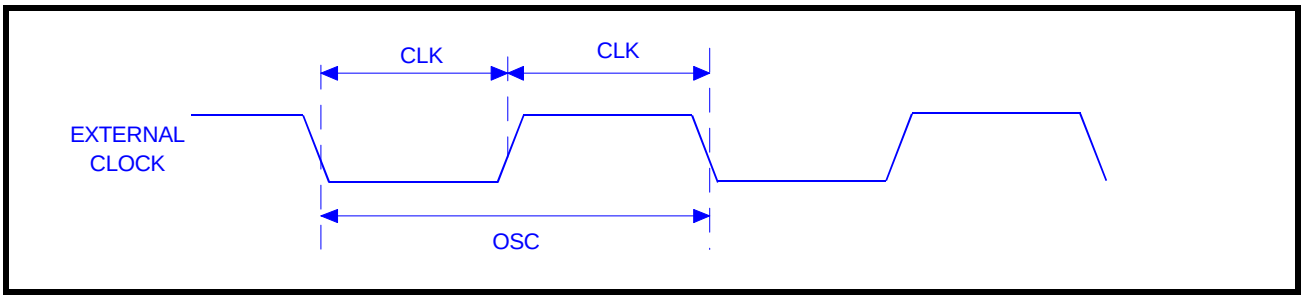


FIGURE 13. MODEM INPUT/OUTPUT TIMING FOR CHANNELS A & B

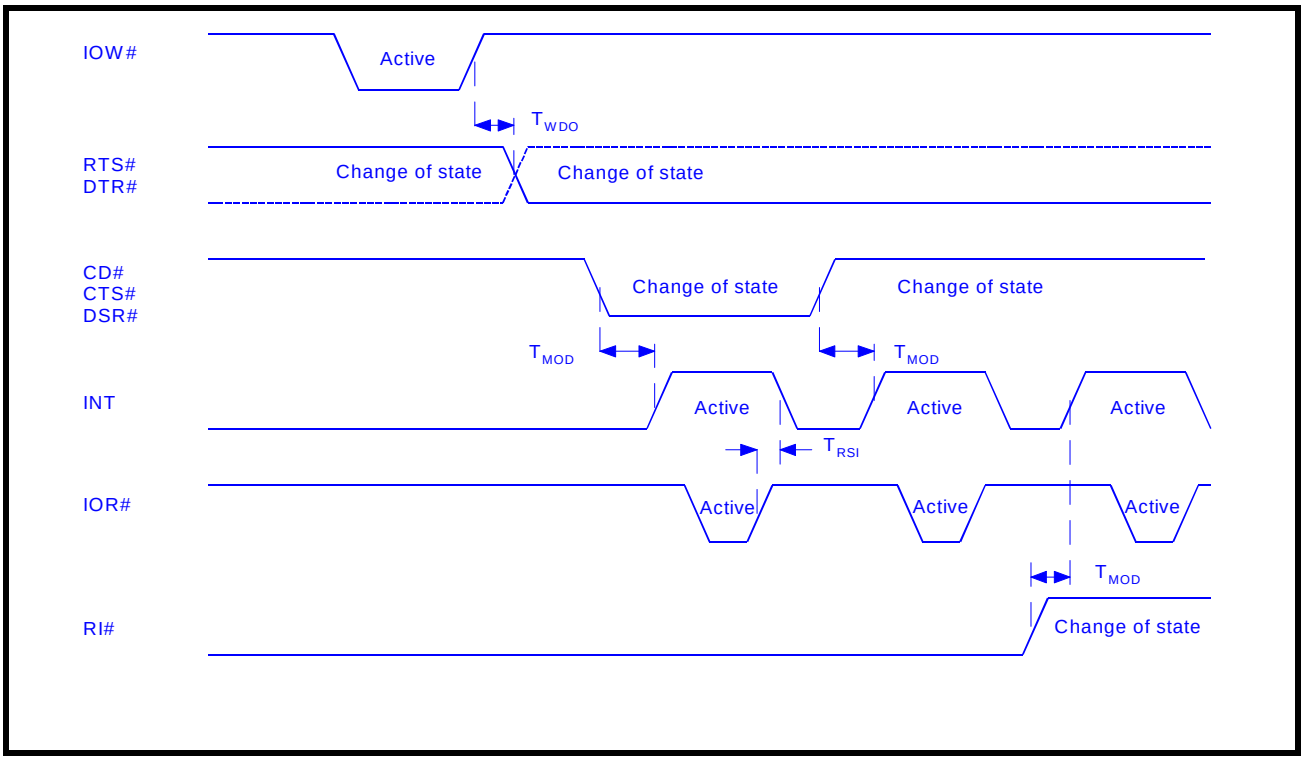


FIGURE 14. DATA BUS READ TIMING

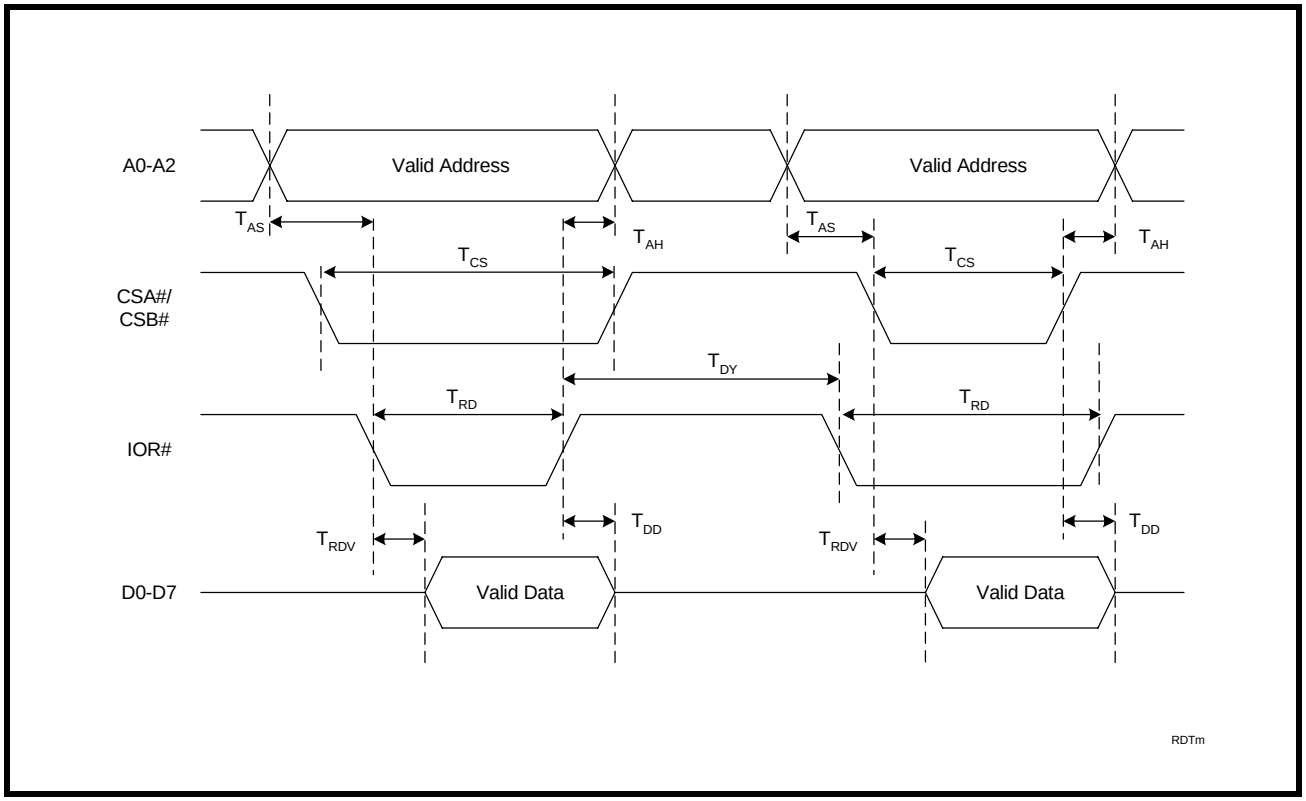


FIGURE 15. DATA BUS WRITE TIMING

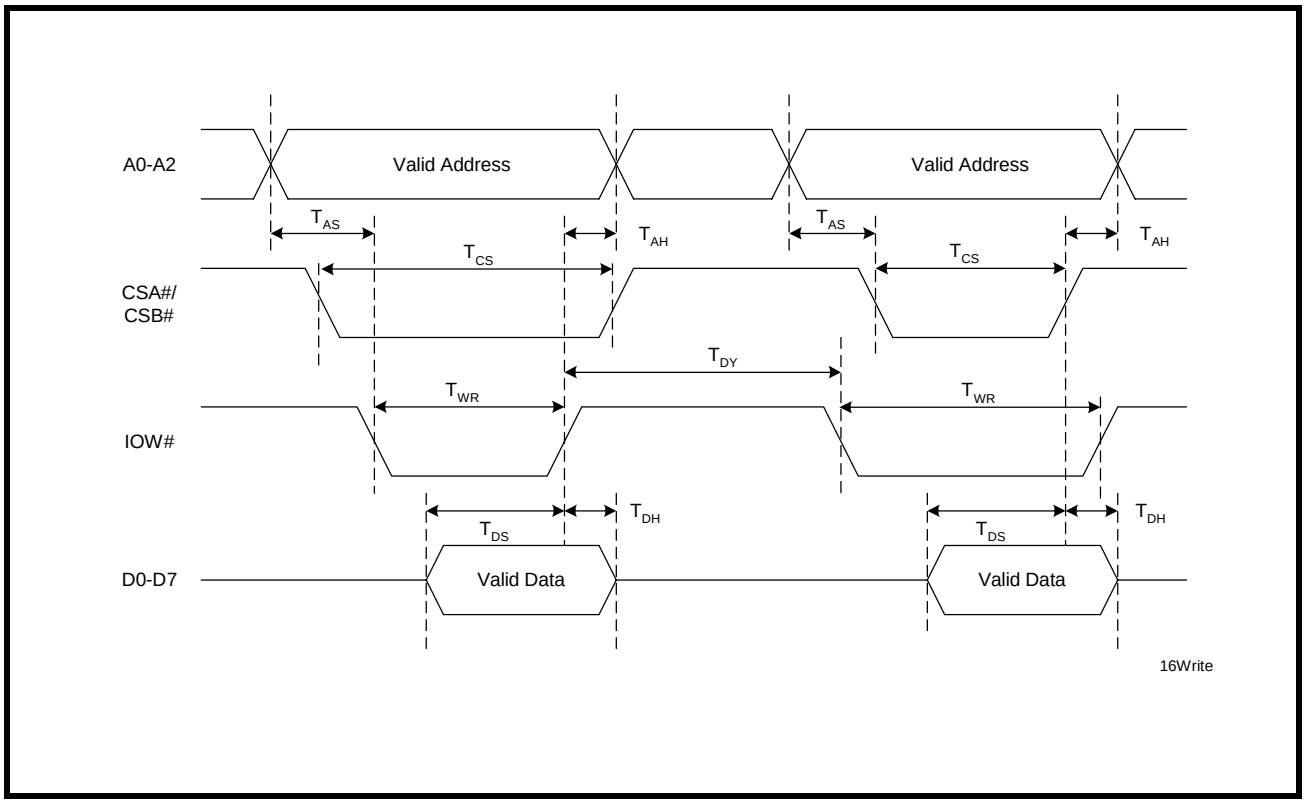


FIGURE 16. RECEIVE READY AND INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B

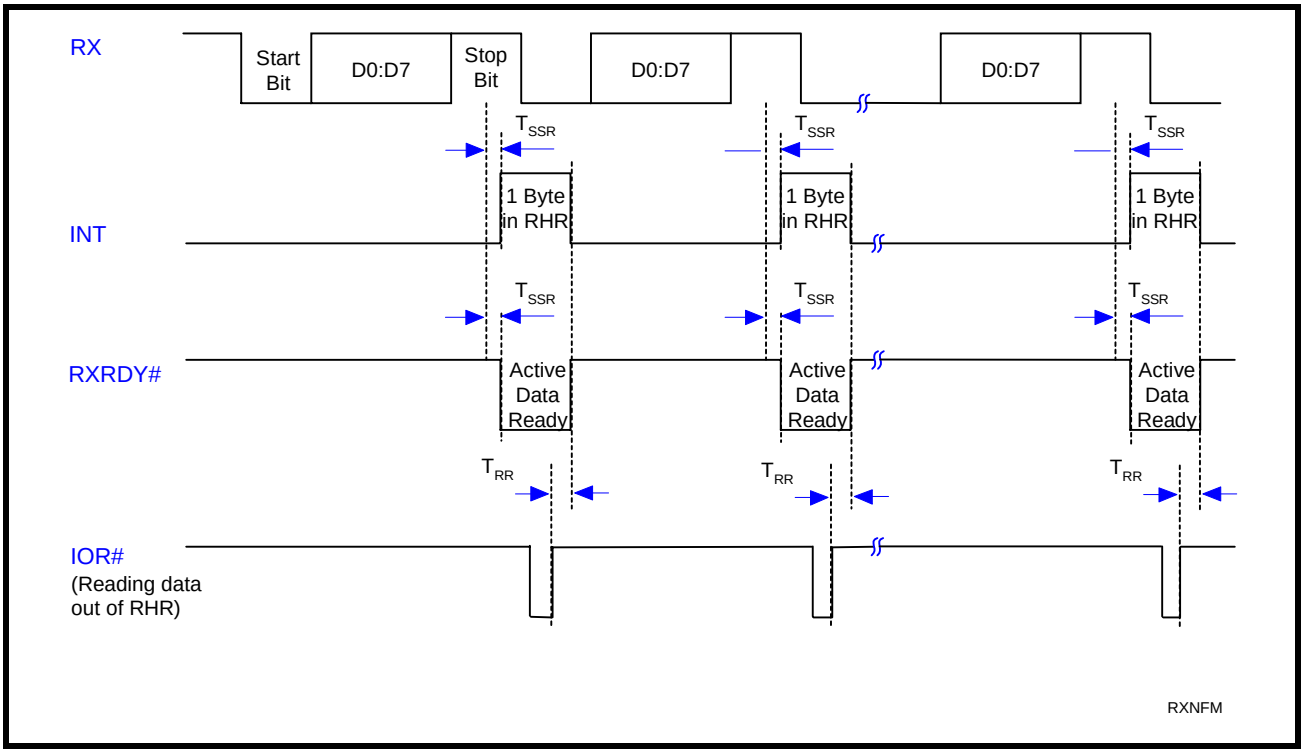


FIGURE 17. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B

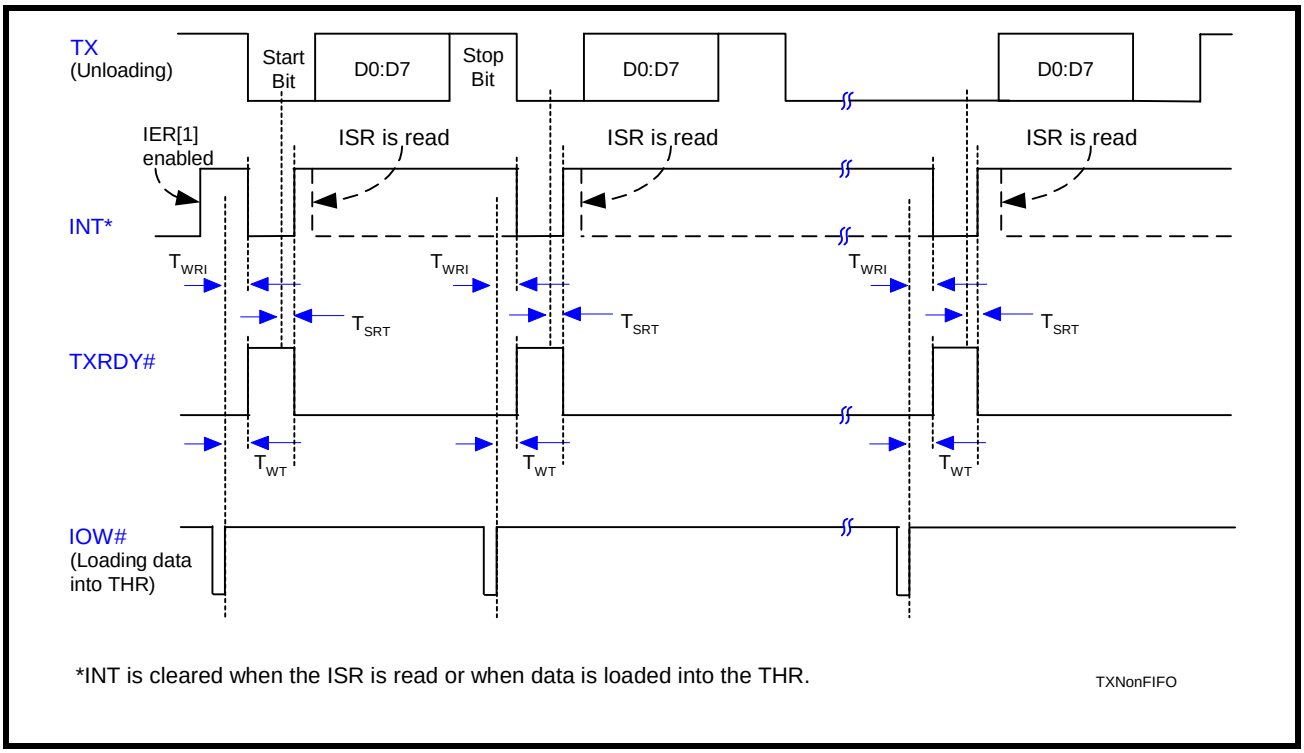


FIGURE 18. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED] FOR CHANNELS A & B

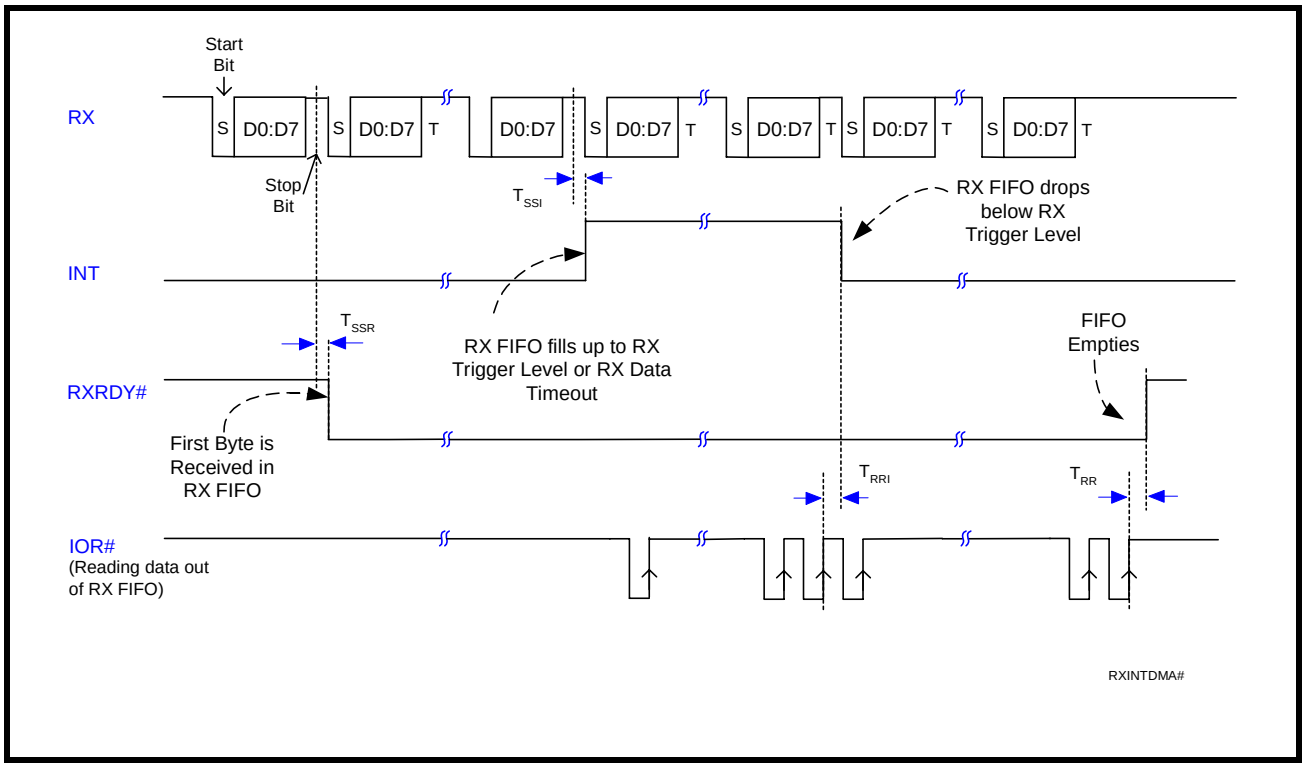


FIGURE 19. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED] FOR CHANNELS A & B

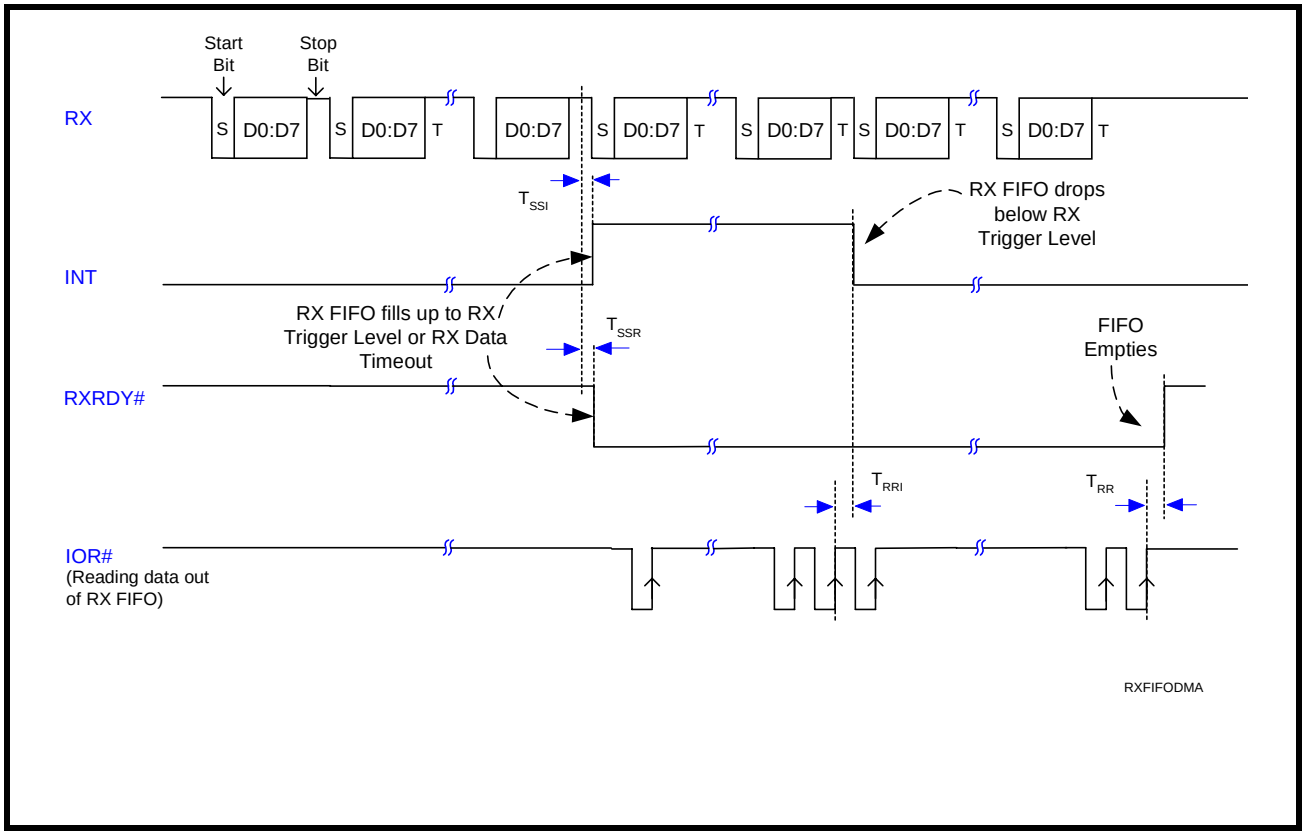


FIGURE 20. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED] FOR CHANNELS A & B

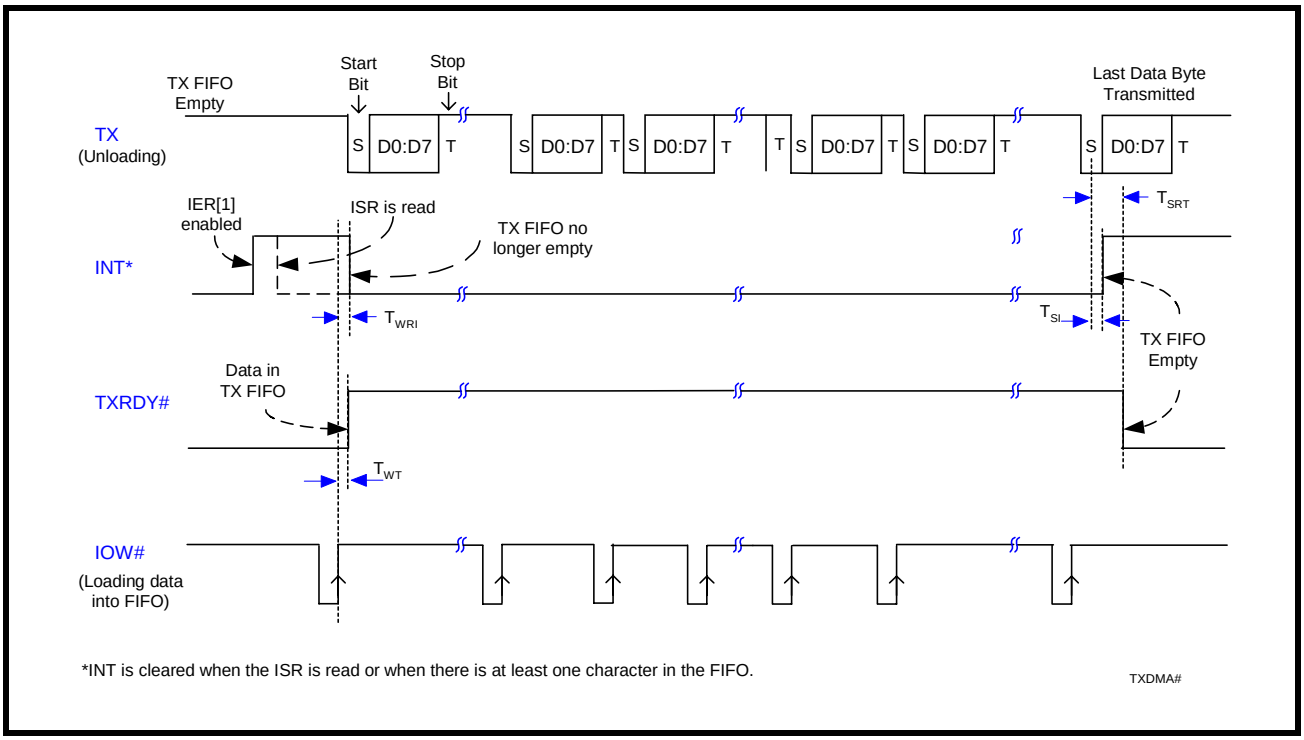
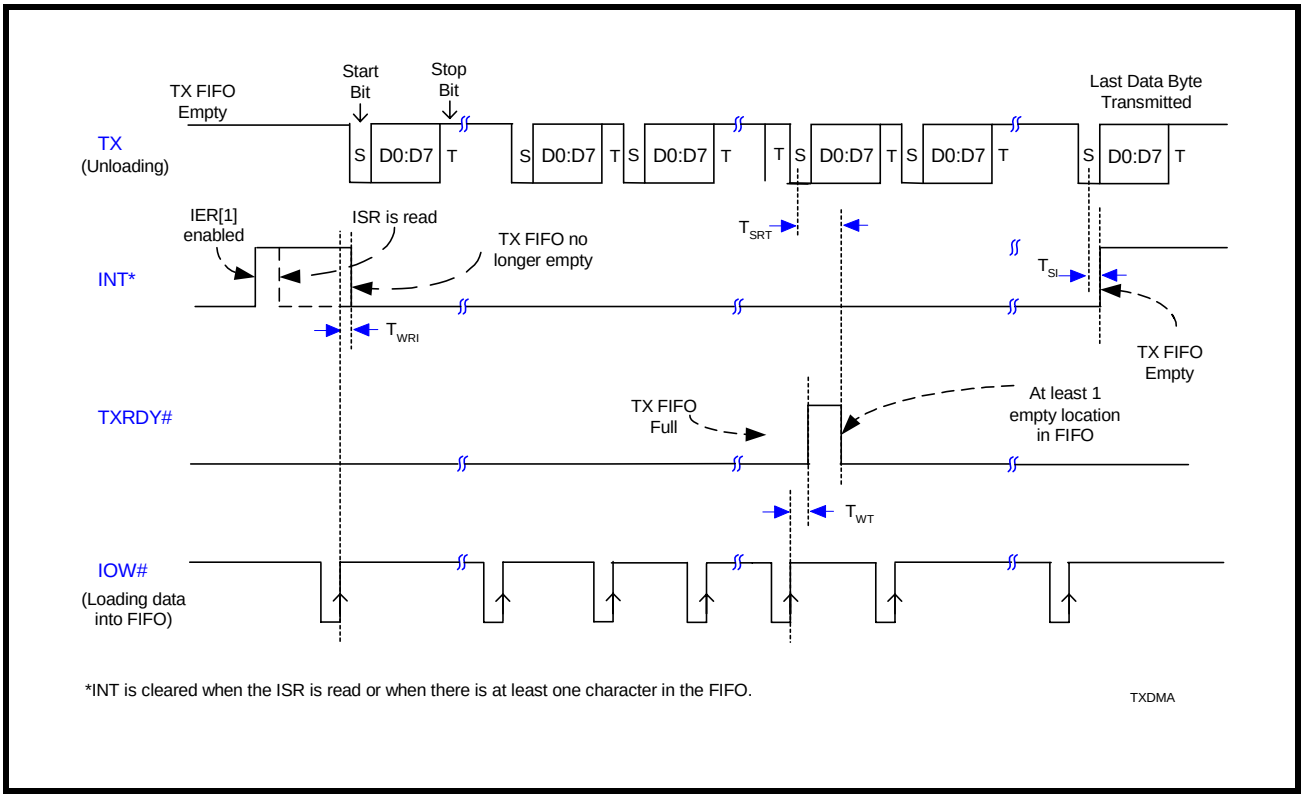


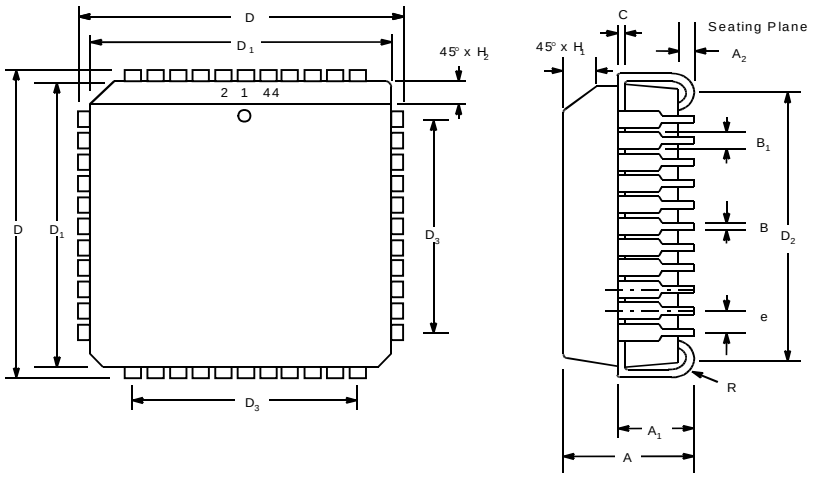
FIGURE 21. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED] FOR CHANNELS A & B



PACKAGE DIMENSIONS (44 PIN PLCC)

44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Revision History

Date	Revision	Description
February 2002	4.0	Changed to standard style format. Text descriptions were clarified and simplified (eg. DMA operation, FIFO mode vs. Non-FIFO mode operations etc). Clarified timing diagrams. Renamed Rclk (Receive Clock) to Bclk (Baud Clock) and timing symbols. Added T_{AH}, T_{CS} and OSC.
March 2002	4.1	Minor clarifications in text descriptions. Changed A0-A7 in Figures 14 and 15 to A0-A2.
September 2003	4.2	Changed to single column format. Corrected A2 and A0 pin numbers in Pin Descriptions. Added Device Status to Ordering Information. Devices with top markings of "A2 YYWW" and newer have 5V tolerant inputs. Devices with top markings of "CC YYWW" and older do not have 5V tolerant inputs.

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