SA01 • SA01-6

FEATURES

- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE — 16-100V
- 20A CONTINUOUS OUTPUT
- PROGRAMMABLE CURRENT LIMIT
- SHUTDOWN CONTROL
- HERMETIC PACKAGE
- 2 IN² FOOTPRINT

APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- PELTIER CONTROL
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

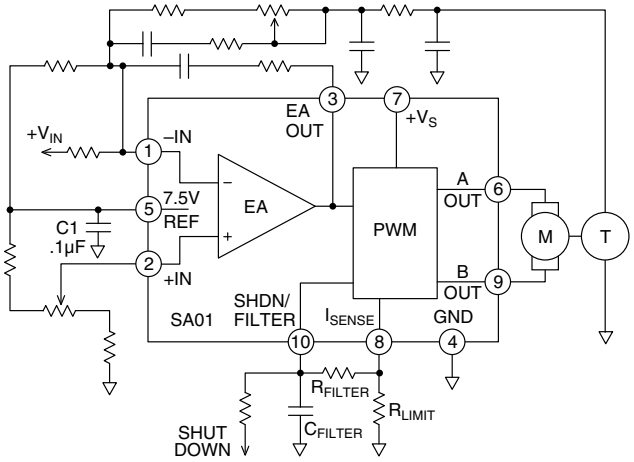
DESCRIPTION

The SA01 amplifier is a pulse width modulation amplifier that can supply 2KW to the load. The full bridge output amplifier can be operated from a single power supply over a wide range of voltages. An error amplifier is included which can provide gain for the velocity control loop in brush type motor control applications. Current limit is programmable by a single resistor. A shutdown input turns off all four drivers of the H bridge output. A precision reference output is provided for use in offsetting the error amplifier. The error amplifier can then be scaled for standard input signals. The amplifier is protected from shorts to supply or ground. The H bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 10-pin hermetic power package occupies only 2 square inches of board space and is isolated.



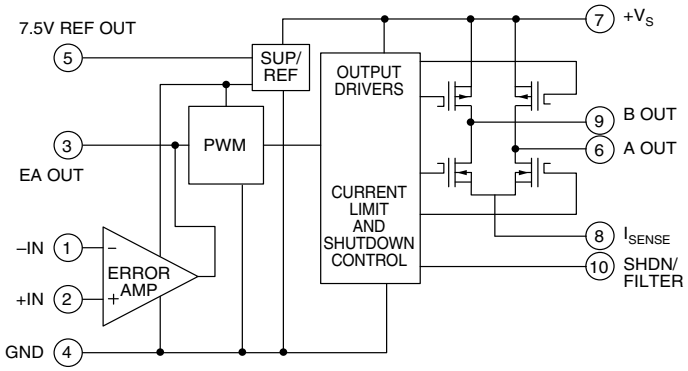
10-PIN POWER DIP
PACKAGE STYLE DE

TYPICAL APPLICATION



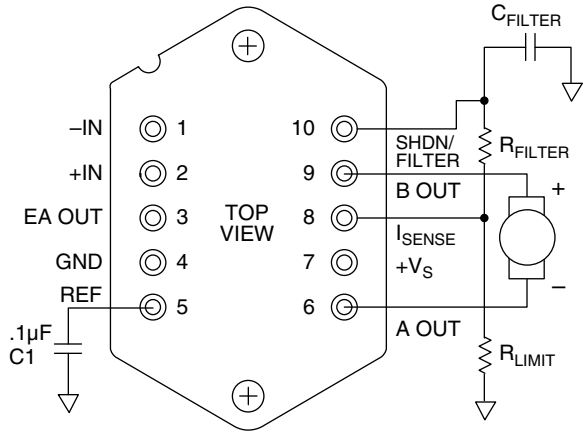
Motor Driver With Tach Feedback

BLOCK DIAGRAM



AS EA OUT (3) GOES MORE POSITIVE, HIGH STATE OF A OUT (6) INCREASES AND HIGH STATE OF B OUT (9) DECREASES.

EXTERNAL CONNECTIONS



$$R_{LIMIT} = \frac{.2}{I_{LIMIT}}$$

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	100V
OUTPUT CURRENT, peak	30A
POWER DISSIPATION, internal	185W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
SHUTDOWN VOLTAGE	10V
REFERENCE LOAD CURRENT	10mA
ERROR AMP INPUT ±	0 to +12V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	SA01 MIN	SA01 TYP	SA01 MAX	SA01-6 MIN	SA01-6 TYP	SA01-6 MAX	UNITS
ERROR AMP								
OFFSET VOLTAGE, initial	T_C = 25°C			10			*	mV
OFFSET VOLTAGE, vs. temperature	Full Temperature Range[5]			50			50	µV/°C
BIAS CURRENT, initial	T_C = 25°C			5			*	µA
BIAS CURRENT, vs. temperature	Full Temperature Range[5]			400			400	nA/°C
OFFSET CURRENT, initial	T_C = 25°C			1			*	µA
OFFSET CURRENT, vs. temperature	Full Temperature Range[5]			80			80	nA/°C
COMMON MODE VOLTAGE RANGE[4]		2		8	*		*	V
COMMON MODE REJECTION, DC[4]		75			*			dB
SLEW RATE			15			*		V/µS
OPEN LOOP GAIN[4]		75			*			dB
GAIN BANDWIDTH PRODUCT			2			*		MHz
OUTPUT								
TOTAL R_{ON}			.25			*		Ω
EFFICIENCY, 10A OUTPUT	V_S = 100V		97			*		%
SWITCHING FREQUENCY	Full temperature range[5]	35.3	42	48.7	35	42	49	KHz
CURRENT, continuous[4]		20			*			A
CURRENT, peak[4]		30			*			A
REFERENCE								
VOLTAGE	I_{REF} = 5mA	7.46	7.50	7.54	*	*	*	V
VOLTAGE VS. TEMP	Full temperature range[5]			50			50	PPM/°C
OUTPUT CURRENT				5			5	mA
LOAD REGULATION[4]			20	50		*	*	PPM/mA
LINE REGULATION			1			*		PPM/V
POWER SUPPLY								
VOLTAGE	Full temperature range[5]	16	50	100	16	50	100	V
CURRENT	I_{OUT} = 0, I_{REF} = 0, Full temperature range[5]		76	90		76	93	mA
CURRENT, shutdown	I_{REF} = 0			25			*	mA
SHUTDOWN								
TRIP POINT		.18		.22	*		*	V
INPUT CURRENT				100			*	nA
THERMAL[2]								
RESISTANCE, junction to case[4]	Full temp range, for each transistor			1.0			*	°C/W
RESISTANCE, junction to air[4]	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications[5]	–25		+85	–55		125	°C

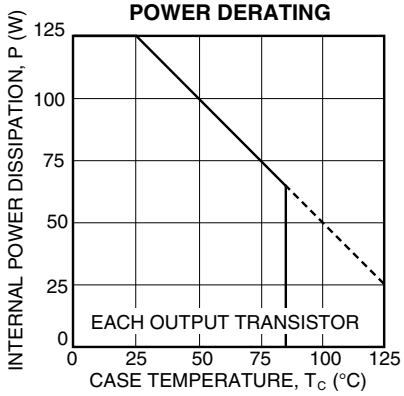
NOTES:
1. Each of the two active output transistors can dissipate 125W, however the N-channel will be about 1/3 of the total dissipated power. Internal connection resistance is .05Ω.
2. Unless otherwise noted: T_C = 25°C.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. Full temperature range specifications apply to the operating case temperature range as specified under THERMAL. For the SA01 these specifications are guaranteed but not tested. For the SA01-6 these specifications are tested over the SA01-6 operating case temperature range.

CAUTION

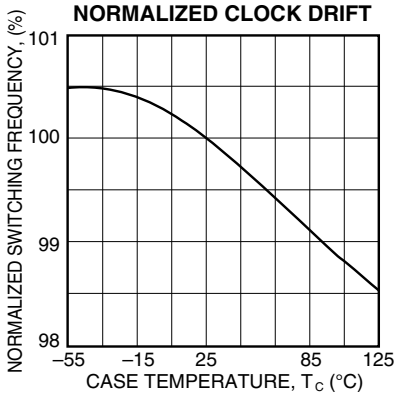
The SA01 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

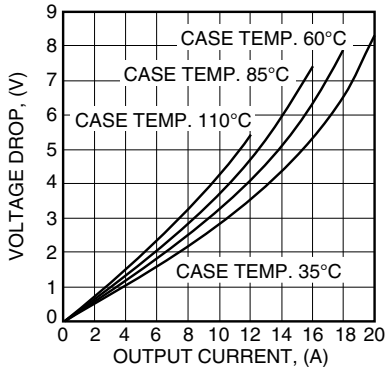
POWER DERATING



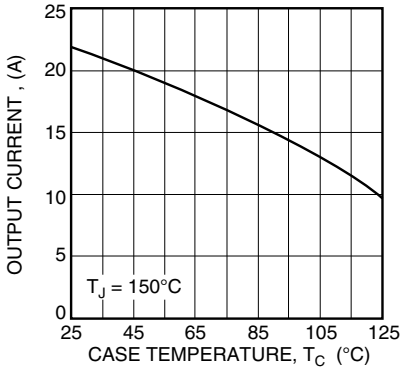
NORMALIZED CLOCK DRIFT



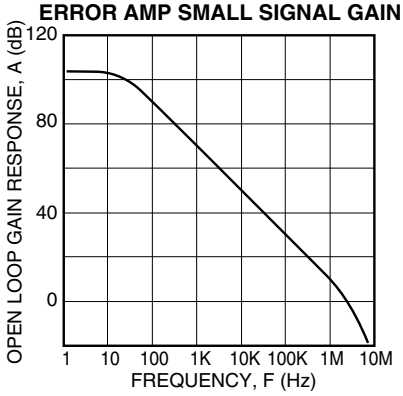
VOLTAGE DROP



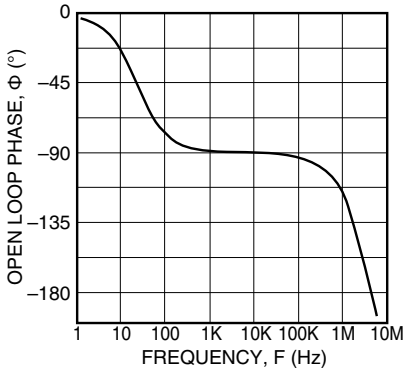
MAXIMUM CONTINUOUS OUTPUT



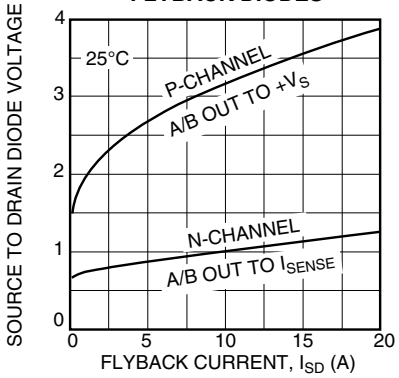
ERROR AMP SMALL SIGNAL GAIN



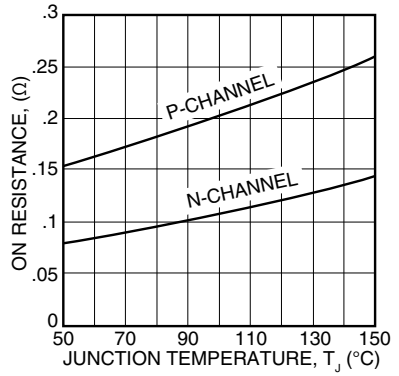
ERROR AMP SMALL SIGNAL PHASE



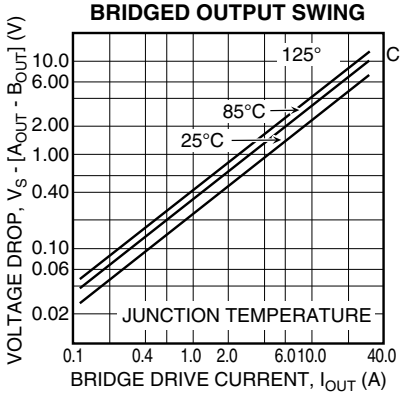
FLYBACK DIODES



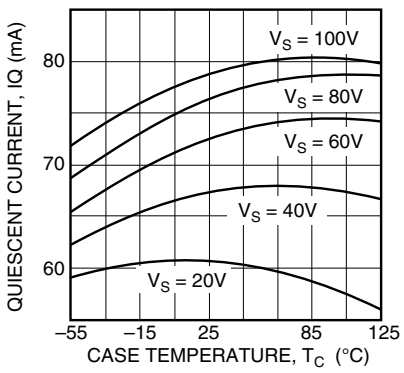
FET ON RESISTANCE



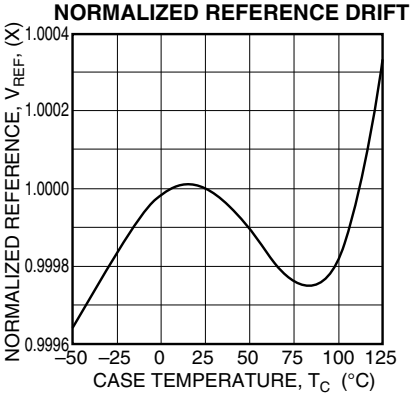
BRIDGED OUTPUT SWING



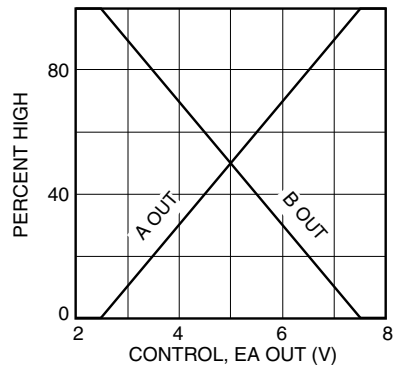
QUIESCENT CURRENT DRIFT



NORMALIZED REFERENCE DRIFT



DUTY CYCLE



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The current limit function sets a peak limit on current flow in pin 8 (Isense). This limits load current and also limits current in the event of a short of either output to +Vs. This circuit can trip anytime during the conduction period and will hold the output transistors off for the remainder of that conduction period.

For proper operation the current limit sense resistor must be connected as shown in the external connection diagram. It is recommended that the resistor be a non-inductive type. Load current flows in pin 8. No current flows in pin 10 (Shutdown/filter) so no error will be introduced by the length of the connection to pin 10. However, the voltage at pin 10 is compared to GND (pin 4) and an error could be introduced if the grounded end of R_{LIMIT} is not directly tied to pin 4. Good circuit board layout practice would be to connect R_{LIMIT} directly between pins 8 and 4.

Switching noise spikes will invariably be found at pin 8. The amplitude and duration will be load dependent. The noise spikes could trip the current limit threshold which is only 200 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 200 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. Suggested starting values are C_{FILTER} = .01µF, R_{FILTER} = 5k.

The required value of R_{LIMIT} may be calculated by:

$$R_{LIMIT} = .2\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current.

SHUTDOWN

The shutdown circuitry makes use of the internal current limiting circuitry. The two functions may be externally combined as shown below in Figure 1. R_{LIMIT} will normally be a very low value resistor and can be considered zero for this application. R_{SD} and R_{FILTER} form a voltage divider for the shutdown signal. After a suitable noise filter is designed for the current limit adjust the value of R_{SD} to give 317 mV of shutdown signal at pin 10 when the shutdown signal is high. This means pin 10 will reach the 200 mV trip point in about one time constant with low output current and less time as output current increases. The voltage at pin 10 is referenced to pin 4 (GND). C_{FILTER} will filter both the current limit noise spikes and the shutdown signal. Shutdown and current limit operate on each cycle of the internal switching rate. As long as the shutdown signal is high the output will be disabled.

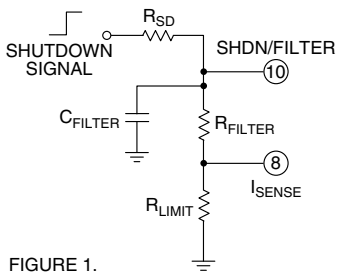


FIGURE 1.

PROTECTION CIRCUITS

There are two conditions which will latch all the output transistors off. The first of these conditions is activation of the high side current limit. Specifically, current in pin 7 ($+V_S$) is monitored. The DC trip level is about 35A and response time about 5us. As actual currents increase the response time decreases. The external fault generally associated with this condition is shorting one of the outputs to ground. However, a load fault can also activate this high side current limit if the current rise time is less than the response time of the filter discussed under "Current Limit". The second of these conditions is activation of any of the four output transistor over-temperature sensors at about 165°C. Ambient temperature, air flow, amplifier mounting problems and all the previously mentioned high current faults contribute to junction temperature. When either of these protection circuits are activated, the root fault must be corrected and power cycled to restore normal operation.

DEAD TIME

There is a dead time between the on and off of each output. The dead time removes the possibility of a momentary conduction path through the upper and lower transistors of each half bridge output during the switching interval. During the dead time all output transistors are off. Noise or flyback may be observed at the outputs during this time due to the high impedance of the outputs in the off state. This will vary with the nature of the load.

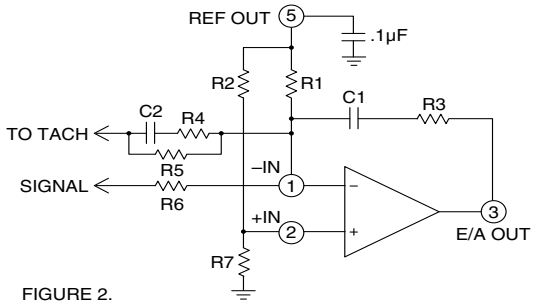


FIGURE 2.

ERROR AMPLIFIER

The internal error amplifier is an operational amplifier. For highest loop accuracy it is best to configure the op amp as an integrator (See Figure 2). Feedback can be adjusted with appropriate poles and zeroes to properly compensate the velocity loop for optimum stability.

The op amp is operated from a single supply voltage generated internally. The non-inverting input of the op amp does not have a common mode range which includes ground. R2 and R7 are used with the reference voltage provided at pin 5 to bias the non-inverting input to +5 volts, which is approximately half of the voltage supplied internally to the op amp. Similarly, R1 and the parallel combination of R5 R6 are selected to bias the inverting input also at +5 volts. Resistors R1 R2 must be matched. Likewise the parallel combination of R5 R6 must be matched with R7. The source impedances of the tach and the signal source may affect the matching and should be considered in the design.

This data sheet has been carefully checked and is believed to be reliable, however, no responsibility is assumed for possible inaccuracies or omissions. All specifications are subject to change without notice.

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