Advanced PWM Controller for Bus Converters

FEATURES

- **Programmable, Load Depended Off Time Control**
- **Frequency Controlled Start Up Allows Small Output Inductor, Low Ripple and Constant Current Start with Large Output Capacitor**
- **Two 0.2-A Push-Pull Outputs Provide Matched Control Signals D to External Drivers**
- **Two Additional 1- D Outputs for Optimal Use of Self-Driven or Control Driven Synchronous Rectifiers**
- **Unregulated, Fixed Volt-Second or Fixed Frequency Modes set by User**
- **Two, 1.5% Overall Accuracy Reference Voltage Options: 5-V for UCC28230 and 3.3-V for UCC28231**
- **Resistor Programmable Switching Frequency up to 1 MHz**
- **Cycle-by-Cycle Current Limit Allows Parallel Operation with Droop Based Current Sharing**
- **Single External Capacitor sets Soft-Start and Over Current Hiccup Mode Parameters with Restart**
- **Severe Short Circuit Hiccup with Restart or Latch Off Protection Option by External Resistor**
- **Input Under Voltage Lock Out**
- **Thermal Shutdown**
- **Thermally Enhanced 3 mm × 2 mm SON-12 and TSSOP-14 Package Options**

APPLICATIONS

- **Intermediate Bus Isolated Converters**
- **DC-to-DC Transformers**

DESCRIPTION

The UCC28230, UCC28231 PWM bus controllers are optimized for use in high efficiency, high power density, unregulated intermediate bus converters. Topologies include push-pull, half-bridge and full-bridge. External drivers, such as the UCC27200 120-V high-side/low-side drivers, can be used with this controller.

Low cost, small size and highly efficient solutions are provided by innovations such as:

- Start-up frequency control circuit allowing small output inductor and the ability to start with large intermediate bus capacitor.
- Load depended off-time control set by user.

Additional 1-D control outputs can be used for primary winding clamping in self-driven output synchronous rectifier applications or as drive signals for the control-driven synchronous rectifier.

Cycle-by-cycle current limit prevents overstresses of converter. If the over current condition causes less than 80% duty cycle at the output, then after a programmed time the controller proceeds into periodical shutdown and restart hiccup mode.

The UCC28230 provides 5 V, and the UCC28231 provides 3.3-V precision reference voltages with 1.5% overall accuracy and 10-mA output current. This reference voltage can be used to supply housekeeping circuit and/or microcontroller. The precision reference voltage can also be used for accurate setting of system parameters.

Other features include under-voltage lockout, thermal shut down, programmable soft start, over-current hiccup mode and short circuit protection with internal restart by default that can be set into latch-off mode by an external resistor.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TYPICAL APPLICATION DIAGRAMS

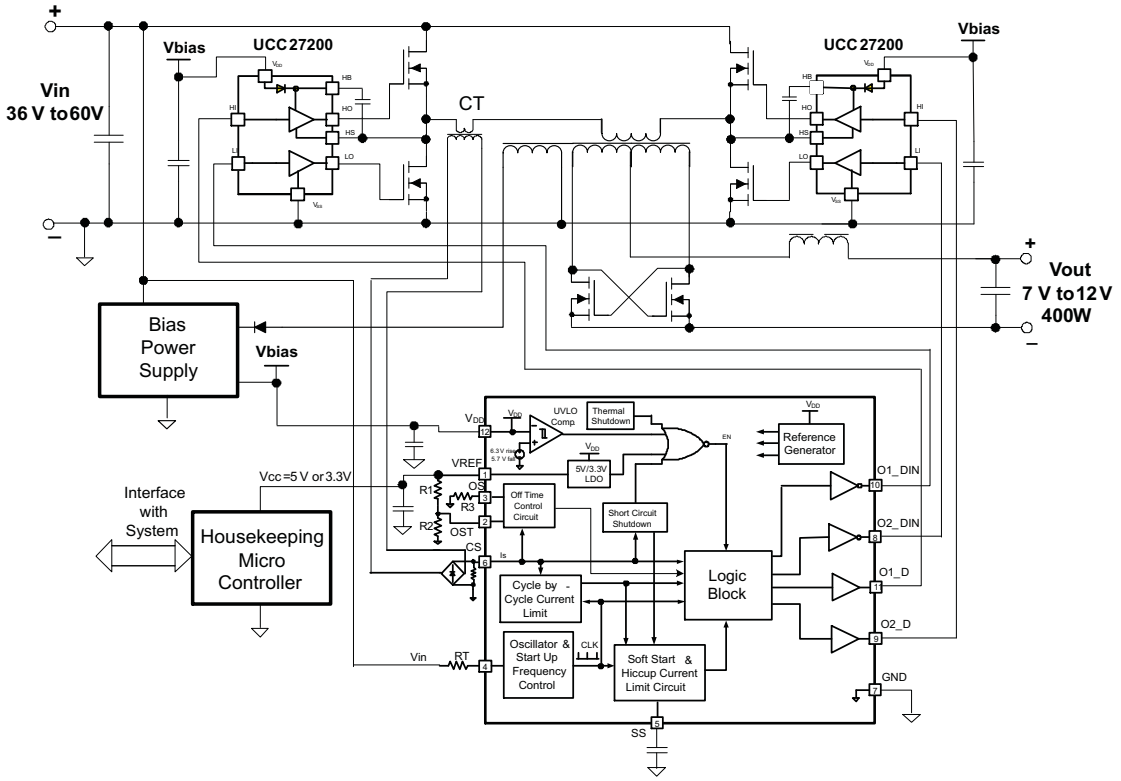


Figure 1. Full-Bridge Bus Converter

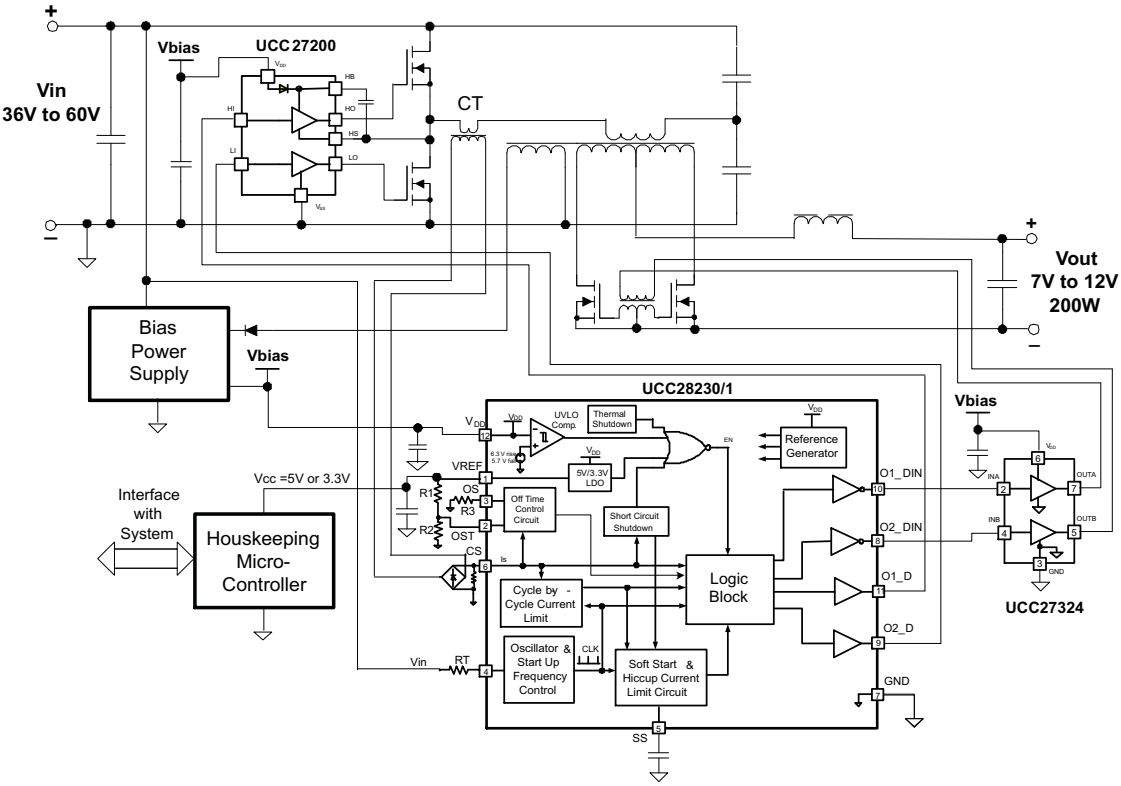
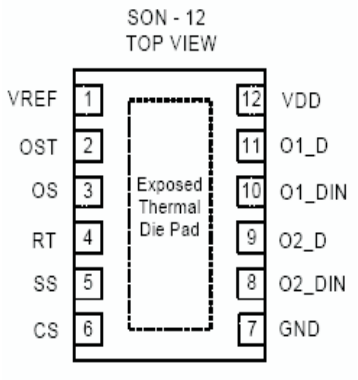
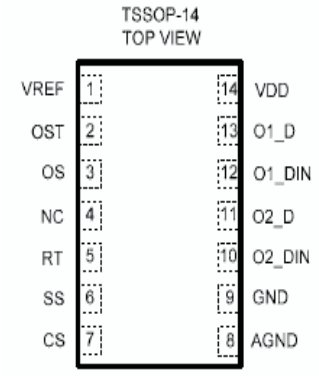


Figure 2. Half-Bridge Bus Converter with Control-Driven Synchronous Rectifier

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PINOUT CONFIGURATION





ORDERING INFORMATION(1) (2)

TEMPERATURE RANGE, $T_A = T_J$	REFERENCE VOLTAGE	PACKAGE	TAPE and REEL QTY	PART NUMBER
–55°C to +125°C	5 V	Plastic 12-pin SON (DRN)	.250	UCC28230DRNT
	5 V		3000	UCC28230DRNR
	3.3 V		250	UCC28231DRNT
	3.3 V		3000	UCC28231DRNR
	5 V	Plastic 14-pin TSSOP (PW)	250	UCC28230PW
	5 V		2000	UCC28230PWR
	3.3 V		250	UCC28231PW
	3.3 V		2000	UCC28231PWR

(1) The 12-pin SON (DRN) and 14-pin TSSOP packages use Pb-Free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255-260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.

(2) The pad underneath the center of the IC is a thermal substrate. The PCB “thermal land” design for this exposed die pad should include thermal vias that drop down and connect to one or more buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the DRN to achieve its full thermal potential. This pad is also internally connected to GND pin.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (1) (2)(unless otherwise noted)

PARAMETER		VALUE	UNIT
V_{DD} (3)	Input supply voltage range	–0.3 to 20.0	V
	O1_D, O2_D, O1_DIN, O2_DIN	–0.3 to V_{DD} +0.3	
	Inputs voltages on OS, CS, SS, RT, OST	–0.3 to 6.3	
	Output voltage on VREF	–0.3 to 5.6	
HBM	ESD rating	2k	
CDM		500	
	Continuous total power dissipation	See Dissipation Rating Table	
T_J	Operating virtual junction temperature range	–55 to +150	°C
T_A	Operating ambient temperature range	–55 to +125	
T_{stg}	Storage Temperature	–65 to +150	
	Lead Temperature (Soldering, 10 sec.) PW Package	+300	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(3) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.

DISSIPATION RATINGS(1)

BOARD	PACKAGE	θ_{JC} (°C/W) JUNCTION TO CASE	θ_{JA} (°C/W) JUNCTION TO AMBIENT	θ_{JP} (°C/W) JUNCTION TO PAD	θ_{JB} (°C/W) JUNCTION TO BOARD
High-K(2)	DRN		70.66	15	37.66
	PW	2.71	97.65	2.07	

(1) These thermal data are taken at standard JEDEC test conditions and are useful for the thermal performance comparison of different packages. The cooling condition and thermal impedance $R_{\theta JA}$ of practical design is specific.
(2) The JEDEC test board JESD51-5 with direct thermal pad attach, 3-inch × 3-inch, 4-layer with 1-oz internal power and ground planes and 2-oz top and bottom trace layers (preliminary data based on modeling)

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range	7	12	17	V
	Operating junction temperature range	–55		125	°C

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ELECTRICAL CHARACTERISTICS(1)

V_{DD} = 12V, 1-µF capacitor from V_{DD} and VREF to GND, $T_A = T_J$ = –55°C to 125°C, RT = 49.9 kΩ connected to 4.4V supply to set Fsw = 100 kHz (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Currents							
$ID_{DD(off)}$	Startup current		V_{DD} = 5.2 V		150	200	µA
I_{DD}	Operating supply current				1.5	2.5	mA
Under Voltage Lockout							
	Start threshold			5.9	6.3	6.9	V
	Minimum operating voltage after start			5.3	5.7	6.2	
	Hysteresis			0.55	0.6	0.75	
Soft Start (SS PIN, Figure 41, Figure 44)							
I_{SS}	Charge current		V_{SS} = 0 V	–30	–25	–20	µA
V_{SS_STD}	Shutdown/restart/reset threshold			0.3	0.55	0.68	V
V_{SS_FP}	Soft-start first pulse threshold			0.68	0.85	1.1	
V_{SS_PU}	Pull up threshold			3.3	3.5	3.8	
V_{SS_CL}	Clamp voltage			4.3	4.5	4.8	
Off-Time Programming (Figure 33)							
T_{OFF5}	Off time between O1_D and O2_D	UCC28230	OS = 8.45 kΩ, CS = 0.3 V, OST = 1 V	32	40	50	ns
T_{OFF3}	Off time between O1_D and O2_D	UCC28231		30	40	53	
T_{DT}	Dead time between O1_D, O1_DIN and O2_D, O2_DIN			10	16		
ΔT_{OFF}	Off time matching				2		
T_{OFFR5}	Off time between O1_D and O2_D	UCC28230	OS = 8.45 kΩ, CS = 0 V, OST = VREF	32	40	50	
T_{OFFR3}	Off time between O1_D and O2_D	UCC28231		30	40	53	
T_{DTREF}	Dead time between O1_D, O1_DIN and O2_D, O2_DIN			10	16		
ΔT_{OFFR}	Off time matching				2		
I_{HYST}	Hysteresis current source				10		µA
T_{OFFMAX}	Maximum off time at low CS		OS = 8.45 kΩ, OST = 1 V, CS = CS_{TH}– 0.03 V	165		235	ns
Switching Frequency at O1_D and O2_D Outputs							
F_{SWNOM}	Nominal frequency		V_{SS} = 4 V	92	100	108	kHz
F_{SWMAX}	Maximum frequency		V_{SS} = 1.8 V	425	550	675	
VREF Output Voltage							
V_{REF5}	VREF total output range	UCC28230	0 ≤ IR ≤ 10 mA; V_{DD} = from 7 V to 17 V, –55°C ≤ T_J ≤ 125°C	4.925	5	5.075	V
V_{REF3}		UCC28231		3.25	3.3	3.35	
I_{SCC}	Short circuit current		VREF = 0 V	–35	–25	–12	mA

(1) Typical values for T_A = 25°C

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ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 12V, 1-µF capacitor from V_{DD} and VREF to GND, $T_A = T_J$ = –55°C to 125°C, RT = 49.9 kΩ connected to 4.4V supply to set Fsw = 100 kHz (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Sense, Cycle-by-Cycle Current Limit With Hiccup, Short Circuit Protection With Latch Off						
V_{CS_LIM}	CS pin cycle-by-cycle threshold		0.48	0.5	0.515	V
T_{CS}	CS to O1_D and O2_D propagation delay	Input pulse at CS from 0.3 V to 0.6 V with 0.03 V/ns slew rate		100		ns
T_{BL}	Leading edge blanking time by internal filter	Input pulse at CS from 0.3 V to 0.6 V with 0.03 V/ns slew rate		50		
I_{DS}	Discharge current to set cycle-by-cycle current limit duration (Figure 41)	CS = 0.6 V, V_{SS} = 4 V	15	20	25	µA
	Hiccup OFF time threshold		3.1	3.4	3.7	V
I_{HCC}	Discharge current to set Hiccup Mode OFF Time (Figure 41, Figure 44)		1.9	2.5	3.1	µA
V_{CS_SC}	CS pin short circuit protection threshold (Figure 44)		0.65	0.7	0.75	V
Outputs O1_D, O2_D, O1_DIN, O2_DIN						
	Sink/Source peak current(2)			0.2		A
	Rise time	C_{LOAD} = 100 pF		12	25	ns
	Fall time	C_{LOAD} = 100 pF		10	25	
RSRC	Output source resistance	I_{OUT} = 20 mA	10	20	35	Ω
RSINK	Output sink resistance	I_{OUT} = 20 mA	5	15	30	
	Duty cycle matching	Pins 7 and 9 pulses matching at F_{SW} = 100 kHz		35		ns
Thermal Shutdown						
	Rising threshold(3)		150	160	170	°C
	Falling threshold(3)		130	140	150	
	Hysteresis			20		

(2) Output sink/source peak current value, defined by equation I_P = 100 pF × dV/dt where dV/dt is taken from the output rise and fall switching waveforms. It is not tested in production. Characterization is available upon request.
(3) Thermal shutdown is not tested in production. Characterization is available upon request

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FUNCTIONAL BLOCK DIAGRAMS

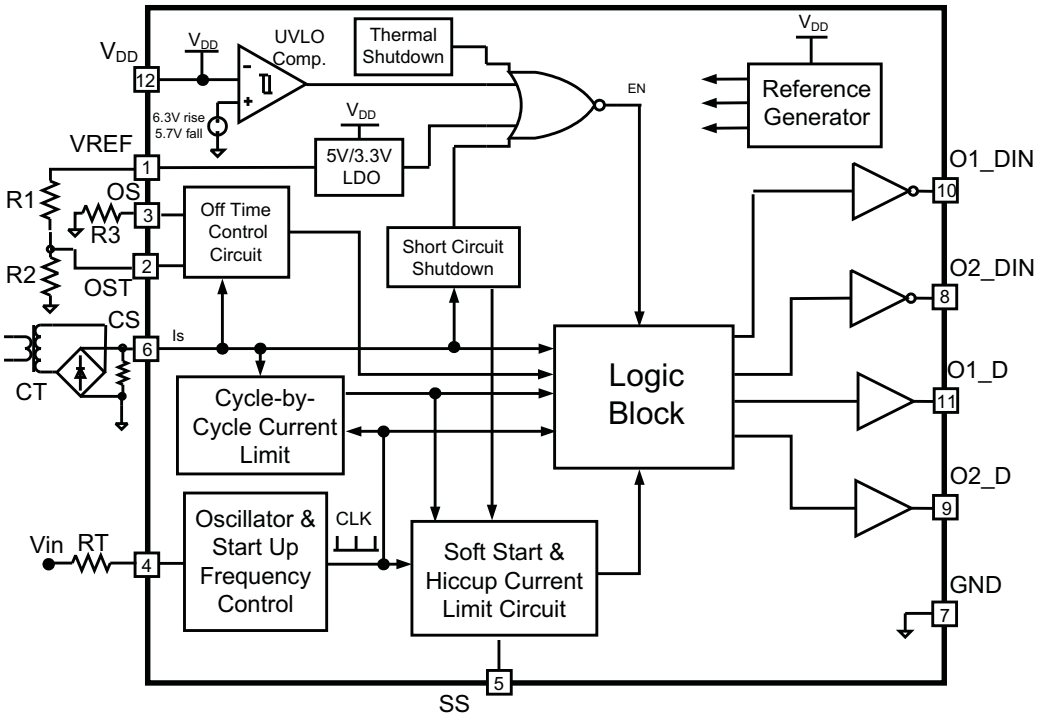


Figure 3. SON-12 Package

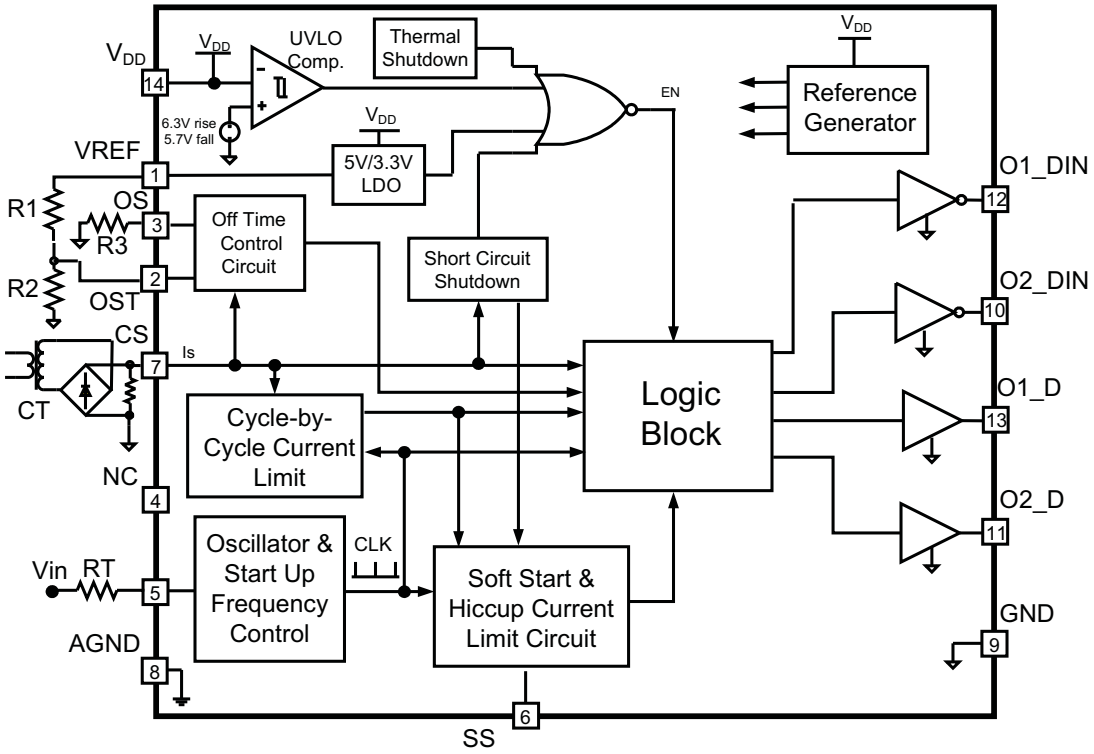


Figure 4. TSSOP-14 Package

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TERMINAL FUNCTIONS

TERMINAL			I/O	FUNCTION
DFN-12 PIN#	TSSOP-14 PIN#	NAME		
1	1	VREF	O	±1.5% accurate 5 V for UCC28230 and 3.3 V for UCC28231, 10-mA output reference voltage with short circuit protection that can be used for fixed switching frequency setting and/or for housekeeping microcontroller. Place decoupling capacitor in 1 μF to 2.2 μF range from this pin to GND.
2	2	OST	I	Off time control threshold pin uses a resistor divider to set current level as percentage of current limit threshold.
3	3	OS	I	Nominal off time T_{OFF} and dead time T_{DT} set pin. An external resistor connected between this pin and GND sets the dead time and nominal off time.
	4	NC		Not connected pin, TSSOP-14 only.
4	5	RT	I	Oscillator timing input pin. The external resistor which is connected between this pin and V_{IN} sets the oscillator frequency which varies with V_{IN}. Tying the external resistor to VREF sets fixed frequency operation independent of V_{IN}.
5	6	SS	I/O	Input to adjustable soft-start,and hiccup mode circuit. Place soft-start capacitor from this pin to GND. The internal charge/discharge current I_{SS} and an external capacitor value set the soft-start timing, duration of cycle-by-cycle current limit and controller turn-off time for hiccup mode operation.
6	7	CS	I	Current sensing pin used for cycle-by-cycle current limit, short circuit protection and off time control.
	8	AGND		Analog ground, TSSOP-14 only.
7	9	GND		Ground pin connected to thermal pad. All signals are referenced to this node.
8	10	O2_DIN	O	0.2-A sink/source switching output pin to an external driver providing 1-D pulse.
9	11	O2_D	O	0.2-A sink/source switching output pin to an external driver providing D pulse.
10	12	O1_DIN	O	0.2-A sink/source switching output pin to an external driver providing 1-D pulse.
11	13	O1_D	O	0.2-A sink/source switching output pin to an external driver providing D pulse.
12	14	VDD	I	Connect this pin to a 7-V to 17-V bias supply. Place a high quality at least 1-μF ceramic bypass capacitor from this pin to GND.

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TYPICAL CHARACTERISTICS

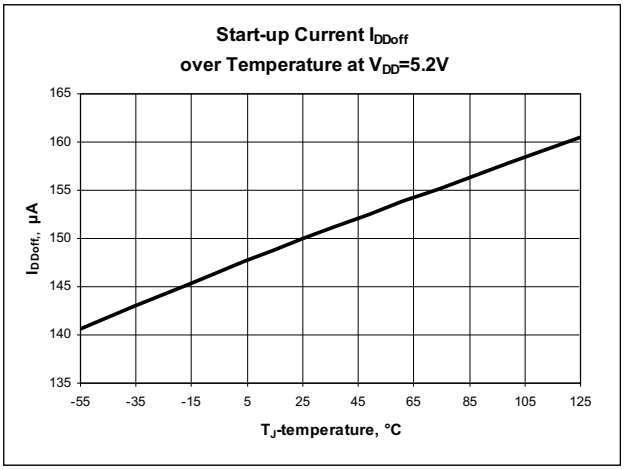


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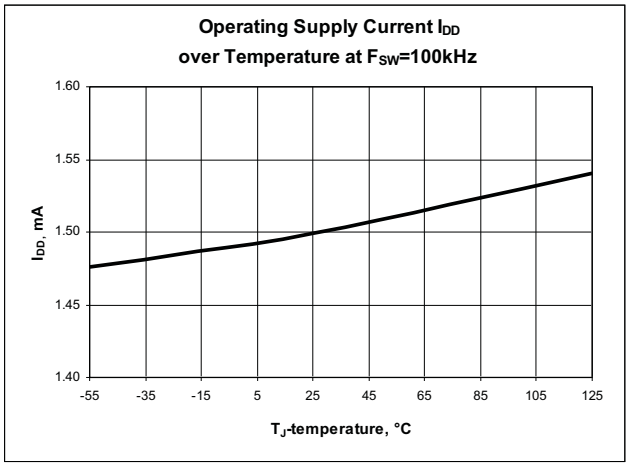


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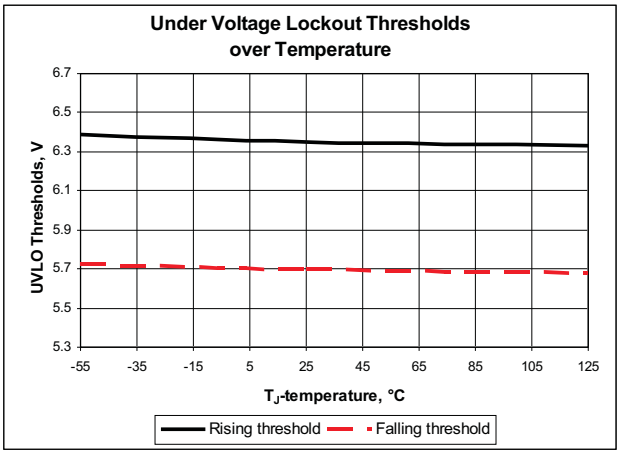


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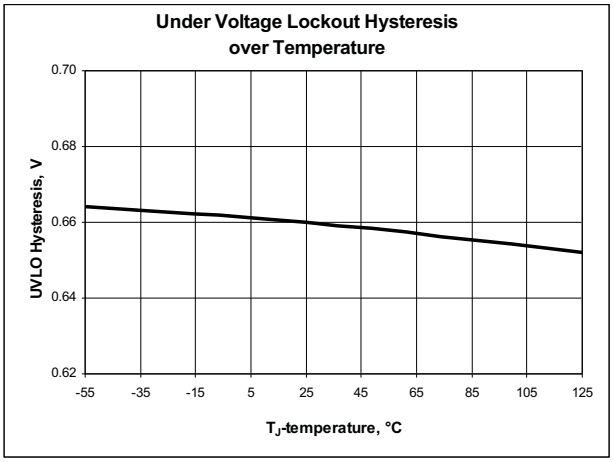


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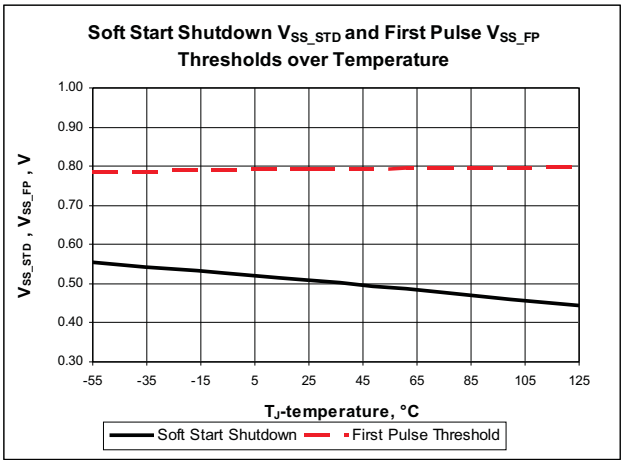


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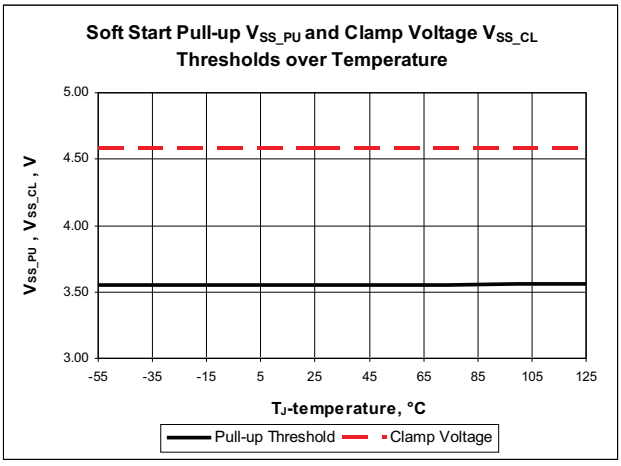


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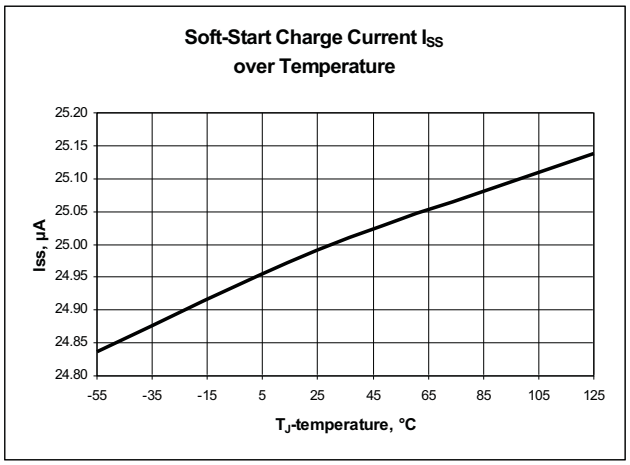


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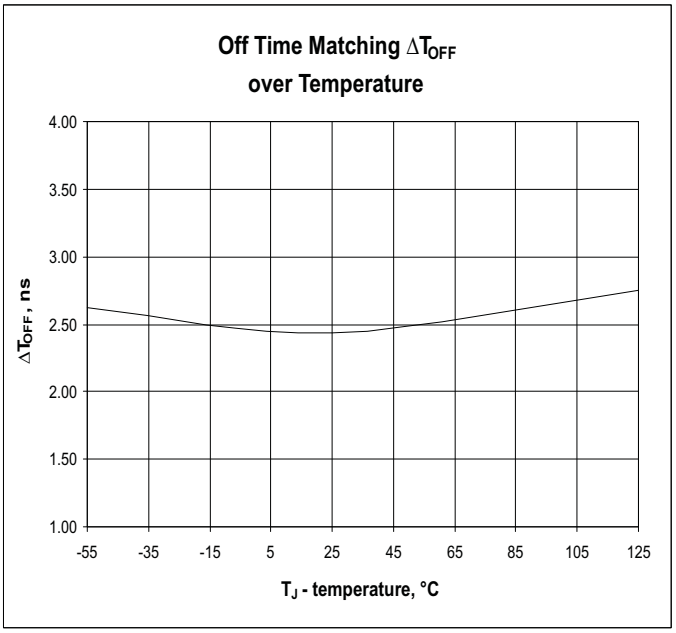


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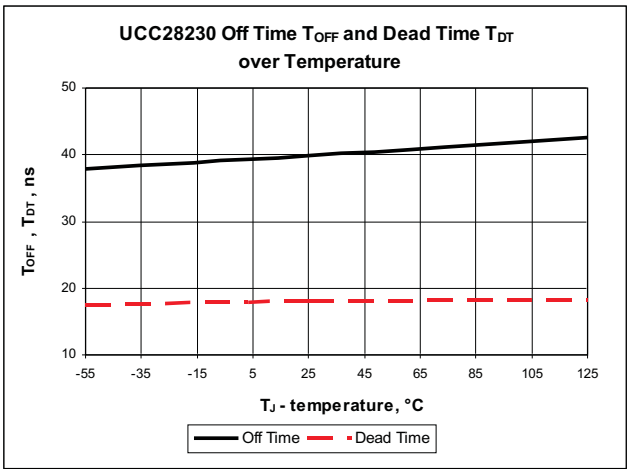


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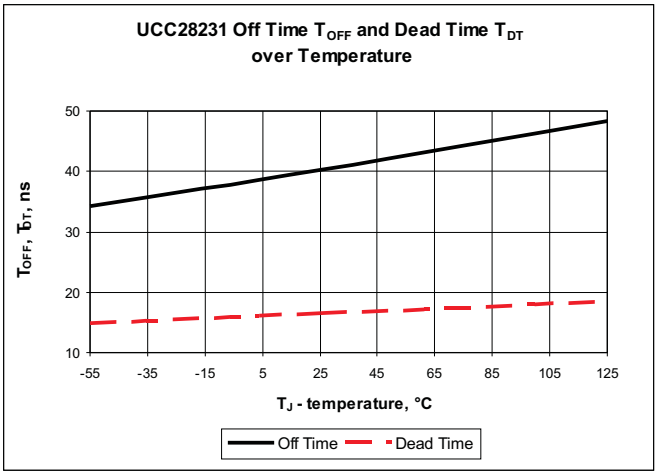


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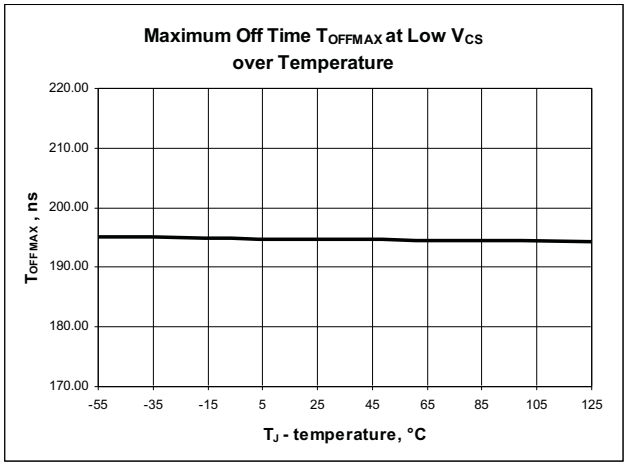


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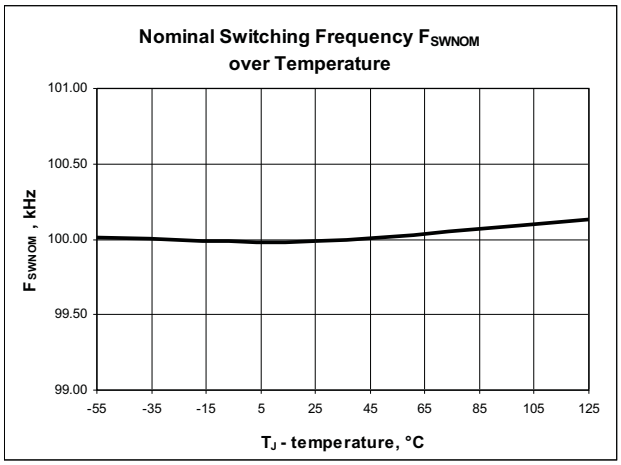


Figure 16.

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TYPICAL CHARACTERISTICS (continued)

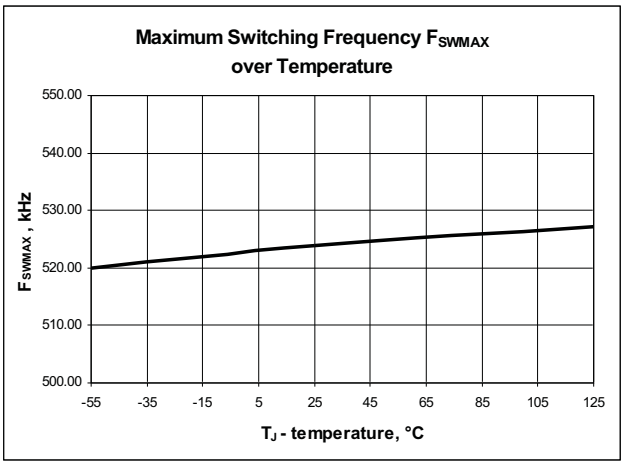


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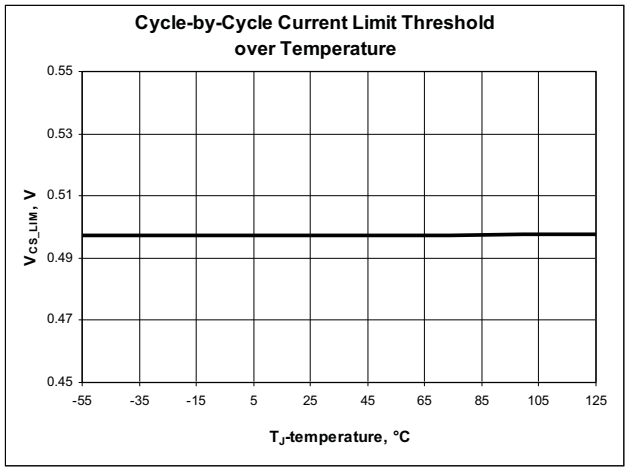


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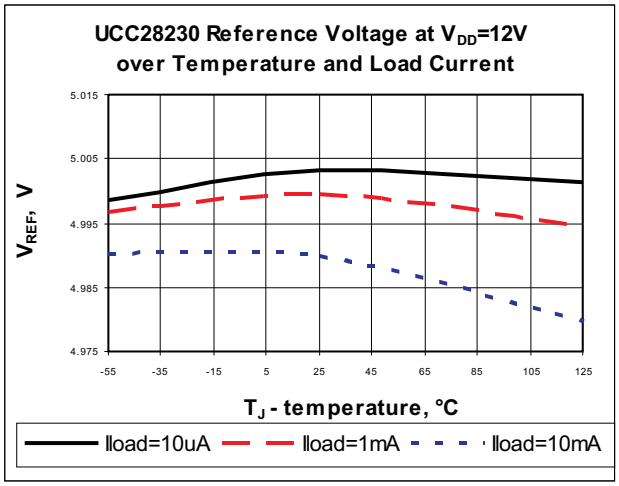


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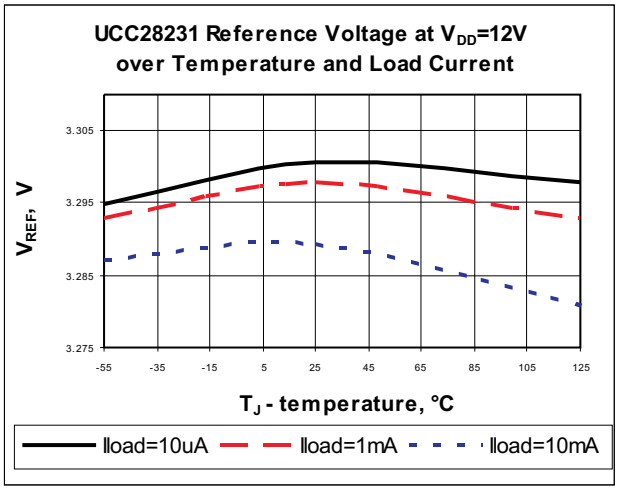


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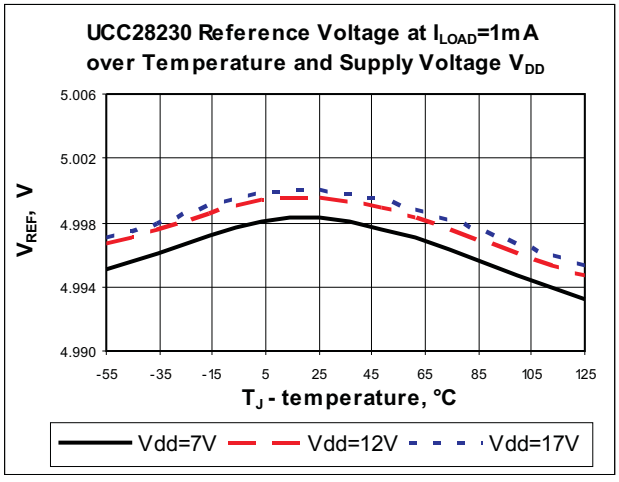


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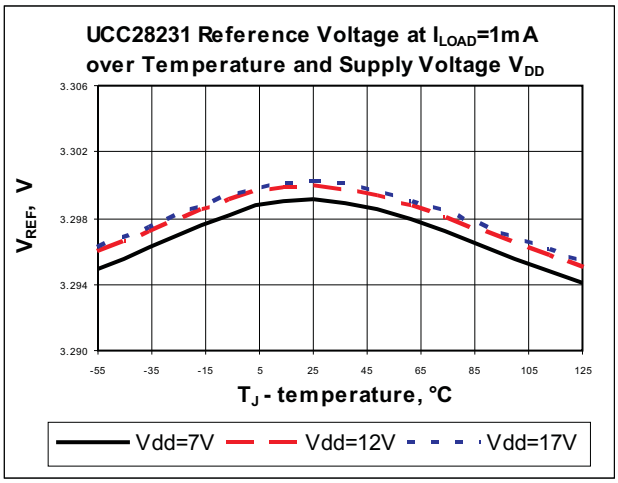


Figure 22.

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TYPICAL CHARACTERISTICS (continued)

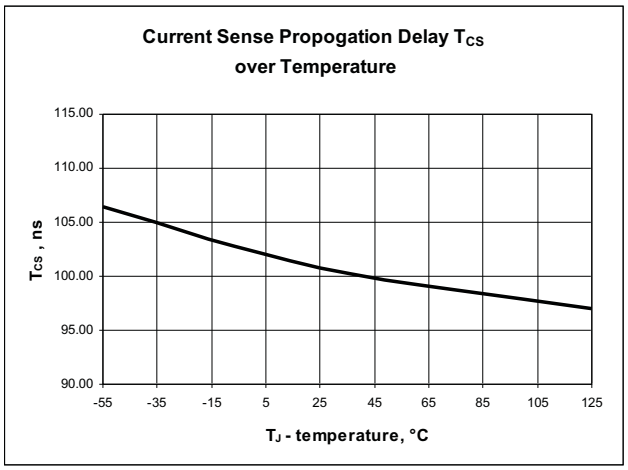


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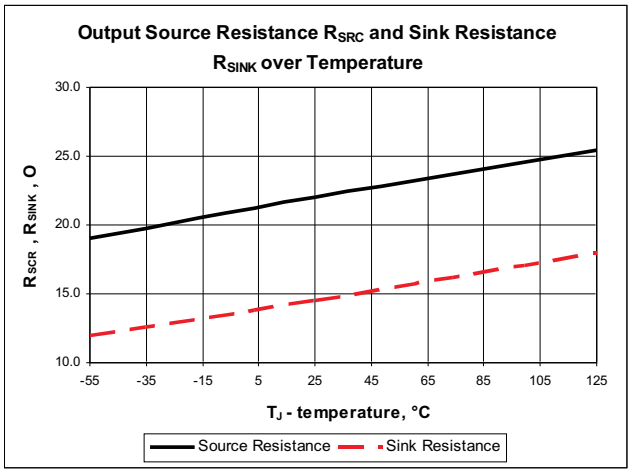


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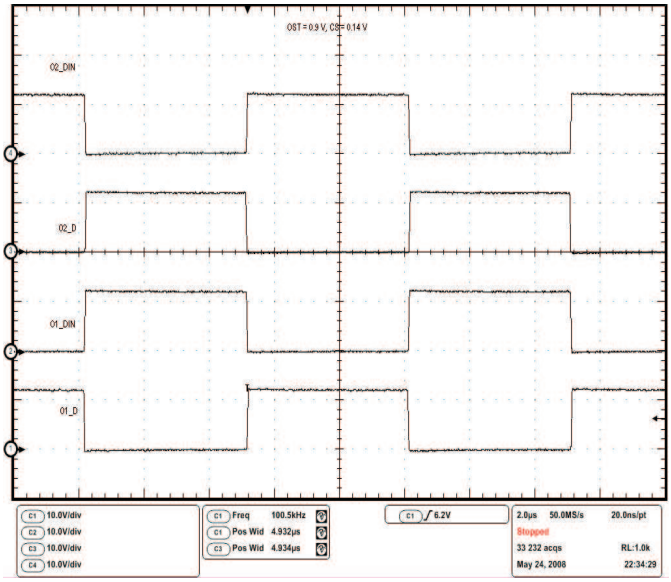


Figure 25. O1_D and O2_D Duty Cycle Matching at V_{CS} = 0.14 V and V_{OST} = 1 V

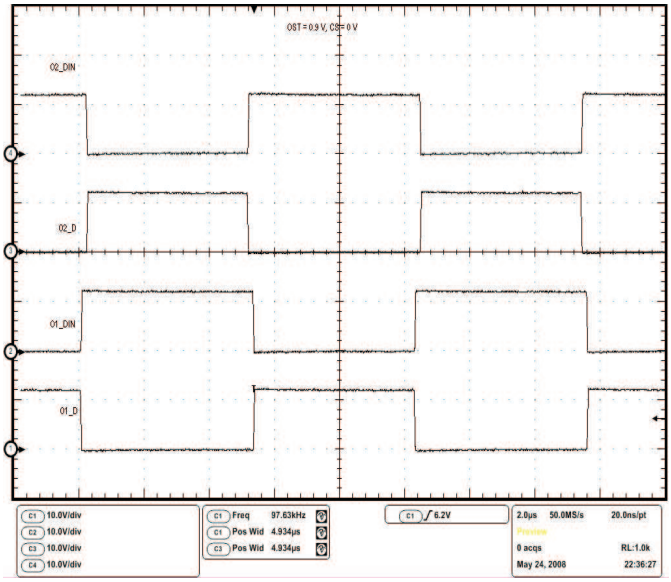


Figure 26. O1_D and O2_D Duty cycle Matching at V_{CS} = 0.0 V and V_{OST} = 1 V

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TYPICAL CHARACTERISTICS (continued)

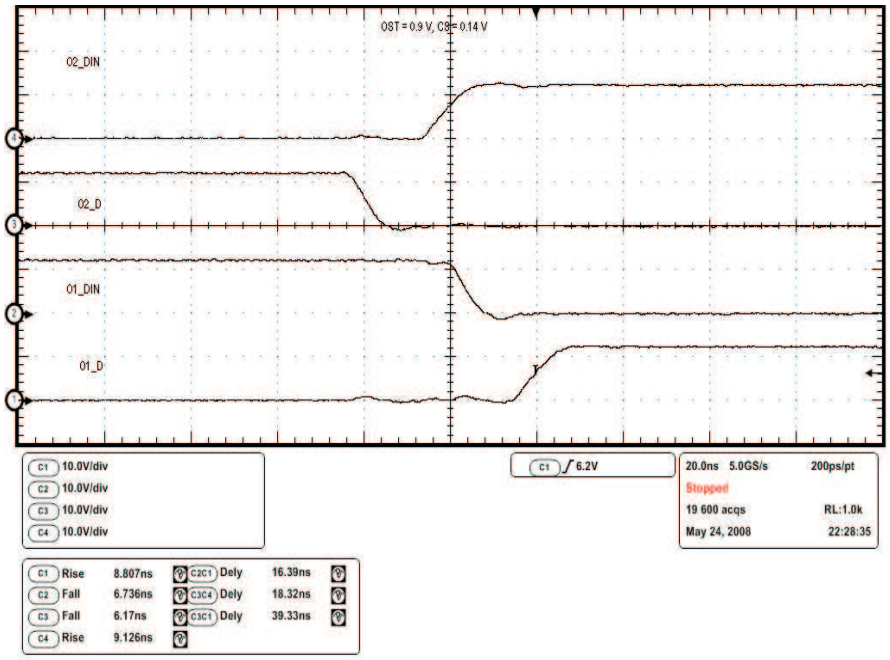


Figure 27. Output Waveforms During First Half Switching Cycle at V_{CS} = 0.14 V and V_{OST} = 1 V

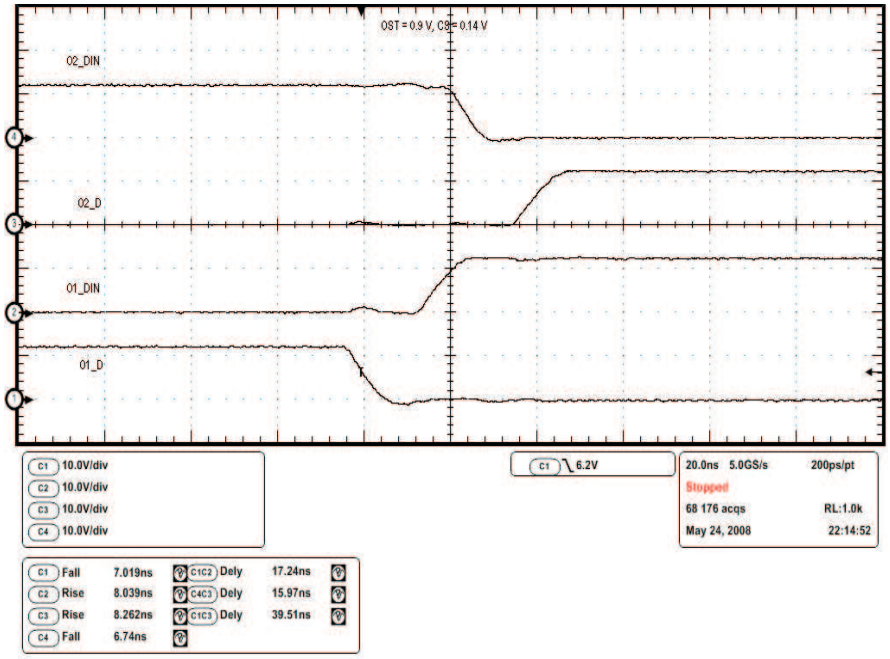


Figure 28. Output Waveforms During Second Half Switching Cycle at V_{CS} = 0.14 V and V_{OST} = 1 V

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TYPICAL CHARACTERISTICS (continued)

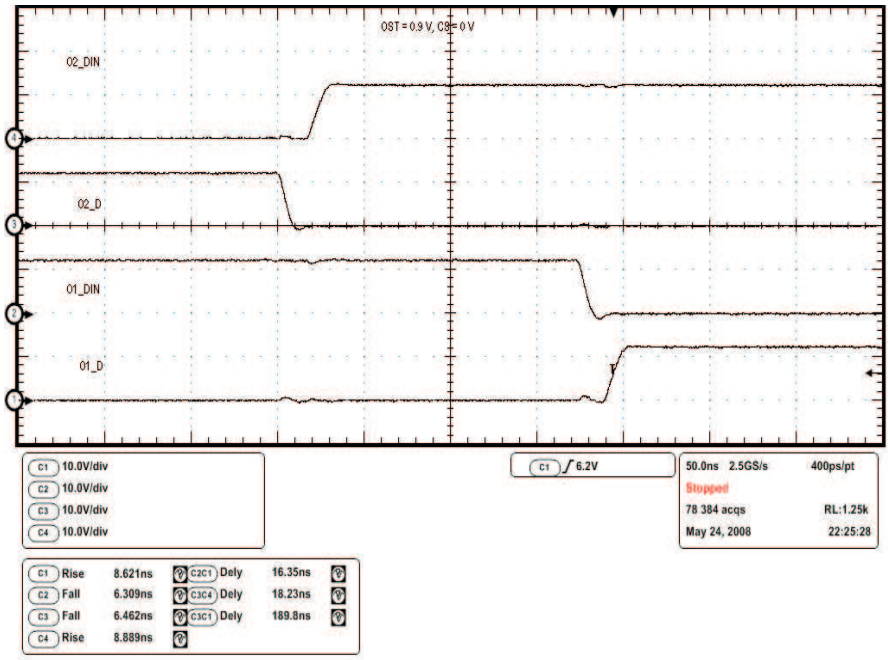


Figure 29. Output Waveforms During First Half Switching Cycle at V_{CS} = 0 V and V_{OST} = 1 V

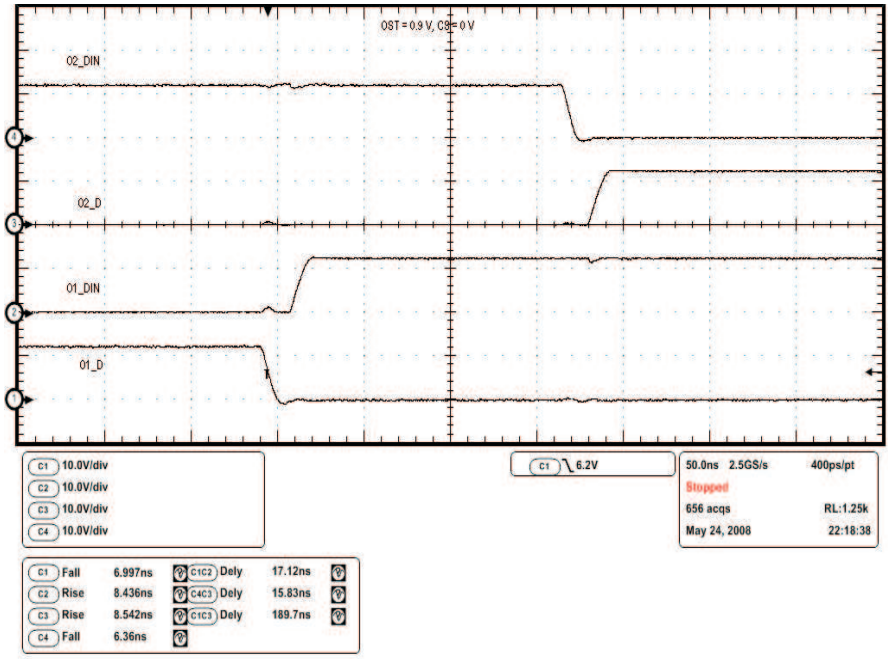


Figure 30. Output Waveforms During Second Half Switching Cycle at V_{CS} = 0 V and V_{OST} = 1 V

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DETAILED DESCRIPTION

Start-Up Protection Logic

Before the controller allows the start up, the following conditions must be met:

- VDD voltage exceeds rising UVLO threshold 6.3 V typical
- The reference voltage 5 V for UCC28230 or 3.3 V for UCC28231 is available
- Junction temperature is below the thermal shutdown threshold 130°C min
- The voltage at soft-start capacitor is not below 0.55 V typical

If all those conditions are met, an internal enable signal EN is generated that initiates the soft start process. The duty cycle during the soft start is defined by the voltage at the SS pin or by cycle-by-cycle current limit circuit depending on load conditions.

Internal Oscillator and Converter Switching Frequency

The oscillator frequency is set by an external resistor at RT pin (see Figure 3 and Figure 4). The oscillator frequency F_{OSC} is twice that of converter switching frequency F_{SW}. The oscillator performs the following main functions:

- Generates clock signal CLK to synchronize internal functional blocks
- By changing the switching frequency during the start up and cycle-by-cycle current limit, the oscillator limits the current ripple at the output inductor allowing the use of small output inductor and start with large output capacitor

Oscillator can operate in the following modes:

- Fixed volt-second mode of operation when the resistor RT is connected between V_{IN} and RT pin. In this mode the switching frequency increases in accordance to an input voltage rise
- Fixed switching frequency mode when the resistor RT is connected between VREF and RT pins.

The switching frequency of converter is defined as $F_{SW(nom)} = 1/T_{SW(nom)}$ (see Figure 33). Equation 1 is used to calculate the nominal switching frequency of the converter and its transformer.

$$F_{SW(nom)} = \frac{1}{\frac{RT}{2500 \times (V_{IN} - 2.4)} + 1.2 \times T_{OFF}} \quad (1)$$

Where RT is in kΩ, V_{IN} is in volts, T_{OFF} is in ms and $F_{SW(nom)}$ is in kHz.

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In most applications, T_{OFF} is set at about 40~50 ns, which can be neglected compared to the total oscillator period. Therefore Equation 1 can be simplified as:

$$F_{SW(nom)} = 2500 \times \frac{(V_{IN} - 2.4)}{RT} \quad (2)$$

In this equation RT is in kΩ, V_{IN} is in volts and $F_{SW(nom)}$ is in kHz.

Figure 31 shows how the nominal switching frequency of converter depends on value of resistor RT, and Figure 32 shows how the switching frequency changes over the input voltage range in case of fixed volt-second mode of operation. The T_{OFF} is set to 40 ns for both figures.

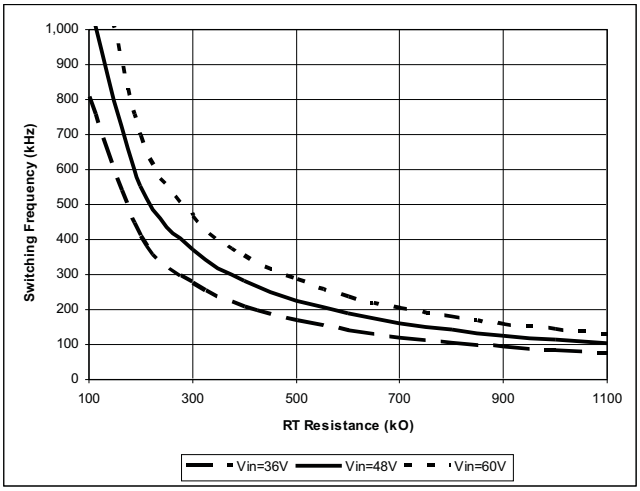


Figure 31. Nominal Switching Frequency of Converter vs Resistor RT

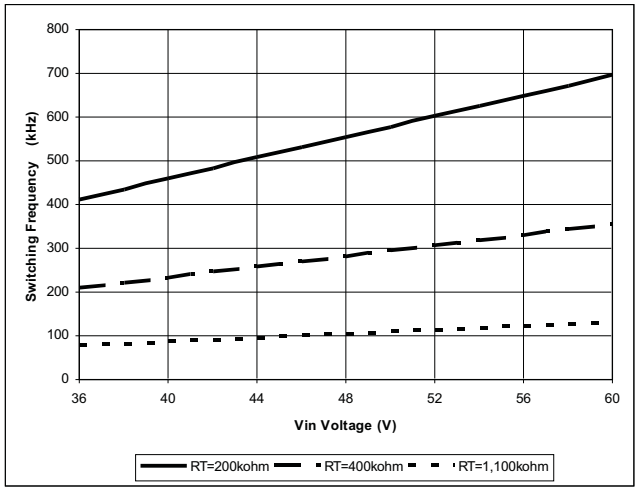


Figure 32. Switching Frequency Variation Over the Input Voltage for Fixed Volt-Second Mode of Operation

Fixed frequency mode of operation can be achieved by connecting the resistor RT between VREF and RT pins. In such case the switching frequency is defined by the following Equation 3, where the impact of T_{OFF} is neglected as well.

$$F_{SW(nom)} = 2500 \times \frac{(VREF - 2.4)}{RT} \quad (3)$$

In this equation the RT is in kΩ, VREF is in volts and $F_{SW(nom)}$ is in kHz.

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Output Signals

The UCC28230/1 has two push-pull outputs O1_D and O2_D that provide D pulse signals to external drivers. The additional two outputs O1_DIN and O2_DIN provide 1-D output pulses with dead time between D and 1-D pulses to avoid shoot-through currents. Such combination of outputs allows use of UCC28230/1 either with self-driven synchronous rectifier, or with the control-driven synchronous rectifier in push-pull, half-bridge or full-bridge configuration.

For the full-bridge self-driven rectifier configuration, outputs O1_D and O2_D control high-side MOSFETs while outputs O1_DIN and O2_DIN control low-side MOSFETs thus shorting the primary winding during (1-D) switching cycle. This avoids number of issues related to self-driven rectification such as start up disabling, reverse current during parallel operation, tendency to oscillate during low duty cycles. The applications circuit for this configuration is shown on Figure 1 and the output signal timing diagrams are shown in Figure 33.

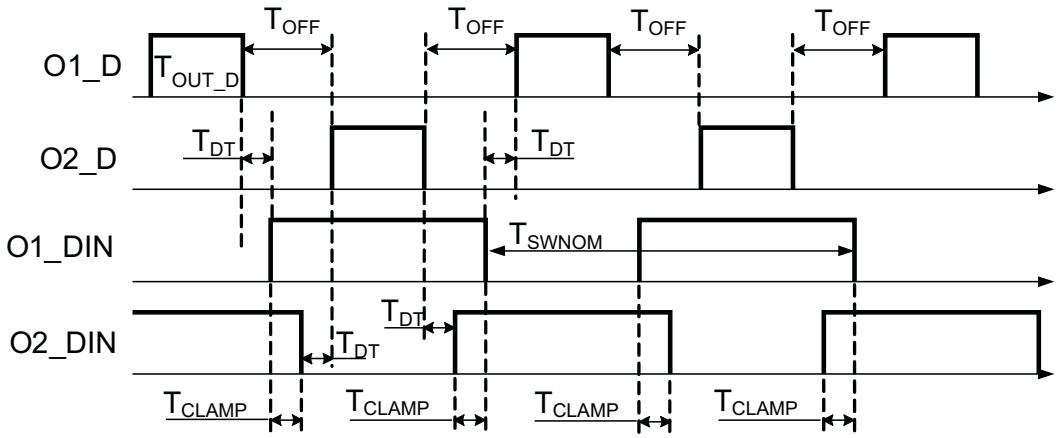


Figure 33. D and (1-D) Output Pulses Providing Dead Time T_{DT} in Each Leg and the Off Time T_{OFF} Between Upper FETs That Includes Some Overlapping Time T_{CLAMP}.

In the steady state condition an unregulated bus converter operates at maximum duty cycle thus having minimum overlapping T_{CLAMP} of (1-D) outputs. During start up or cycle-by-cycle current limit, the duty cycle can be very low, so (1-D) output pulses occupy most of the switching cycle time. This provides zero voltage clamping of the transformer's primary winding. The UCC28230/1 also includes an off-time control feature. This feature allows user to increase off time T_{OFF} when the converter output current is below a programmable current threshold. This feature reduces switching losses of the synchronous rectifier at light load and it is described in detail in Offtime Control Circuit section.

For the control driven half-bridge topology, the outputs O1_D and O2_D provide control pulses for the high-side and low-side MOSFETs, while the outputs O1_DIN and O2_DIN can be used to drive the pulse transformers providing control signals to the secondary-side MOSFET rectifiers as shown in Figure 2.

In case of full-bridge topology with the control-driven rectifier, the outputs O1_DIN and O2_DIN are used to control primary low-side MOSFETs as well as the secondary-side rectifier MOSFETs.

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Start-Up Frequency Control Circuit

The start-up frequency control circuit addresses the need for bus converter to start at heavy load with a large output capacitance. In the steady state condition bus converters operate with the minimum off time and as the result, the output inductor current ripple is low. Therefore the output inductor value is able to be selected very low to save the size and cost. During over current or soft start condition the duty cycle is controlled by the cycle-by-cycle current limit circuit or by the voltage at soft-start capacitor. In this condition, the duty cycle D for the output inductor can be anywhere between 0 and 1 causing significant output inductor current ripple that reaches its maximum at duty cycle D = 0.5. The current limit circuit on primary side limits the peak current, not the average current. The limiting of peak current with a large ripple causes the fold back characteristic of converter output, which prevents the converter from ever reaching its nominal steady state output voltage.

The output inductor duty cycle is a ratio of output pulses T_{OUT}_D at pins O1_D and O2_D to the half of switching cycle $T_{SW(nom)}$, i.e. $T_{OUT}_D + T_{OFF}$ (see Figure 33):

$$D = \frac{T_{OUT}_D}{T_{OUT}_D + T_{OFF}} \tag{4}$$

The start-up frequency control circuit changes the switching frequency during the start up or during the cycle-by-cycle current limit to maintain the output inductor current ripple almost constant at any duty cycle D. This allows an additional cost and size saving because the output inductor can be selected based on steady state condition rather than the transient condition, which dictates significantly larger inductance value and size. Examples of switching frequency changes over duty cycle variation for the selected nominal frequencies 100 kHz and 450 kHz are shown in Figure 34. The plots are given for the nominal off time at 53 ns and 77 ns (right column) and for no load off time at 196 ns, 209 ns accordingly. It is shown that the impact of nominal off time on switching frequency is minimal. However the no load off time causes visible frequency reduction especially at maximum frequency when the duty cycle D is around 0.5.

Switching Frequency Plots vs Duty Cycle for $F_{SW(nom)}$ Set at 100 kHz and 450 kHz at Different No Load and Nominal T_{OFF} Time Sets.

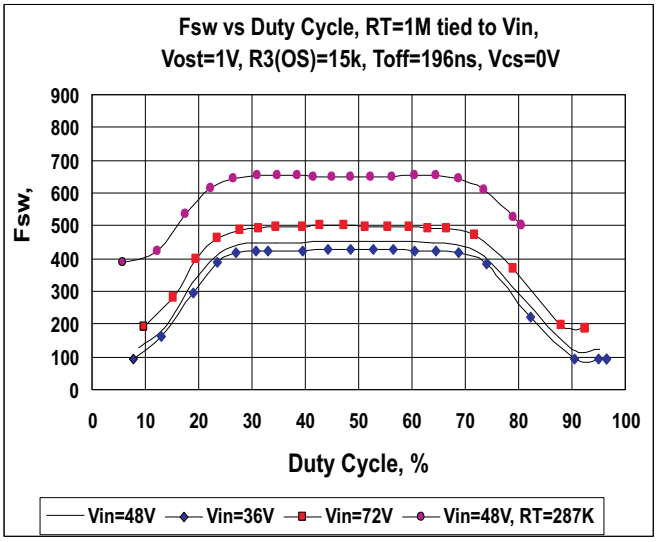


Figure 34.

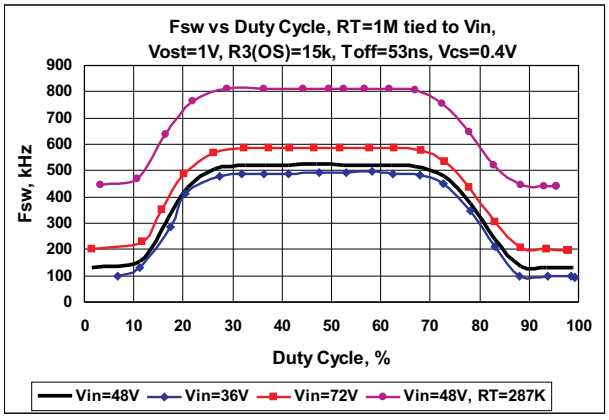


Figure 35.

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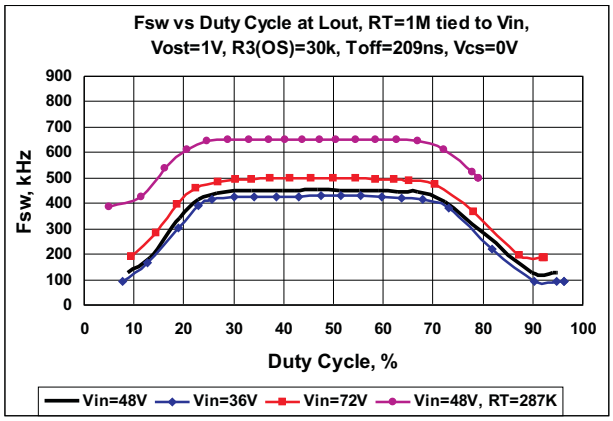


Figure 36.

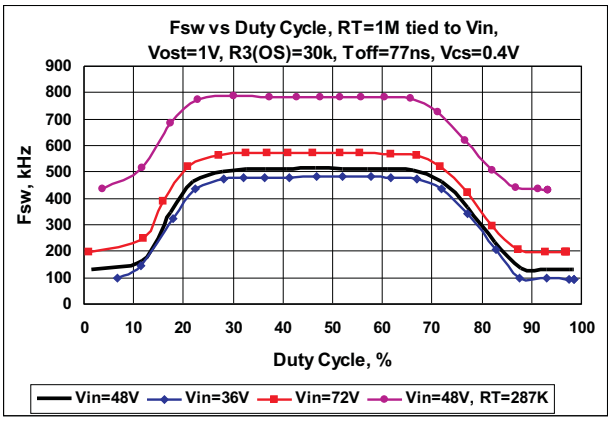


Figure 37.

To avoid jittering during the fast duty cycle change and reduce sensitivity to noise, the transfer function of switching frequency of the converter to the duty cycle has 20-kHz bandwidth well below the switching frequency. The maximum switching frequency $F_{SW(max)}$ of converter is given by:

$$F_{SW(max)} \cong F_{SW(nom)} + 375\,kHz \tag{5}$$

Where T_{OFF} affect is neglected as well and the frequency is in kHz. T_{OFF} has more affect on switching frequency F_{SW} at very high frequency. One can see how T_{OFF} affects FSW(max) in Figure 34.

The relation between switching frequency F_{SW} and duty cycle D in Figure 34 can be best described by:

$$F_{SW} \approx \begin{cases} F_{SW(nom)} & D < 0.1 \text{ or } D > 0.9 \\ F_{SW(max)} & 0.4 \le D \le 0.6 \\ F_{SW(max)} \times D \times (1-D) & 0.1 \le D < 0.4 \text{ or } 0.6 < D \le 0.9 \end{cases} \tag{6}$$

Knowing the maximum switching frequency $F_{SW(max)}$ at D = 0.5 and the ratio of peak output inductor current to the nominal load current KL = $I_{L(max)}/I_O$, allows calculate the output inductor value by using the following Equation 7.

$$L_O = \frac{V_{IN} \times D \times (1-D)}{N_{TR} \times 4 \times F_{SW(max)} \times (KL-1) \times I_O} \tag{7}$$

In this equation N_{TR} is transformer turns ratio from primary winding to the secondary. The selection of KL depends on the average output inductor current $I_{L(ch)}$ that needs to be provided during the start up to charge the output capacitor and supply the load. To ensure that the converter starts the following condition needs to be met.

$$I_{L(max)} \le 2 \times I_{L(ch)} \tag{8}$$

How $I_{L(ch)}$ needs to be defined is described in the following section.

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Soft Start

The soft-start pin SS is multi-function pin used for the following operations:

- Soft start with the duty cycle graduate increase from zero to its maximum value of almost 100%
- Setting cycle-by-cycle over current hiccup mode conditions
- On/off control for the converter
- Indicator of severe short circuit condition

The soft-start duration is defined by an external capacitor connected between SS pin and ground and the internal charge current that has typical value of 25 μA. During soft start, the duty cycle of controller is determined by the voltage at SS pin. Below the 0.85-V threshold, there are no switching pulses at the outputs. Pulling the soft-start pin externally below or above 0.55-V typical threshold can be used for the on/off control. When the soft-start voltage is rising from 0.85 V up to 2.85 V and there is no current limit condition, the duty cycle applied to the output inductor is increasing accordingly from 0 to 1. The external capacitor C_{SS} value can be defined by the Equation 9:

$$C_{SS} = \frac{T_{SS} \times 25\,\mu A}{(2.85V - 0.85V)} \tag{9}$$

For example, if the soft-start time T_{SS} is selected 10 ms, then the soft-start capacitor C_{SS} is equal to 125 nF and the closest available standard value100 nF can be selected. Notice, that the output pulses do not appear until the voltage at soft start capacitor reaches 0.85 V. An additional typical soft start delay caused by this can be calculated by the Equation 10:

$$T_{DEL} = \frac{C_{SS} \times 0.85V}{25\,\mu A} \tag{10}$$

For the C_{SS} = 100 nF the calculated delay is 3.4 ms.

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The Equation 9 and Equation 10 use typical values for calculations. If the output capacitor of the bus converter is large and the soft-start time is selected relatively short, then the converter should deliver large charge current to the output capacitor to provide the required soft start time. This current might hit the current limit threshold and the soft-start time can be longer than expected. Figure 38 provides an estimation of the required average charge current from the converter to charge the output capacitor within predetermined soft-start time. To avoid tripping of the current limit comparator, the current limit threshold should be set above the required average charge current with the additional current required by the load, half of the output inductor current ripple and the magnetizing current of the transformer. The average output inductor charge current I_{OUT} during the cycle-by-cycle current limit can be described by the following equation:

$$I_{OUT} = I_{O(lim)} - \frac{N_{TR} \times V_{IN} \times D}{4 \times L_m \times F_{SW}} - \frac{V_{IN} \times D \times (1-D)}{4 \times N_{TR} \times L_O \times F_{SW}} \quad (11)$$

Here $I_{O(lim)}$ is the output current limit and L_m is magnetizing inductance. The $I_{O(lim)}$ is always less or equal to $I_{L(max)}$ to avoid saturation of the output inductor. The output voltage V_O over output current I_{OUT} is as follows

$$V_O = \frac{(V_{IN} - I_{OUT} \times R_{PR} / N_{TR}) \times D}{N_{TR}} - I_{OUT} \times R_{SEC} \quad (12)$$

Where R_{PR} is the equivalent resistance on primary side and R_{SEC} is the equivalent resistance on secondary side.

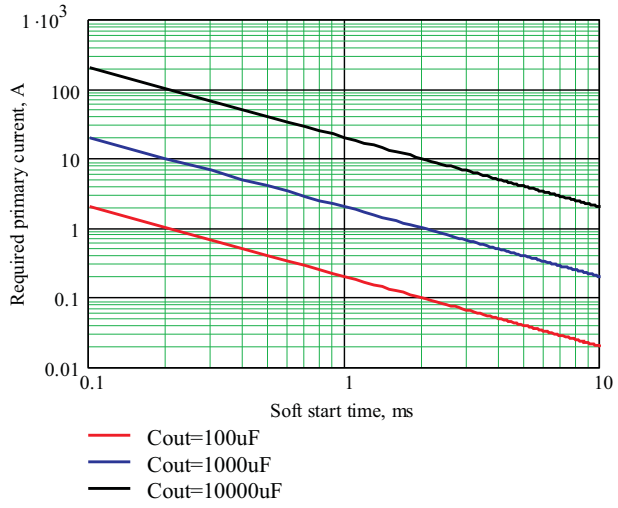


Figure 38. Estimated Average Primary-Side Charge Current From the Converter Required to Charge the Output Capacitor of Specified Value Within Required Soft-Start Time

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Figure 39 shows the output voltage as function of the average load current limited by the cycle-by-cycle current limit threshold after substituting (9) into (10). These plots are generated for the following conditions: V_{IN} = 48 V, N_{TR} = 5, L_O= 0.1 µH, L_m = 75 µH, $I_{O(lim)}$ = 73 A, R_{pr} = 25 mΩ and R_{SEC} = 4 mΩ at F_{SW}= 100 kHz, 200 kHz and 400 kHz. This fold back type of behavior limits the start-up capability of unregulated IBC. One can see that at 100-kHz switching frequency and 0.5 duty cycle (i.e., $V_O \approx 5$ V), only about 11.5 A average current is available to charge the output capacitor while at 400 kHz, the charge current can be as high as 60 A. The plots in Figure 39 show the required average charge current reflected to the primary side of the converter with N_{TR} = 5:1 for different output capacitor values depending on the selected soft-start time, which do not count extra current drawn by the load itself. Therefore the significant output inductor current ripple not only can trip the peak current mode control current limit circuit to reduce the average output inductor current available to charge the output capacitor, but also can cause the hiccup or latch off of the converter to prevent it from starting at all. Increasing the current limit threshold to allow the normal start up of the converter can cause potential overstress if for some reason the load exceeds its nominal current during the steady state operation.

Without frequency control circuit, the module operates only at 100 kHz. At 100 kHz the secondary charge current available is only 11.5 A, which is only 2.3 A if reflected to the primary side (N_{TR} = 5). The 2.3-A current is able to charge the 10000-µF output capacitor within 10 ms provided that there is no additional load current applied.

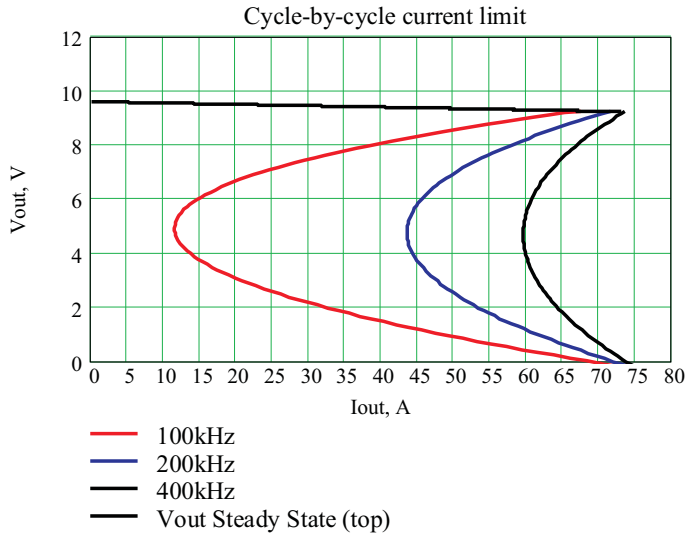


Figure 39. Output Voltage at Cycle-by-Cycle Current Limit

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With the frequency control circuit, the start up switching frequency is 400 kHz. At 400-kHz, 60-A charge current is available, which is 12 A if reflected to the primary side. Assuming as in previous case 2.3 A portion of this current is used to charge the 10000-µF output capacitor within 10 ms, the remaining 9.7 A on primary side allows extra 48.5-A current to supply the load itself on the secondary side. Figure 40 shows a design example using the startup frequency control of UCC28230 to start up with 30-A constant load current and 10900-µF output capacitor.

Using SS pin and soft-start capacitor to set cycle-by-cycle over-current hiccup mode is described further in Cycle-by-Cycle Current Limit section and Short Circuit Protection section.

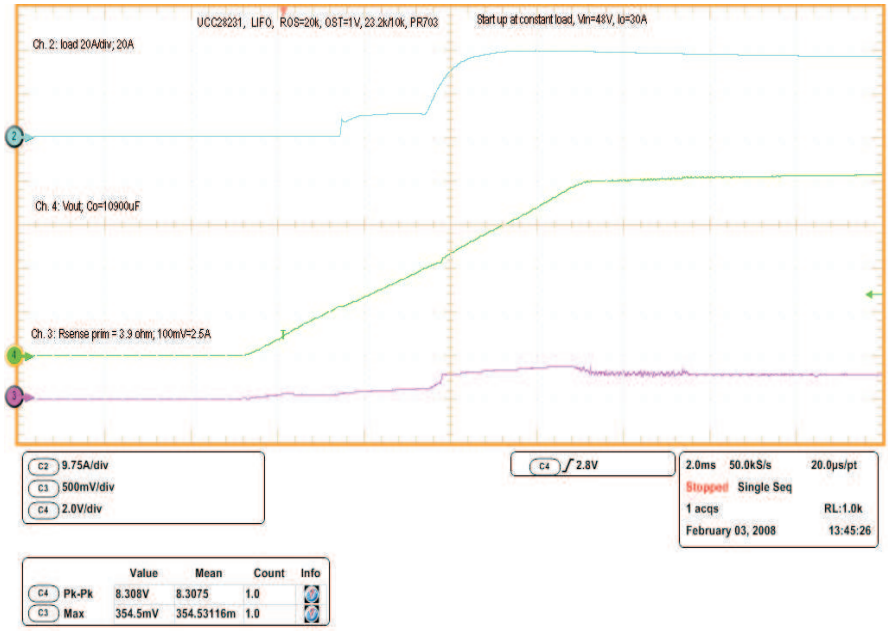


Figure 40. Start up at 30-A Constant Current Load With C_O = 10900 µF

Current Sensing

The current sensing pin CS is used for the following functional blocks:

- Cycle-by-cycle current limit
- Adjustable off-time control
- Short circuit protection

Cycle-by-Cycle Current Limit and Short Circuit Protection

The cycle-by-cycle current limit provides peak current limit on primary side when the load current exceeds its predetermined threshold. For peak current mode control, certain leading edge blanking time is needed to prevent the controller from false tripping due to switching noise. In order to save external RC filter for the blanking time, an internal 50-ns filter at CS input is provided. With the 50-ns delay from the input of the current sense comparator to the outputs, the total propagation delay T_{CS} from CS pin to outputs is about 100 ns. An external RC filter is still needed if the power stage requires more blanking time. The 0.5-V ±3% cycle-by-cycle current limit threshold is optimized for efficient current transformer based sensing. The duration when a converter operates at cycle-by-cycle current limit depends on the value of soft-start capacitor and how severe is the over current condition. The soft-start capacitor value also determines the so called hiccup mode off-time duration. These are achieved by the internal discharge current I_{DS} (Equation 13) and I_{HCC} (see Figure 41) at SS pin.

$$I_{DS} = \left(-25 \times \left(1 - D\right) + 5\right)\mu A \tag{13}$$

When the output inductor duty cycle D at cycle-by-cycle current limit is above 80%, the converter operates as the current source and does not enter into hiccup mode at all. This allows parallel operation of converters using droop current sharing technique. At more severe over current condition, the duty cycle D becomes lower and Ids becomes large enough to initiate hiccup mode with periodical restart. The behaviour of the converter at different modes and related soft-start capacitor charge/discharge currents are shown in Figure 41.

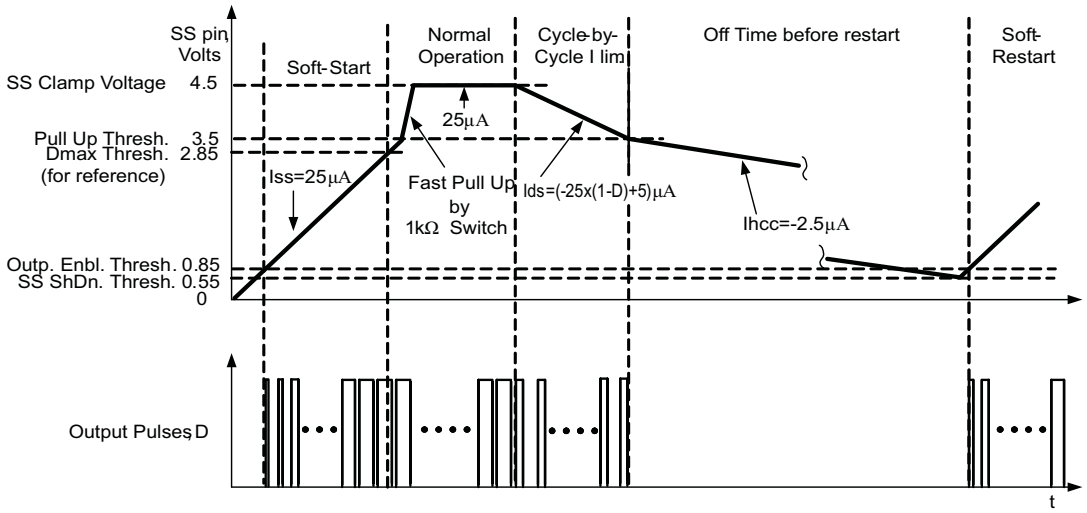


Figure 41. Timing Diagram of Soft-Start Voltage V_{SS} at Different Modes of Operation Defined by Voltage Thresholds and Related Soft-Start Capacitor Charge/Discharge Currents

The largest discharge current is at the duty cycle close to zero as 20 µA. This current sets the shortest operation time during the cycle-by-cycle current limit which is defined as:

$$T_{CL(on)} = \frac{C_{SS} \times \left(4.5V - 3.5V\right)}{20\,\mu A} \tag{14}$$

Thus, if the soft-start capacitor CSS = 100 nF is selected, then the $T_{CL(on)}$ time will be 5 ms.

To calculate the hiccup off time $T_{CL(off)}$ before the restart, Equation 15 needs to be used:

$$T_{CL(off)} = \frac{C_{SS} \times \left(3.5V - 0.55V\right)}{2.5\,\mu A} \tag{15}$$

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With the same soft-start capacitor value 100 nF, the off time before the restart is going to be 118 ms. Notice, that if the over current condition happens before the soft-start capacitor voltage reaches the 3.5-V threshold during start up, the controller limits the current but the soft-start capacitor continues to be charged. As soon as the 3.5-V threshold is reached, the soft-start voltage is quickly pulled up to the 4.5-V threshold by an internal 1-kΩ $R_{DS(on)}$ switch and the cycle-by-cycle current limit duration timing starts by discharging the soft-start capacitor. Depending on specific design requirements, the user can override default parameters by applying external charge or discharge currents to the soft-start capacitor. Figure 42 shows the operation of a full-bridge system at cycle-by-cycle current limit. The waveforms include drain-source voltages of synchronous rectifiers and voltage at CS pin. The whole cycle-by-cycle current limit and hiccup operation is shown in Figure 43. In this example the cycle-by-cycle current limit lasts about 25 ms followed by 150 ms of off time.



Figure 42. Cycle-by-Cycle Current Limit

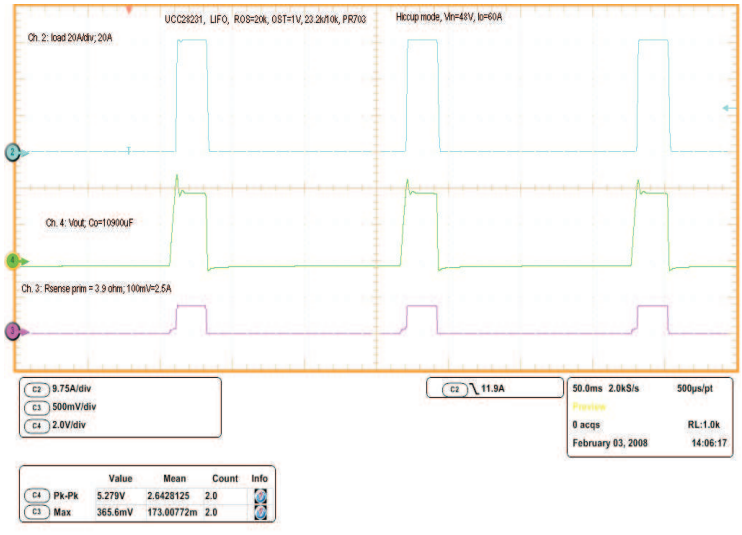


Figure 43. Hiccup Mode with Cycle-by-Cycle Current Limit at I_{OUT} = 60 A

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In the event of a severe short circuit condition, the current sense voltage will exceed the short circuit threshold set at 0.7 V min. At this point the controller shuts down the converter with propagation time 100 ns and pulls the soft start pin up to the 4.5-V threshold. (see Figure 44).

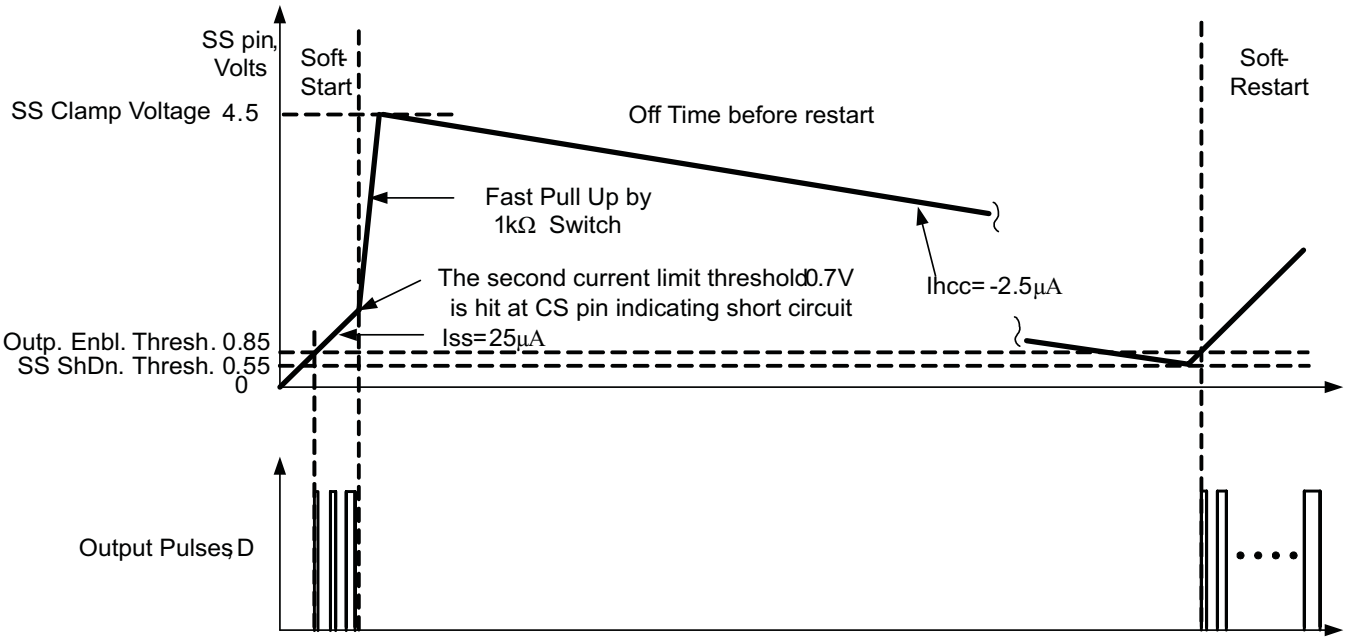


Figure 44. Timing Diagram for the Soft-Start Capacitor Voltage V_{SS} During Short Circuit Protection

At this condition the soft-start voltage is forcibly pulled up even if the soft-start charge is not completed. After that, the soft-start capacitor is discharged by 2.5-μA current until its voltage reaches the 0.55 V in order to resume the soft-start cycle again. The duration of off time before the restart is defined by Equation 16:

$$T_{CL(off)} = \frac{C_{SS} \times (4.5V - 0.55V)}{2.5\,\mu A} \tag{16}$$

With the same soft-start capacitor value 100 nF, the off time before the restart is going to be about 158 ms. Similar to the over current condition, the hiccup mode with the restart can be override by user if a pull-up resistor is connected between the SS and VREF pins. If the pull-up current provided by the resistor exceeds 2.5 μA, then the controller remains in the latch-off mode. In this case, an external soft-start capacitor value should be calculated with the additional pull-up current taken into account. The latch-off mode can be reset externally if the soft-start capacitor forcibly discharged below 0.55 V or the V_{DD} voltage is lowered below the UVLO threshold.

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Off-Time Control Circuit

The off time control circuit provides optimal off time between O1_D and O2_D outputs depending on the load current condition. The UCC28230/1 implements the off time control approach based on step function with hysteresis (see Figure 45).

Off-time control is an important feature to address an optimal operation of self-driven synchronous rectifier over the whole load current range. In self-driven rectifier applications, the turn-on and off time of the synchronous FETs is defined by the current of output inductor and its polarity. Some additional energy is also provided from the magnetizing inductance of a power transformer but it may not be sufficient for the fast switching. Therefore, at light load the off-time should be longer than at full load to allow previously conducting rectifier MOSFET to be completely turned off before the next switching half-cycle. This ensures the rectifier MOSFET having enough time to turn off before the primary-side MOSFET forces it to turn off. The turn off of the rectifier MOSFET, while still conducting, results in a current surge followed by a significant voltage spike which lowers the efficiency and reliability of converter.

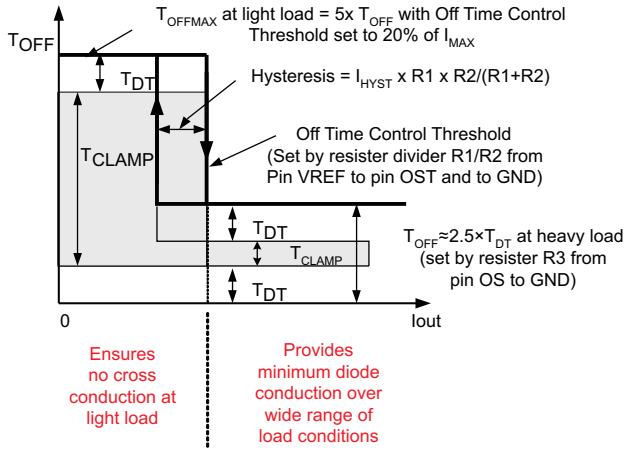


Figure 45. The Off Time Change as Function of Load Current

Usually there is no direct access to the load current of bus converters, so the primary current sensing is used to replicate load current changes (see Figure 45). The largest part of the primary current is the load current on secondary side of power transformer reflected into the primary side in accordance to transformer's turn ratio. The primary current includes not only the reflected load current, but also magnetizing current. However, for the most practical applications the accuracy of solution with magnetizing current included is sufficient because in this application the magnetizing current is only small percentage of overall current. With this assumption, the voltage at pin CS can be defined as:

$$V_{CS} = I_{OUT} \times \frac{R_{CS} \times W_{CT(pr)} \times W_{PT(sec)}}{W_{PT(pr)} \times W_{CT(sec)}} \quad (17)$$

Where I_{OUT} is the output inductor current, R_{CS} is the current sense resistor, $W_{PT(pr)}$ and $W_{PT(sec)}$ are the primary and secondary number of turns of power transformer windings and the $W_{CT(pr)}$ and $W_{CT(sec)}$ are the primary and secondary number of turns of current transformer windings.

UCC28230/1 uses OS pin and OST pin to program the nominal off time T_{OFF} and the output current threshold where the off time steps up to the new value $T_{OFF(max)}$. The dead time T_d and nominal off time T_{OFF} are set by resistor R3 between OS pin and GND (Figure 3, Figure 4 and Figure 50). Figure 46 shows how to choose R3 resistance to achieve the dead time Td and nominal off time T_{OFF} for both UCC28230 and UCC28231. For example, if a 40ns nominal T_{OFF} is needed, the resistor value should be 8.45kΩ, and Td is about 17ns for UCC28230 and 15ns for UCC28231. 15 kΩ R3 at OS pin sets T_{OFF} to 50 ns and T_d to 23 ns for UCC28230, with T_{OFF} as 47 ns and T_d as 19 ns for UCC28231. Based on Figure 46, one can tell that T_{OFF} is about 2.2 to 2.64 times of T_d for UCC28230, and 2.25 to 2.75 times of T_d for UCC28231.

Figure 25 through Figure 30 from Typical Waveforms show the output switching waveforms including rise and fall time and off time T_{OFF1}, T_{OFF2} for each half switching cycle and dead time T_{d1}, T_{d2}, T_{d3} and T_{d4} for each half switching cycle.

Off time and dead time selection based on the resistor R3 value.

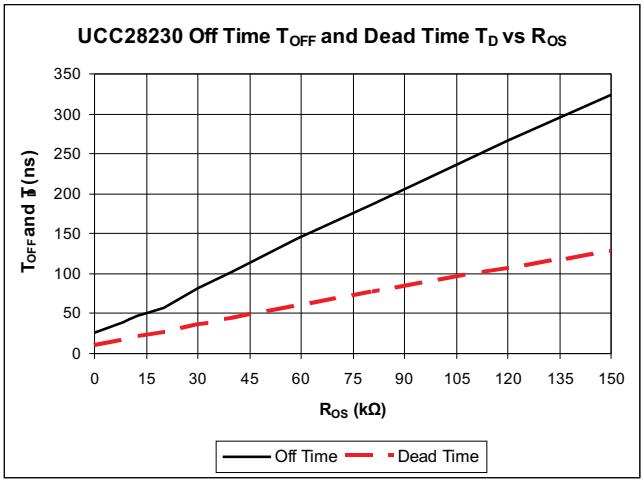


Figure 46.

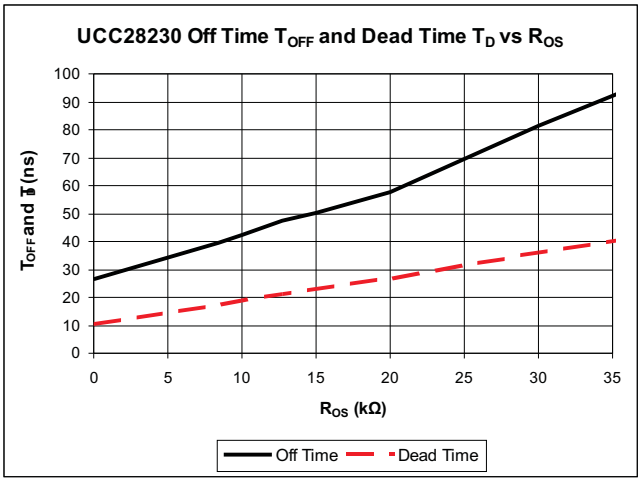


Figure 47.

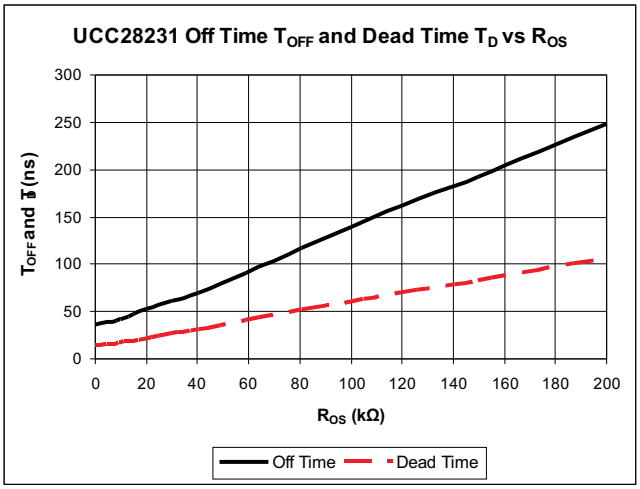


Figure 48.

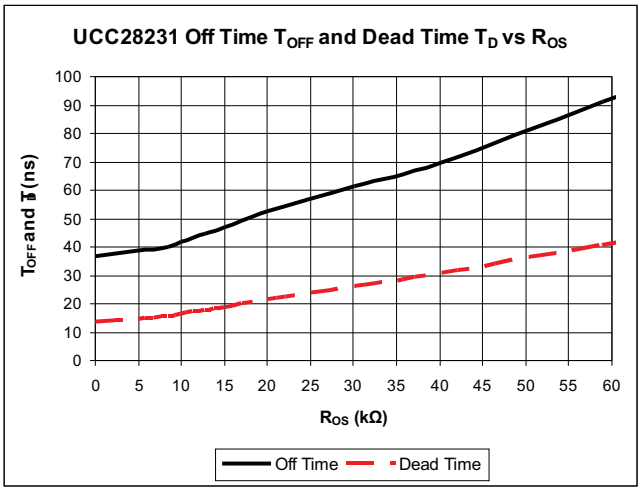


Figure 49.

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The next step is to set the output current threshold below that the off time changes to its maximum value. This threshold is defined as:

$$VOST = VREF \times \frac{R2}{R1 + R2} \tag{18}$$

The increase of off time at light load condition is provided by the increasing of overlapping time T_{CLAMP} of O1_DIN and O2_DIN outputs (see Figure 33). This ensures the faster turning off of the rectifier MOSFETs when the primary winding is clamped. The dead time between the switching of primary MOSFETs in each leg remains the same over the load current, which is still proportional to nominal off time as shown in Figure 46.

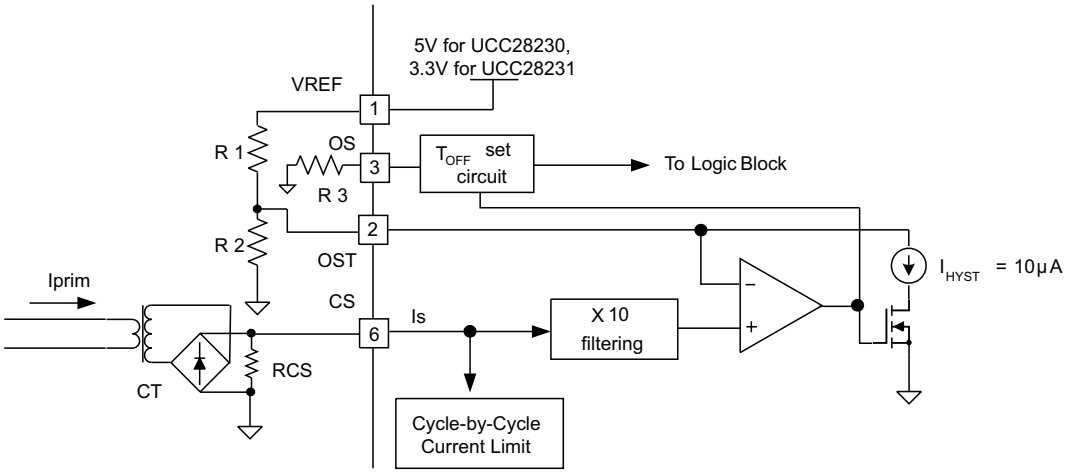


Figure 50. The Off-Time Control Circuit Using Comparator With Hysteresis

Selecting optimal hysteresis is important to avoid oscillation. UCC28230/31 provides the flexibility of programming the hysteresis with internal 10-µA current I_{HYST} and the values of external resistors R1 and R2 (see Figure 50). Equation 19 shows how to choose the hysteresis.

$$V_{hyst} = I_{hyst} \times \frac{R1 \times R2}{R1 + R2} \tag{19}$$

In some cases, the disabling of off-time control circuit is needed, which can be done by simply connecting OST pin to GND or to VREF. Connecting OST pin to the VREF is characterized in the electrical table and is the preferable way to maintain fixed off time set by resistor R3.

The load dependent dead time will cause a slight change in output duty cycle at the programmed transition point from light load to heavy load and vice-versa. This slight change in duty cycle corresponds to a slight change in output voltage.

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APPLICATION INFORMATION

DESIGN EXAMPLE

Two design examples are provided to show how to design an intermediate bus converter with UCC28230/1. Design Example 1 provides a concise step-by-step design. Its design specifications, schematics and test results are illustrated on efficiency, power dissipation and output voltage regulation. Design Example 2 is to show an industry standard quarter brick module design with 12-layer boards and embedded magnetic parts. Its design specifications, schematics, and test results are provided.

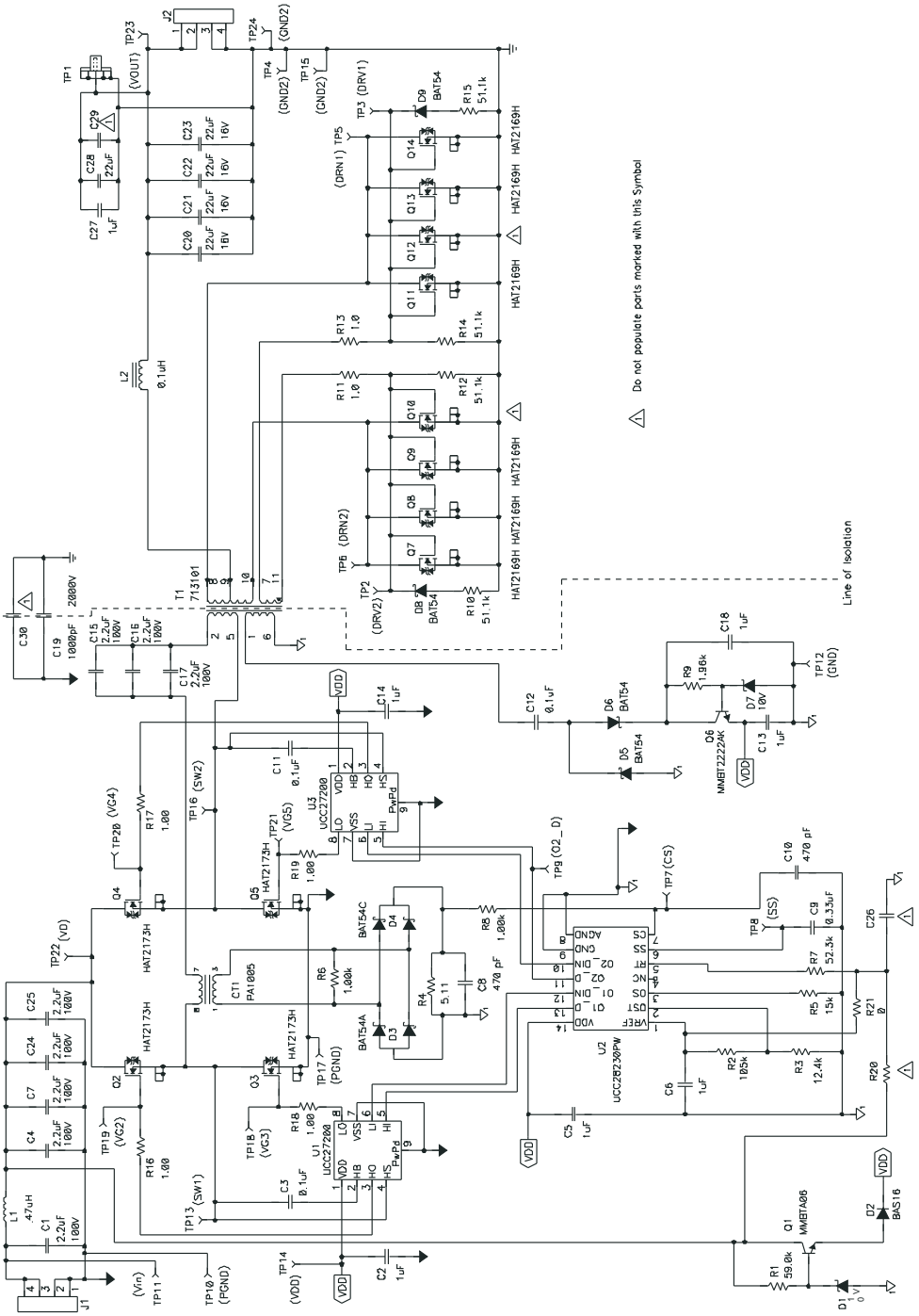


Figure 51. Design Example of IBC Using UCC28230 Controller Device

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Design Goals

This example illustrates the design process and component selection for an intermediate bus converter using UCC28230. The target design is a 300-W full bridge converter with narrowed input voltage range in a close to quarter brick form factor with open-loop control for the telecom applications in intermediate bus architecture. Its specifications are shown in Table 1.

Table 1. 300W IBC Specifications

PARAMETER		MIN	TYP	MAX	UNIT
Input voltage	V_{IN}	43	48	53	V_{DC}
Output voltage	V_{OUT}		9.6		
Output power	P_{OUT}			300	W
Output load current	I_{OUT}			30	A
Load capacitance	C_{OUT}			10,000	µF
Switching frequency	F_{SW}		125		kHz
Over power limit	P_{LIMIT}			150%	
Efficiency at full load	η (V_{IN} = 48 V)		96%		
Isolation		1500			V
Turns-ratio	N_{PRI} : N_{SEC}		5:1		

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Recommended PCB Device Layout

The device programming components should be placed as close as possible to the device. The power ground should be separated from the signal ground and connected only at one point at device pin 8 and 9 for TSSOP package. For SON package there is only one ground pin available, pin 7. In this case, pin 7 is used to replace the connection of pin 8 and pin 9 of TSSOP. The following takes TSSOP as the example. For SON, a similar arrangement on the layout should be made. Capacitors for bias decoupling (C5), reference voltage decoupling (C6), and soft start (C9), should be placed right across the signal ground and pins 14, 1 and 6, respectively. All programming resistors, R2, R3, R5, and R7 should be placed next to the device pins they should be connected to minimize their EMI noise reception. See Figure 52 for a recommended component layout and placement. PCB design considerations of other circuit part are discussed later in the relevant part design.

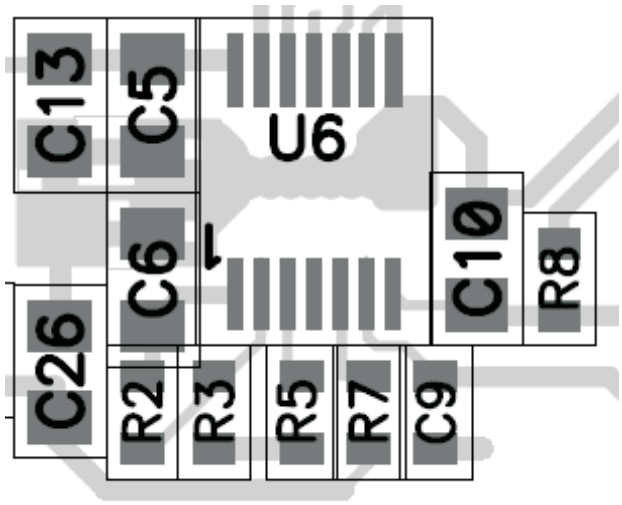


Figure 52.

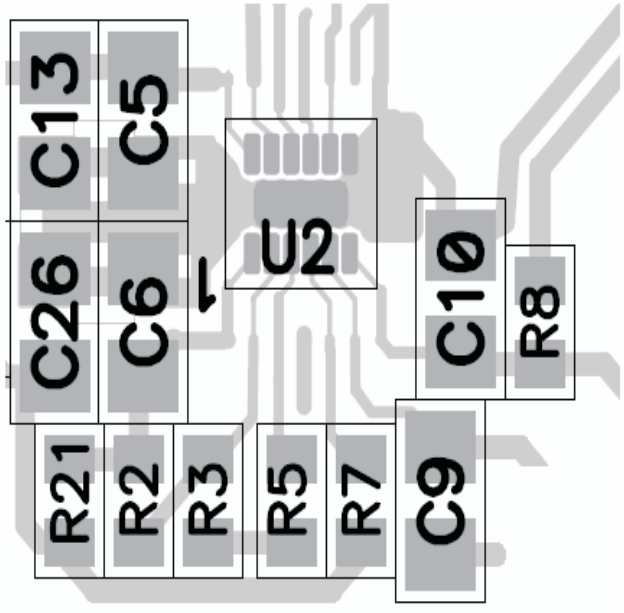


Figure 53.

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Programming the UCC28230

Switching frequency: R7 Equation 3

$$R7 = RT = K1 \times \frac{(VREF - K2)}{f_{SW}} = 2500 \times \frac{(5 - 2.4)}{125} = 52\,k\Omega \Rightarrow 52.3\,k\Omega \tag{20}$$

Soft-start time: C9

Considering power on with maximum 10,000-µF load capacitors, soft-start time may need be adjusted and if soft-start time is determined as 25 ms, then based on Equation 9

$$C_9 = C_{SS} = \frac{T_{SS} \times K3}{(K4 - K5)} = \frac{25 \times 25\,\mu A}{(2.85V - 0.85V)} = 0.27\,\mu F \Rightarrow 0.33\,\mu F \tag{21}$$

Multilayer ceramic capacitor (X7R or X5R) should be used.

Dead time set-up resistor, R5

Assuming T_d = 20 ns, based on Figure 46

$$R5 = 13\,k\Omega \Rightarrow 15\,k\Omega \tag{22}$$

Off-time adjustment threshold and hysteresis resistors: R2 and R3

T_{OFF} is set up at 10% of rated load, V_{OST} = 0.5V, with hysteresis V_{HYST} = 100 mV. Based on Equation 18 and Equation 19, kΩ

$$\frac{R3}{R2} = \frac{V_{OST}}{(VREF - V_{OST})} \tag{23}$$

$$R3 = \frac{V_{hyst}}{I_{hyst}} \times \left(1 + \frac{V_{OST}}{VREF - V_{OST}}\right) \tag{24}$$

Solution to the above two equations yields R2 = 99.9 kΩ, and R3 = 11.1 kΩ.

V_{DD} decoupling capacitor: C5 High quality low ESR and low ESL such as multilayer ceramic capacitor (X7R or X5R) with a value between 0.1 to 1.0 µF should be used.

VREF decoupling and stability capacitor: C6

High quality low ESR and low ESL such as multilayer ceramic capacitor (X7R or X5R) with a value between 1.0 to 2.2 µF should be used .

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Current Sensing

Power stage design shows primary DC current maximum value is determined

$$I_{P(rms)} = \frac{P_{LIMIT}}{V_{IN(min)}} = \frac{450}{43} = 10.5\ (with\ 20\%\ marg\ in) \Rightarrow 12.6\ A \tag{25}$$

If pick up a current transformer with turns ratio of 100:1, R4 is determined as 5.11Ω with current sense threshold at 150% of rated power.

Current sensing plays a critical role to achieve several features of UCC28230 including over current protection and off time adjustment. Usually the sensing element cannot be placed next to the device. In such a case, it is strongly recommended to route the PCB with Kelvin connection from the current sensing output device (R4) to the IC (Pin 7) as shown in Figure 54. A small RC filter (R8 and C10) is required to attenuate possible high frequency noise. A small capacitor, C8, can also be added to get further filtering effect while usually it is not needed.

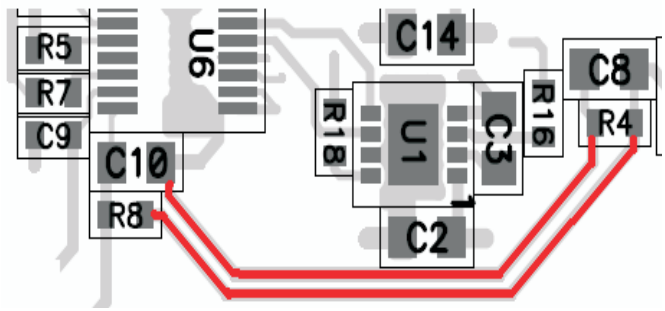


Figure 54.

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Power Stage

Transformer:

The design goal shows a 300-W transformer with turns ratio 5:1. To make the design close to the telecom typical applications, planar magnetic core is used with windings using PCB traces.

Primary MOSFETs

In steady state, the primary MOSFET's duty cycle is about 50%. At minimum input voltage 43 V, maximum 450-W power, and 96% efficiency, their current rating can be determined as

$$I_{D(rms)} = \frac{P_{LIMIT}}{V_{IN(min)}} \times \frac{\sqrt{\alpha}}{\eta} = \frac{450}{43} \times \frac{\sqrt{0.5}}{0.96} = 7.7\,A \tag{26}$$

α = duty cycle of MOSFETS

Their voltage rating is determined as 53 V. After considering 20% margin, current and voltage rating should be 9 A and 80 V, respectively.

Primary MOSFET drivers

The UCC28230 of 0.2-A MOSFET driving capability requires external MOSFET drivers. One good option is to use UCC27200 for U1 and U3. Gate resistors (1.0 Ω) of R16-19 are suggested to add in and attenuate possible parasitic ringing. UCC27200 is designed for half bridge application with 2-A driving capability. Each UCC27200 should have its own VDD high quality decoupling and driving energy capacitor (typical value 1.0 μF) of low ESR and low ESL. Its boost strap capacitor value of 0.1μF can be selected.

Secondary MOSFETs

In steady state, the secondary MOSFETs have their duty about 50%. At minimum input voltage 43 V, maximum 450-W power, transformer turns ratio 5:1, their current rating can be determined as:

$$I_{D(rms)} = \frac{P_{LIMIT}}{V_{IN(min)}} \times \sqrt{\alpha} \times N_t = \frac{450}{43} \times \sqrt{0.5} \times 5 = 52.3\,A \tag{27}$$

Their voltage rating can be determined as:

$$V_{DS} = \frac{V_{IN(max)}}{N_t} \times 2 = \frac{53}{5} \times 2 = 21.2V \tag{28}$$

After considering potential parasitic ringing, 40-V MOSFETs may be used.

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Output Inductor

The output inductor value is determined by the start-up condition with supposed maximum peak-to-peak ripple current. The ripple current is a function of input voltage, duty cycle, switching frequency and transformer turns ratio. At start, a highest ripple should occur at about 0.5 duty cycle and maximum input voltage when the switching frequency should be designed in accordance with the top flat area shown in Figure 34. A typical ripple current can be initially taken around 90% of the maximum output current from steady state operation.

$$L_2 = \frac{D \times (1-D) \times V_{IN}}{2 \times n \times f_{sw} \times I_{pk-pk}} = \frac{0.5 \times (1-0.5) \times 53}{2 \times 5 \times 500 \times 10^3 \times 25} = 106\ nH \tag{29}$$

The inductor value is then determined to be 100 nH.

Test Results

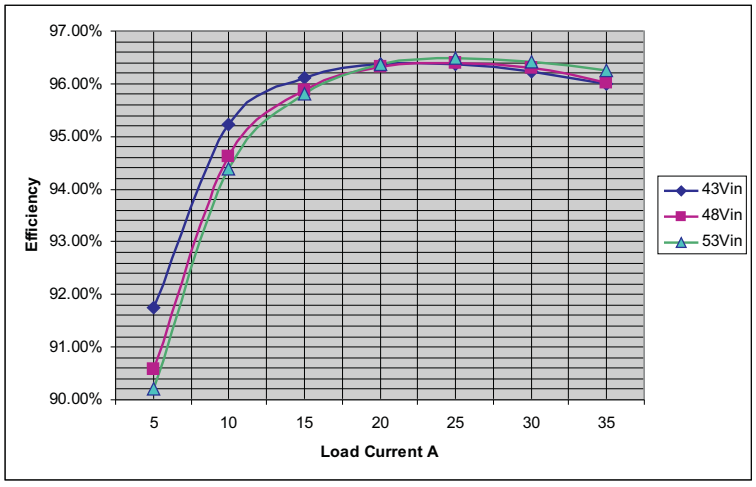


Figure 55. Efficiency

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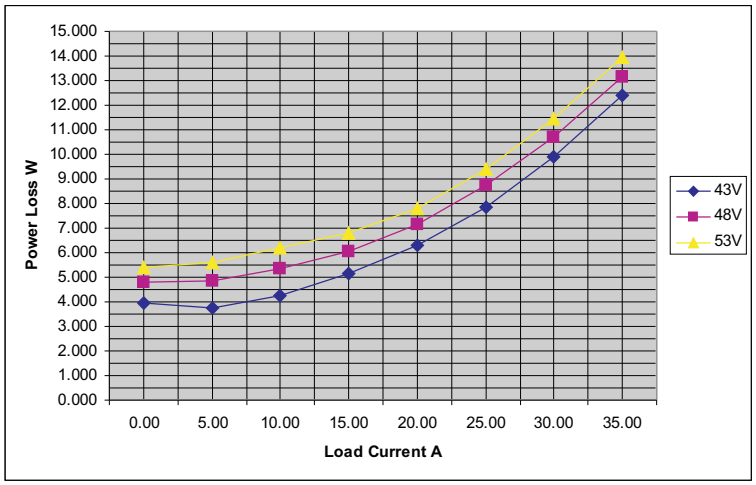


Figure 56. . Power Dissipation

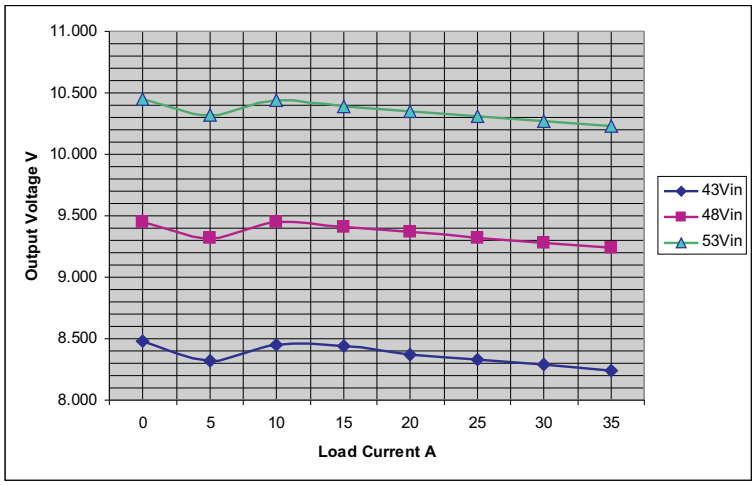


Figure 57. Load regulation

Design Example 2

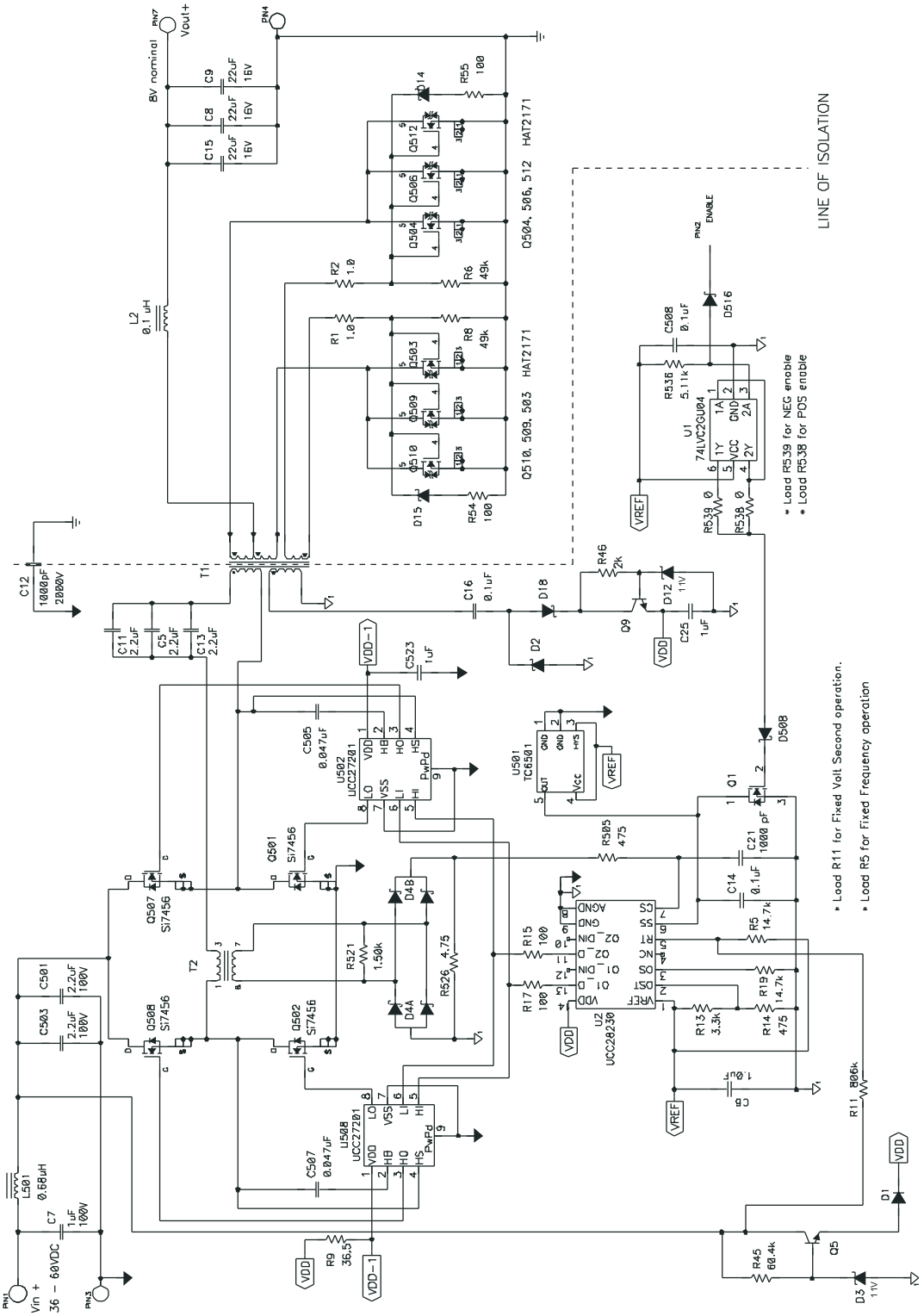


Figure 58.

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This design consists of a 350 watt 6:1 bus converter in an industry standard quarter brick package, utilizing the UCC28230 PWM Bus Controller, UCC27201 High Voltage High-Side Low-Side Drivers and a 12-layer PCB with embedded magnetic parts. This design features low profile construction representative of typical isolated dc-to-dc construction in a quarter brick form factor. Typical efficiency above 97% is achieved with this design. By using the UCC28230 PWM Bus Controller allows optimum duty cycle control for both light load and full load. The unique feature of sampling the primary transformer current and controlling the dead time provides reduced no load/ light load power dissipation by increasing the dead time to minimize output synchronous rectifier cross conduction, yet reducing the dead time at higher output loads to achieve maximum power transfer to the load. As with all self driven synchronous rectifiers, transformer design is critical. Minimal leakage inductance to reduce ringing on the MOSFETs and minimize or eliminate snubbers along with optimum coupling of the output secondary winding with the gate drive winding for precise timing of the turn on and off of the synchronous rectifiers. This is required to reduce the amount of conduction of the internal intrinsic diode of the MOSFETs.

350-W IBC Specifications

PARAMETER		MIN	TYP	MAX	UNIT
Input voltage	V_{IN}	36	48	60	V_{DC}
Output voltage	V_{OUT}		8.0		
Output power	P_{OUT}			350	W
Output load current	I_{OUT}			45	A
Load capacitance	C_{OUT}			10,000	µF
Switching frequency	F_{SW}		165		kHz
Over power limit	P_{LIMIT}			150%	
Efficiency at full load	η (V_{IN} = 48V)		96%		
Isolation		1500			V
Turns-ratio	N_{PRI} : N_{SEC}		6:1		

Test Results

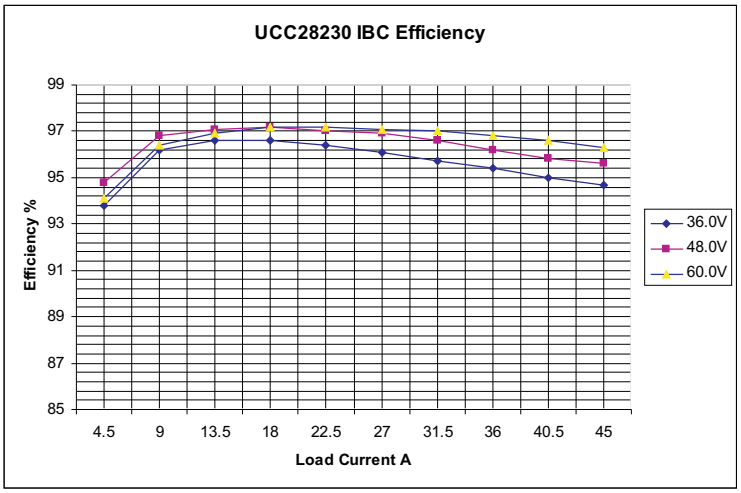


Figure 59. Efficiency

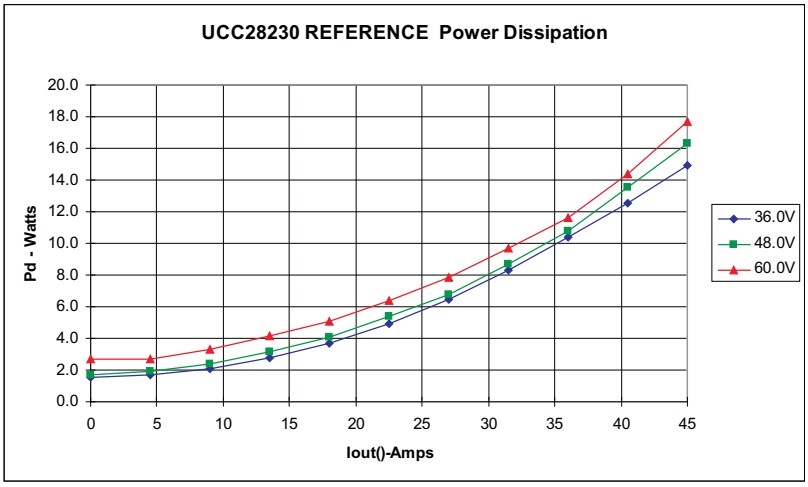


Figure 60. Power Dissipation

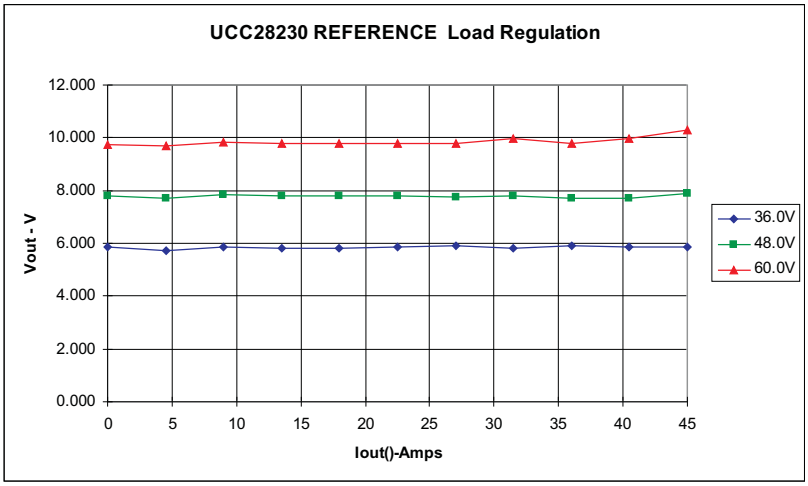


Figure 61. Load Regulation

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28230DRNR	ACTIVE	USON	DRN	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	230	Samples
UCC28230DRNT	ACTIVE	USON	DRN	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	230	Samples
UCC28230PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	28230	Samples
UCC28230PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	28230	Samples
UCC28231DRNR	ACTIVE	USON	DRN	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	231	Samples
UCC28231DRNT	ACTIVE	USON	DRN	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	231	Samples
UCC28231PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	28231	Samples
UCC28231PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	28231	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

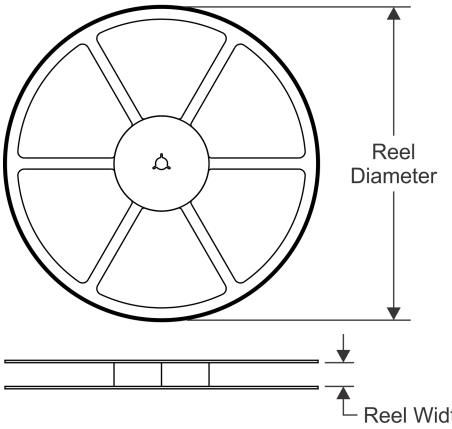
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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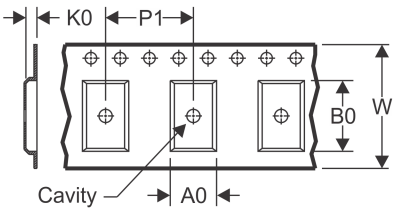
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

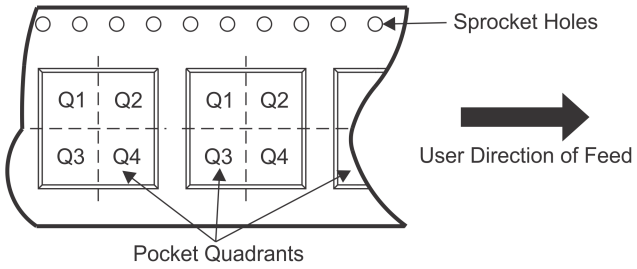


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

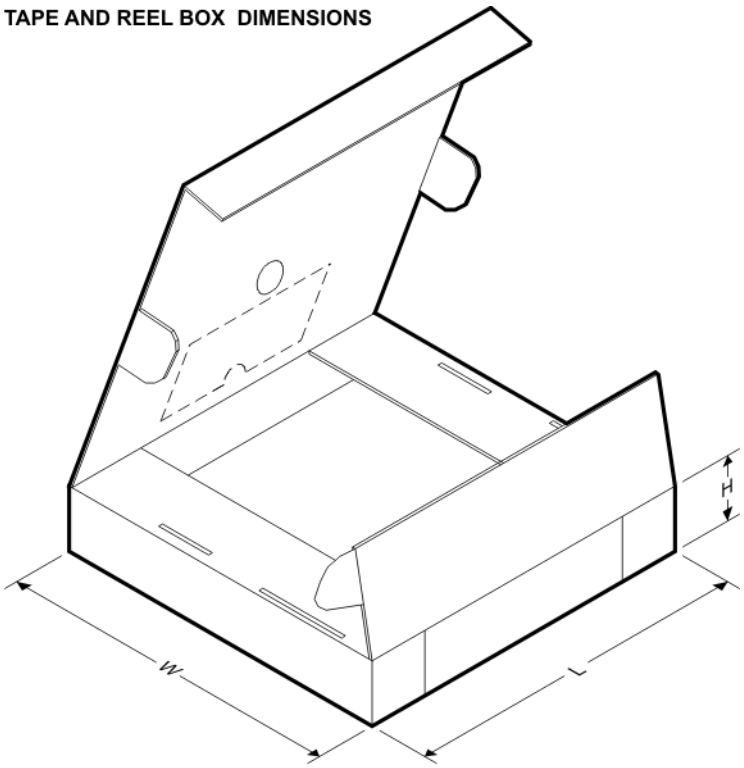
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28230DRNR	USON	DRN	12	3000	180.0	12.4	2.3	3.3	0.85	4.0	12.0	Q1
UCC28230DRNT	USON	DRN	12	250	180.0	12.4	2.3	3.3	0.85	4.0	12.0	Q1
UCC28231DRNR	USON	DRN	12	3000	330.0	12.4	2.3	3.3	0.85	4.0	12.0	Q1
UCC28231DRNT	USON	DRN	12	250	180.0	12.4	2.3	3.3	0.85	4.0	12.0	Q1

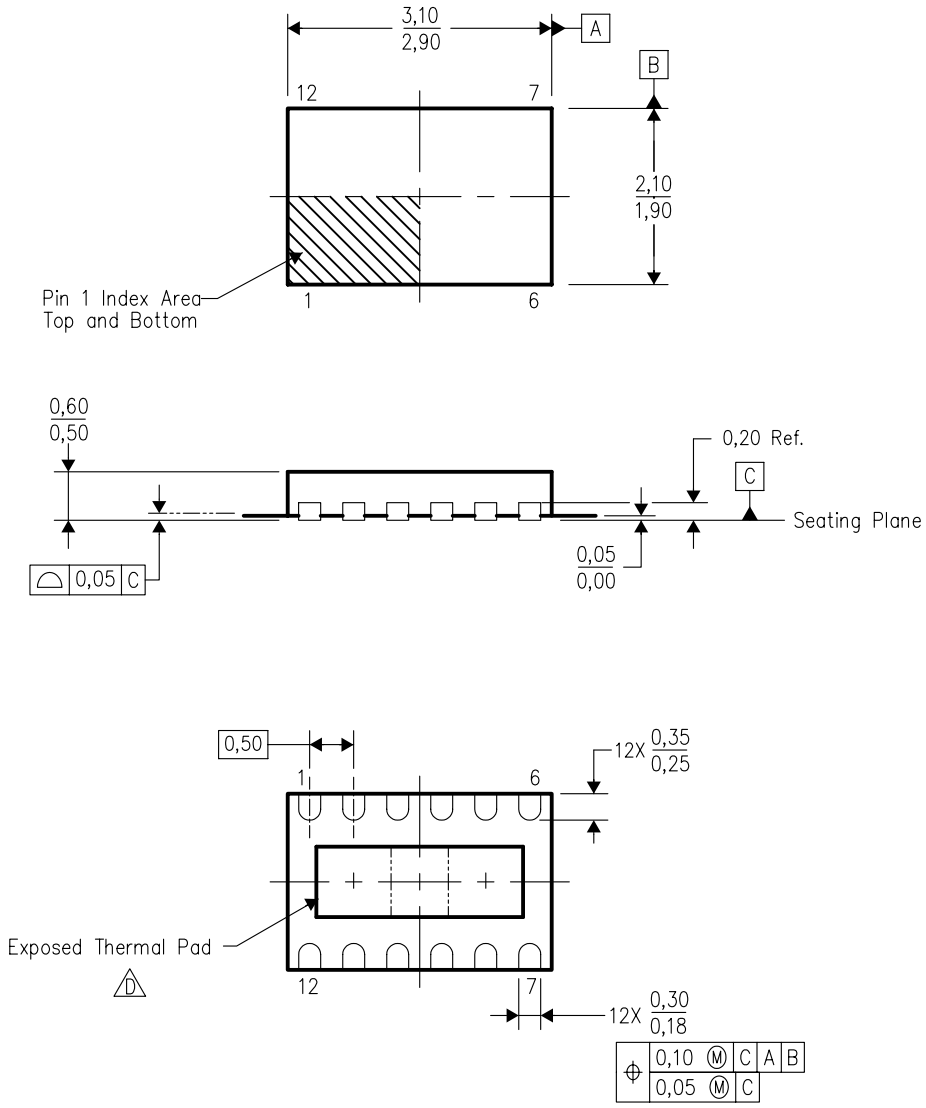
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28230DRNR	USON	DRN	12	3000	210.0	185.0	35.0
UCC28230DRNT	USON	DRN	12	250	210.0	185.0	35.0
UCC28231DRNR	USON	DRN	12	3000	338.1	338.1	20.6
UCC28231DRNT	USON	DRN	12	250	210.0	185.0	35.0

DRN (R–PDSO–N12) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229.

THERMAL PAD MECHANICAL DATA

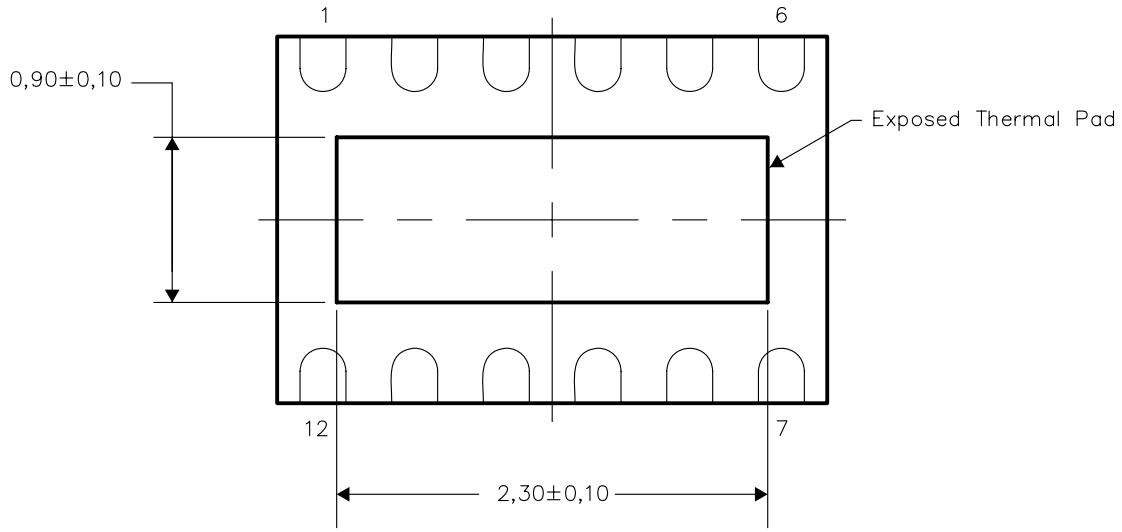
DRN (R–PDSO–N12)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

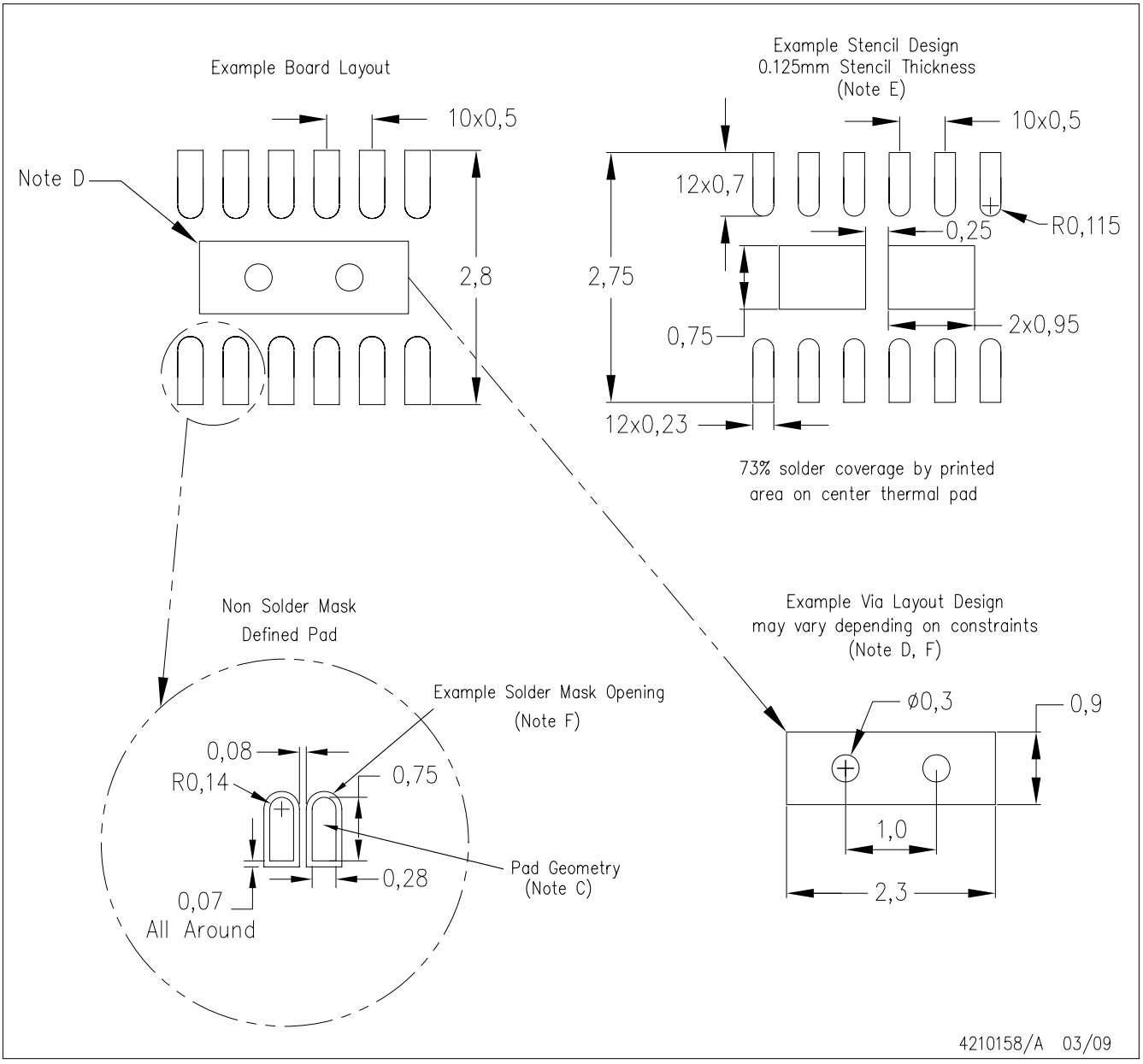


Bottom View

NOTE: All linear dimensions are in millimeters

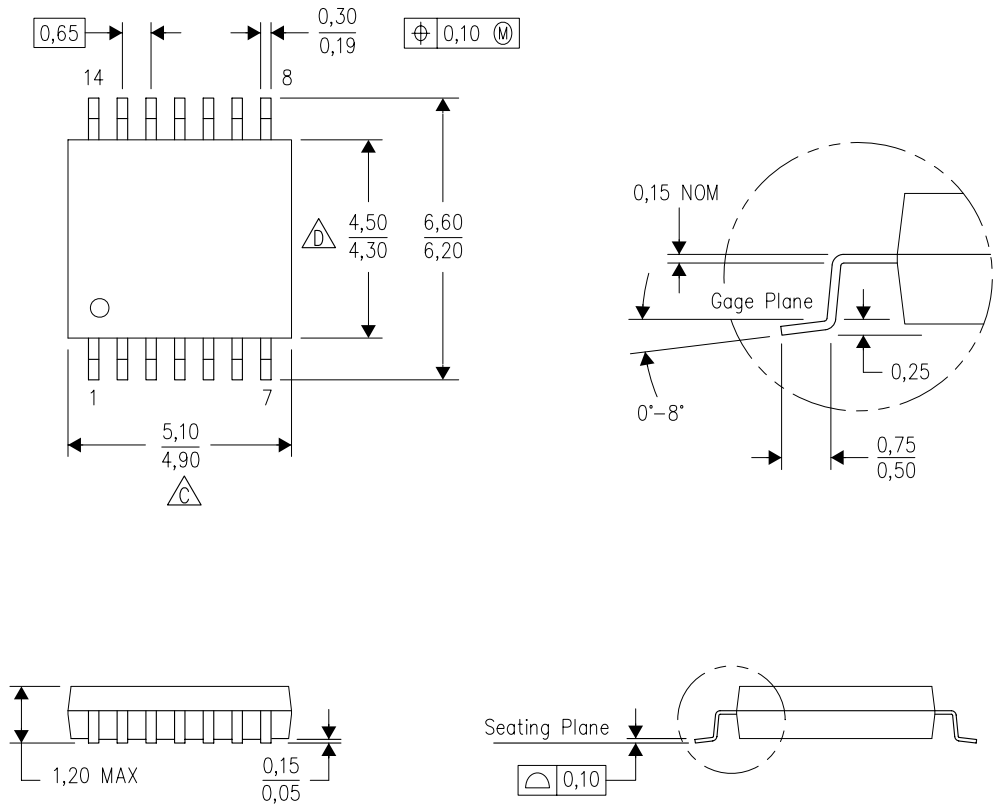
Exposed Thermal Pad Dimensions

DRN (R–PUSON–N12)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

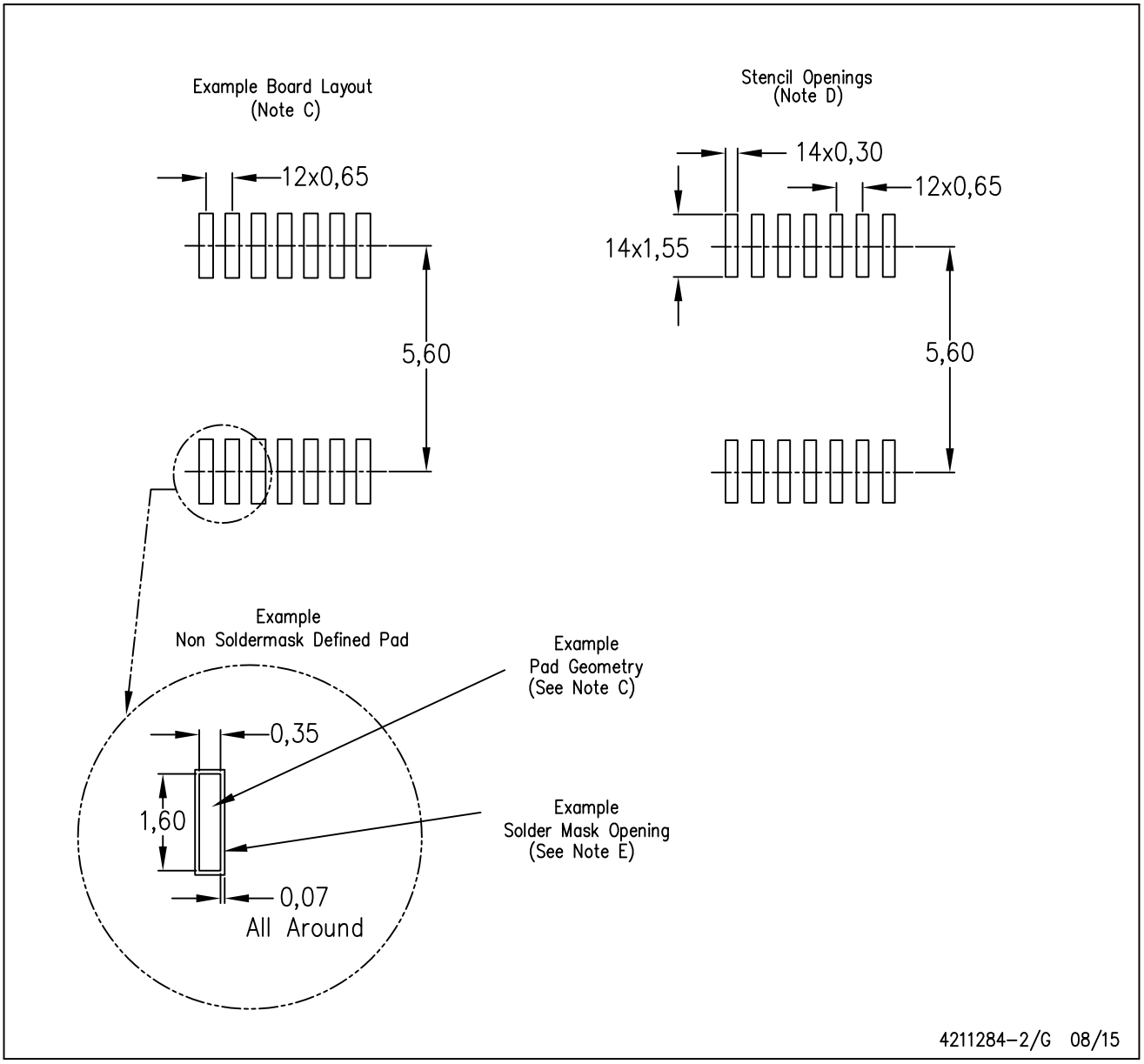
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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