

FEATURES

- USB/UART multi-function 16-bit PC Card device
- Host interface
 - 16-bit PC Card (PCMCIA revision 8.0) compliant
 - CompactFlash/CF+ (revision 3.0) compliant
- USB host controller
 - Supports USB 2.0/1.1 full-speed compliant (12 Mbps) & low speed (1.5 Mbps) devices
 - 8-Kbyte data buffer
 - Integrated OHCI-like controller supported by Oxford Semiconductor drivers
 - Supports control, bulk, interrupt & isochronous transfers
 - Supports USB PORT_OVER_CURRENT & PORT_POWER signals via MIO pins
- Integrated USB PHY transceivers
- Flexible OX16C95x-based UART
 - Supports 450 up to 950 (fully programmable)
 - Baud rates up to 12 Mbps
 - 128-byte deep transmit/receive FIFO
 - Software-compatible with standard 16C550
 - Readable FIFO levels
 - 9-bit data framing as well as 5,6,7 & 8
 - Detection of bad data in the receiver FIFO
- Optional wakeup from low-power mode
- Automated in-band flow control using programmable Xon/Xoff characters
- Automated hardware flow control using CTS#/RTS# & DSR#/DTR#
- Integral support for 4-byte I/O access for enhanced host-side data throughput
- 8-Kbit x 8 EEPROM for CIS & default configuration. Programmable using Oxford Semiconductor utilities
- Power management for low-power operation
 - USB suspend & resume
 - UART sleep mode
- Single 12-MHz crystal oscillator for low power
- 4 multi-purpose I/O pins configurable as interrupts
- UART & MIO pins have variable I/O voltage levels from 1.8 V to 3.3 V nominal
- PC Card/CF+ I/Os are all 3.3 V with 5-V tolerance
- Single supply voltage range 2.85 V to 3.6 V
- Internal regulation for 1.8 V
- Supply current
 - Less than 4 mA idle
 - Less than 13 mA active
- Industrial temperature range -40°C to +85°C
- 64-pin QFN (9 mm x 9 mm) package

DESCRIPTION

The OXCFU950 is a low-cost, synchronous 16-bit PC Card (PCMCIA) or CompactFlash/CF+ to UART and USB host controller. It combines the high performance of Oxford Semiconductor OX16C95x UART technology with USB host capabilities. The inclusion of both a UART and USB make the OXCFU950 ideal for wireless data cards.

The OXCFU950 integrates an OHCI-based USB host controller, which supports a single USB port via the integrated transceiver. An 8-Kbyte memory provides an efficient interface for buffer and control structures between the USB controller and the device driver.

The attribute memory, UART and USB registers can be programmed via the internal EEPROM during power up or hard/soft reset, allowing different card manufacturers to customize information contained in the attribute memory or UART/USB registers, for example PC Card ID value.

The 3.3-V technology has been specified to operate as low as 2.85 V to allow an in-line regulator to be used for mixed 3-V/5-V applications. CF/PC Card pins are 5-V tolerant and the variable I/O voltage to the UART/MIO pins eases the connection to application chipsets.

A number of power-down modes are included to minimize power consumption, including sleep modes for when a device function is not being used.

The OXCFU950 contains a single-channel ultra-high performance OX16C95x UART offering data rates up to 12 Mbps and 128-byte deep transmitter and receiver FIFOs. Deep FIFOs reduce CPU overhead and allow utilization of higher data rates.

The OXCFU950 USB controller supports OHCI-compliant host stack software (available from Oxford Semiconductor).

The OXCFU950 UART is software-compatible with the widely-used industry-standard 16C550 type devices and compatibles, as well as other OX16C95x family devices.

The addition of software resets enable the device to recover from unforeseen error conditions, allowing drivers to restart gracefully.

The OXCFU950 includes four user I/O pins to enhance external device control. These I/O pins can also be configured as interrupt inputs.

For simplicity, the host interface is referred to as the CompactFlash interface throughout this specification. Unless otherwise stated, this should be taken to include PCMCIA 16-bit Card operation as well as CompactFlash/CF+.

BLOCK DIAGRAM

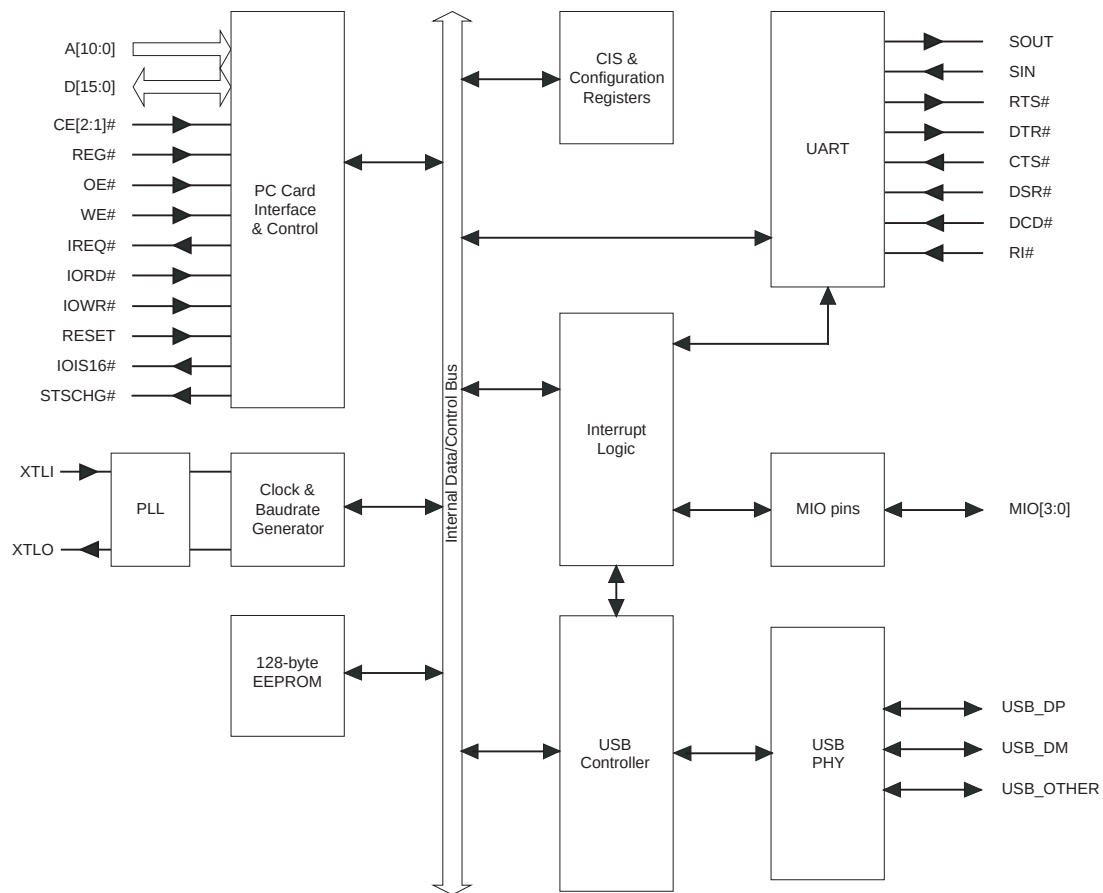


Figure 1: Block Diagram

PIN INFORMATION

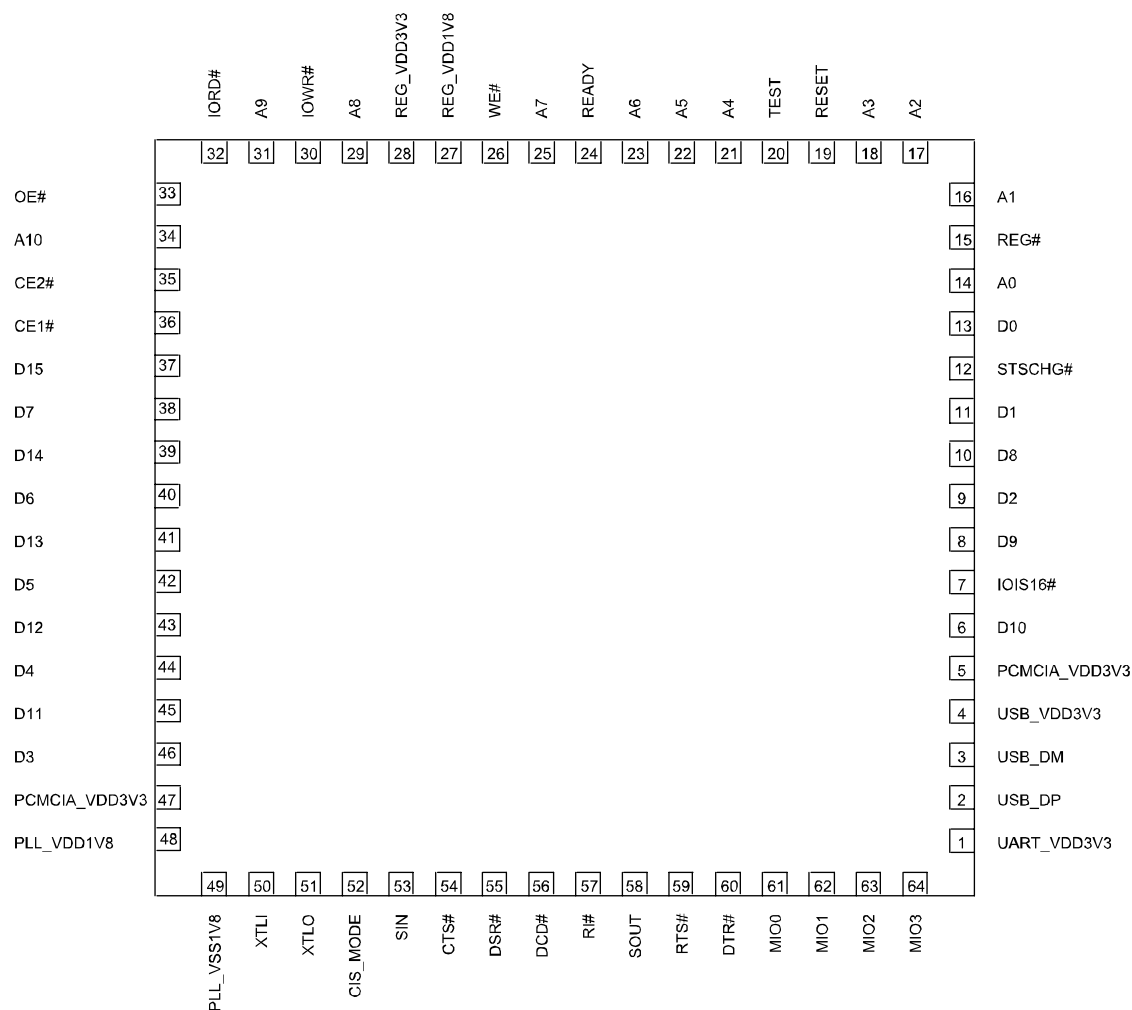


Figure 2: OXCFU950 Pin Information (QFN64)

PIN DESCRIPTIONS

Pin Number	Pad Type ^{Note 1}	Pin Name	Description
PC Card/Compact Flash Interface & Control ^{Note 2}			
14,16,17,18,21,22,23,25,29,31, 34	I_C_33_5_N_	A[10:0]	PC Card/CompactFlash address bus, bits [10:0]
13,11,9,46,44,42,40,38,10,8,6,45,43,41,39,37	B_T_33_5_N_2_	D[15:0]	PC Card/CompactFlash data bidirectional bus.
15	I_C_33_5_N_	REG#	Register select and I/O enable.
35,36	I_C_33_5_N_	CE[2:1]#	Active-low card enable.
33	I_C_33_5_N_	OE#	Active-low output enable used to gate memory read data (attribute memory). Host must negate the OE# signal during write operations.
26	I_C_33_5_N_	WE#	Active-low write enable used for strobing memory write data (attribute memory).
32	I_C_33_5_N_	IORD#	Active-low I/O read enable.
30	I_C_33_5_N_	IOWR#	Active-low I/O write enable.
7	O_T_33_1	WP	Write protect (in memory-only mode).
		IOIS16#	Data is 16-bit (in I/O & memory mode).
19	I_C_33_5_S_	RESET	PC Card/CompactFlash reset. Note : This pin requires an external reset pulse generator (RC network) to allow for the startup time for the internal oscillator and PLL.
24	O_T_33_2	READY	Device ready (in memory-only mode).
		IREQ#	Active-low Interrupt request (in I/O & memory mode). Indicates to the host system that the PC Card/CF requires host software service. Note: interrupt can support level or pulsed types.
12	O_T_33_2	BVD1	Battery voltage detect 1 (in memory-only mode). Not supported so held static.
		STSCHG#	Active-low status-changed pin (in memory & I/O mode). Used to alert the host system that the card status has changed. In this case it means that a function's ready state has changed. The host should check this by considering each function's PRR.
5,28,47	P_33	PCMCIA_VDD3V3	Connected internally.
UART (MODEM) Function ^{Note 3}			
58	O_T_33_1	SOUT	UART serial data output.
		IrDA_Out	UART IrDA data output when MCR[6] is set in enhanced mode.
53	I_C_33_5_N_	SIN	UART serial data input.
		IrDA_In	UART IrDA data input when IrDA mode is enabled (see above).
56	I_C_33_5_N_	DCD#	Active-low modem data-carrier-detect input.
60	O_T_33_1	DTR#	Active-low modem data-terminal-ready output. If automated DTR# flow control is enabled, the DTR# pin is asserted & deasserted if the receiver FIFO reaches or falls below the programmed thresholds.
		485_En	In RS485 half-duplex mode, the DTR# pin may be programmed to reflect the state of the transmitter empty bit to control the direction of the RS485 transceiver buffer automatically (see register ACR[4:3]).
59	O_T_33_1	RTS#	Active-low modem request-to-send output. If automated RTS# flow control is enabled, the RTS# pin is de-asserted & reasserted when the receiver FIFO reaches or falls below the programmed thresholds.
54	I_C_33_5_N_	CTS#	Active-low modem clear-to-send input. If automated CTS# flow control is enabled, upon de-assertion of the CTS# pin the transmitter completes the current character & enters idle mode until the CTS# pin is reasserted. Note: flow control characters are transmitted regardless of the state of the CTS# pin.

Pin Number	Pad Type ^{Note 1}	Pin Name	Description
55	I_C_33_5_N_	DSR#	Active-low modem data-set-ready input. If automated DSR# flow control is enabled, upon de-assertion of the DSR# pin, the transmitter completes the current character & enters idle mode until the DSR# pin is reasserted. Note: flow control characters are transmitted regardless of the state of the DSR# pin.
57	I_C_33_5_N_	RI#	Active-low modem ring-indicator input.
1	P_33	UART_VDD3V3	Power supply to UART and MIO I/O interfaces. Voltage on these pins should be tied to 1.8 V to 3.3 V supply (depending on requirement).
Crystal Oscillator / PLL pins^{Note4}			
51	A_18	XTLO	Crystal oscillator output.
50	A_18	XTLI	Crystal oscillator input. Frequency = 12 MHz. Note : a pull-down resistor of 500 K Ω is required on this pin.
49	P_18	PLL_VSS1V8	Ground (0 Volts) for PLL & oscillator cells. This pin should be tied to ground.
48	P_18	PLL_VDD1V8	Power supply for PLL & oscillator cells. This pin should be tied to 1.8 volts (i.e. tied to REG_VDD1V8 pin).
USB^{Note 5}			
2	A_33	USB_DP	USB data plus.
3	A_33	USB_DM	USB data minus.
4	P_33	USB_VDD3V3	Power supply to USB I/O interface. This pin should be tied to 3.3 volts.
Multi-Purpose I/O^{Note 3}			
64,63,62,61	B_T_33_5_N_1_	MIO[3:0]	Multipurpose IO pins. Note: if enabled, MIO[3:0] can be used as an interrupt inputs. MIO[3:2] can be configured to act as the USB power management control signals PORT_OVER_CURRENT & PORT_POWER
Miscellaneous Pins/Pads^{Note2}			
52	I_C_33_5_N_U	CIS_MODE	Test mode select pin/default CIS select
20	I_C_33_5_N_D	TEST	Test pin. This pin should be tied to VSS for normal operation.
Additional Power and Ground			
65 (Thermal bonding pad)	P_00	VSS	Main digital ground pin. The VSS pin should be tied to ground. Note this is the thermal bonding pin underneath the 64-pin QFN package
27	P_18	REG_VDD1V8	Output supply from internal voltage regulator at 1.8 V. Can be used as power supply to PLL (i.e. pin #48).

Table 1: Pin Descriptions

Note 1 : Pad syntax description

Pad type	Syntax
Digital Input pad	t a xy h i p
Digital Output pad	t a xy d
Digital Tristate output pad	t a xy d
Digital Bidirectional pad	t a xy h i d p
Analogue pad	t xy
Power Pad	t xy

Table 2: Pad Type Syntax

Symbol	Description	Values
t	Pad type	I—input pad O—output pad T—Tri-state output pad B—Bidirectional pad A—Analogue pad P—Power pad
a	Logic type	C—cmos T—TTL
xy	Operating voltage	33—3V3 18—1V8 00—0 V (i.e. VSS Ground)
h	Tolerant input voltage level	5—5 V N—same as operating voltage
i	Input type	N—normal S—Schmitt
d	Output drive strength	1—x1 drive strength 2—x2 drive strength 3—x3 drive strength
p	Pull up/down resistor	U—pull up resistor D—pull down resistor

Table 3: Pad Type Syntax Symbol Descriptions

Note 2 : PC Card/CompactFlash Power Domain Group

- This group of signals is in the PC Card/CompactFlash power domain group.
- Supply voltage range is specified from 2.85 V to 3.6 V.
- This is also the internally connected supply to the internal regulator. Hence pin #28 should be connected to the PC Card/CompactFlash supply source.

Note 3 : Modem Power Domain Group

- This group of I/O signals is in the MODEM power domain group.
- Supply voltage range is specified from 1.8 V to 3.6 V.

Note 4 : Analogue Power Domain Group

- This group of I/O signals is in the analogue power domain group (which supplies the oscillator and PLL).

Note 5 : USB Power Domain Group

- This group signals is in the USB power domain group.
- Supply voltage range is specified from 2.85 V to 3.6 V.

APPLICATION

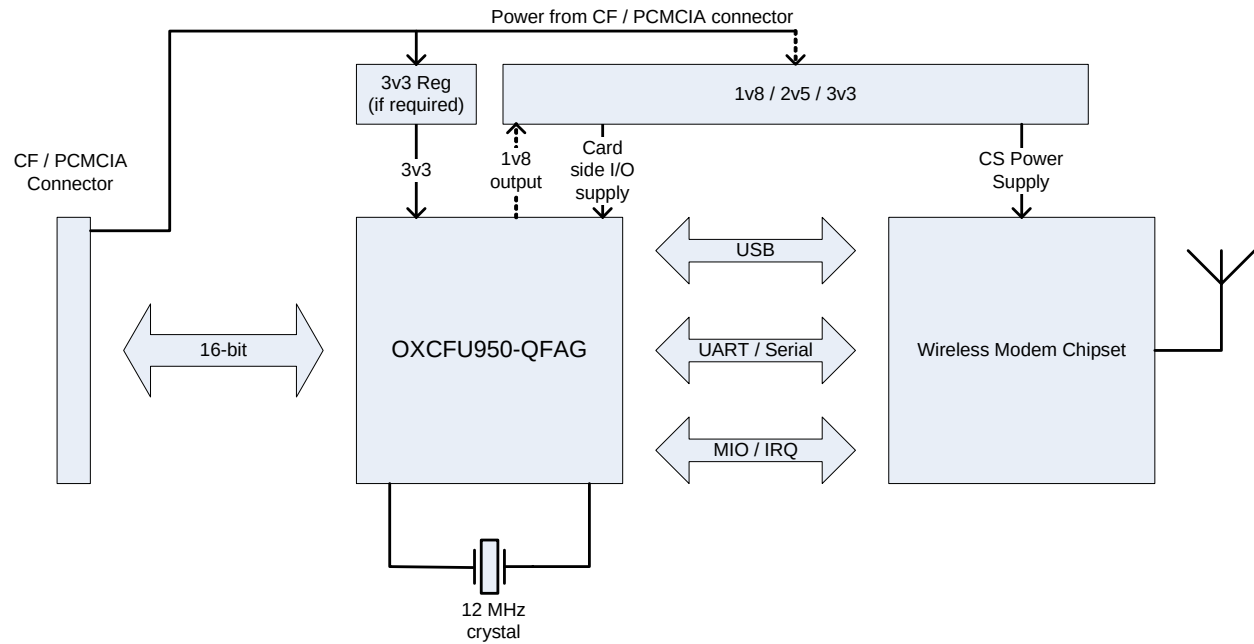
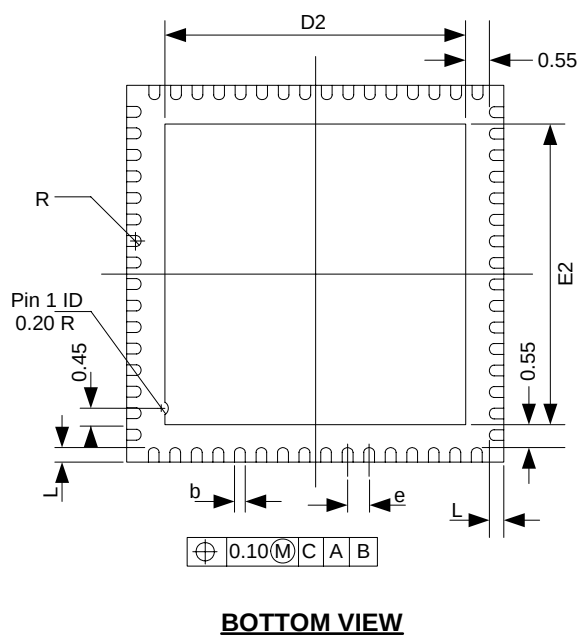
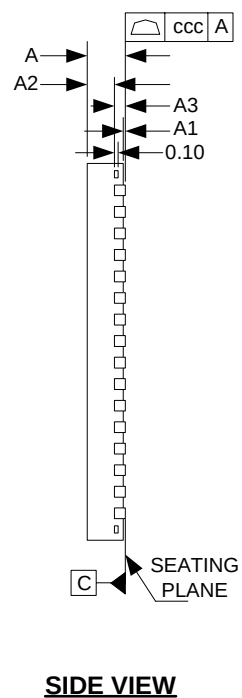
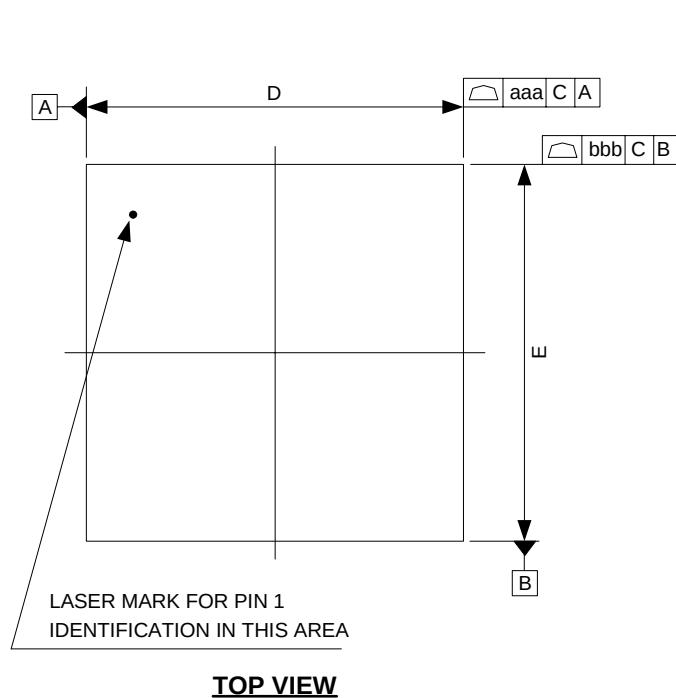


Figure 3: Sample Application

PACKAGE DETAILS

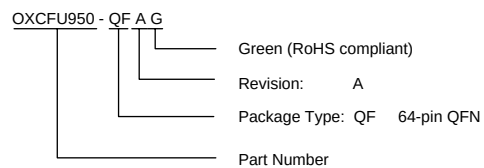


Package Dimensions

Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A	---	---	0.90	---	---	0.035
A1	---	---	0.05	---	---	0.001
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.23	0.25	0.28	0.009	0.010	0.011
D	9.00 bsc			0.354 bsc		
D2	6.95	7.10	7.25	0.274	0.280	0.285
E	9.00 bsc			0.354 bsc		
E2	6.95	7.10	7.25	0.274	0.280	0.285
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.125	---	---	0.005	---	---
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

ORDERING INFORMATION

The following conventions are used to identify Oxford Semiconductor products:



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