Designer's™ Data Sheet
SCANSWITCH™

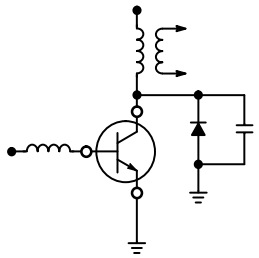
NPN Bipolar Power Deflection Transistor For High and Very High Resolution Monitors

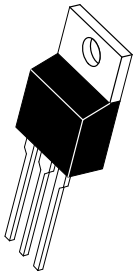
MJE16204

POWER TRANSISTORS
6.0 AMPERES
550 VOLTS — V_{CES}
45 AND 80 WATTS

The MJE16204 is a state–of–the–art SWITCHMODE™ bipolar power transistor. It is specifically designed for use in horizontal deflection circuits for 20 mm diameter neck, high and very resolution, full page, monochrome monitors.

- **550 Volt Collector–Base Breakdown Capability**
- Typical Dynamic Desaturation Specified (New Turn–Off Characteristic)
- Application Specific State–of–the–Art Die Design
- Isolated or Non–Isolated TO–220 Type Packages
- Fast Switching:
  65 ns Inductive Fall Time (Typ)
  680 ns Inductive Storage Time (Typ)
- Low Saturation Voltage:
  0.4 Volts at 3.0 Amps Collector Current and 400 mA Base Drive
- Low Collector–Emitter Leakage Current — 100 μA Max at 550 Volts — V_{CES}
- High Emitter–Base Breakdown Capability For High Voltage Off Drive Circuits — 9.0 Volts (Min)
- Case 221D is UL Recognized at 3500 V_{RMS}: File #E69369





CASE 221A–06
TO–220AB
MJE16204

MAXIMUM RATINGS

Rating	Symbol	MJE16204	Unit
Collector–Emitter Breakdown Voltage	V_{CES}	550	Vdc
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	250	Vdc
Emitter–Base Voltage	V_{EBO}	8.0	Vdc
RMS Isolation Voltage(2) Per Fig. 14 (for 1 sec, T_A = 25°C, Per Fig. 15 Rel. Humidity < 30%) Per Fig. 16	V_{ISOL}	— — —	V
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	6.0 8.0	Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	2.0 4.0	Adc
Repetitive Emitter–Base Avalanche Energy	$W_{(BER)}$	0.2	mJ
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above T_C = 25°C	P_D	80 32 0.64	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARCTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.56	°C/W
Lead Temperature for Soldering Purposes 1/8″ from the case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.
* Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink thermal grease applied, and a mounting torque of 6 to 8 in•lbs.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

SCANSWITCH, SWITCHMODE and Designer's are trademarks of Motorola, Inc.

(REPLACES MJF16204)

© Motorola, Inc. 1995

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector Cutoff Current (V_{CE} = 550 Vdc, V_{BE} = 0 V)	I_{CES}	—	—	100	μAdc
Emitter–Base Leakage (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	—	—	10	μAdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mA, I_C = 0)	$V_{(BR)EBO}$	8.0	11	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	325	—	Vdc
ON CHARACTERISTICS (1)					
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 133 mAdc) (I_C = 3.0 Adc, I_B = 400 mAdc)	$V_{CE(sat)}$	— —	0.25 0.4	0.6 1.0	Vdc
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 400 mAdc)	$V_{BE(sat)}$	—	0.9	1.5	Vdc
DC Current Gain (ICE = 6.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	8.0	14	20	—
DYNAMIC CHARACTERISTICS					
Dynamic Desaturation Interval (I_C = 3.0 A, I_{B1} = 400 mA)	t_{ds}	—	50	—	ns
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	90	150	pF
Gain Bandwidth Product (V_{CE} = 10 Vdc, I_C = 1.0 A, f_{test} = 1.0 MHz)	f_T	10	—	—	MHz
Emitter–Base Turn–Off Energy ($EB_{(avalanche)}$ = 500 ns, R_{BE} = 22 Ω)	$EB_{(off)}$	—	6.6	—	μJ
Collector–Heatsink Capacitance (Mounted on a 1″ x 2″ x 1/16″ Copper Heatsink, V_{CE} = 0, f_{test} = 100 kHz)	$C_{c–hs}$	—	3.0	—	pF
SWITCHING CHARACTERISTICS					
Inductive Load (Table 2) (I_C = 3.0 A, I_B = 400 mA) Storage Fall Time	 t_{sv} t_{fi}	 — —	 680 65	 1500 150	ns

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

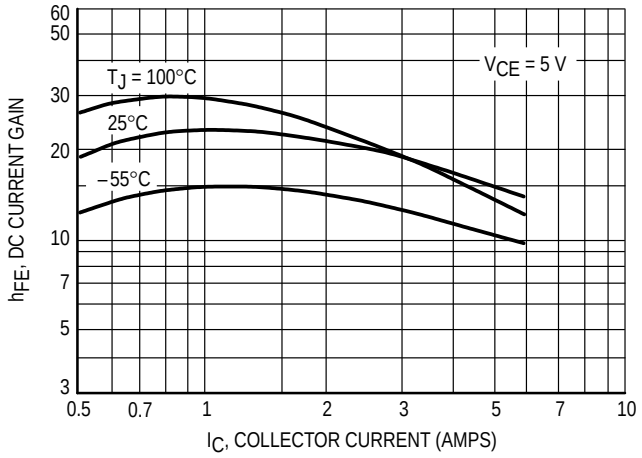


Figure 1. Typical DC Current Gain

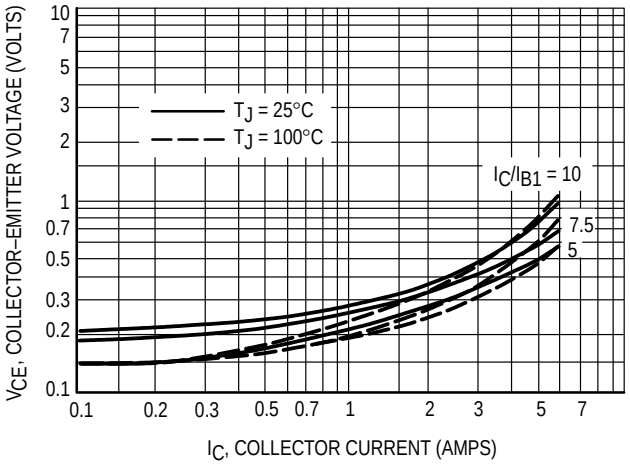


Figure 2. Typical Collector–Emitter Saturation Voltage

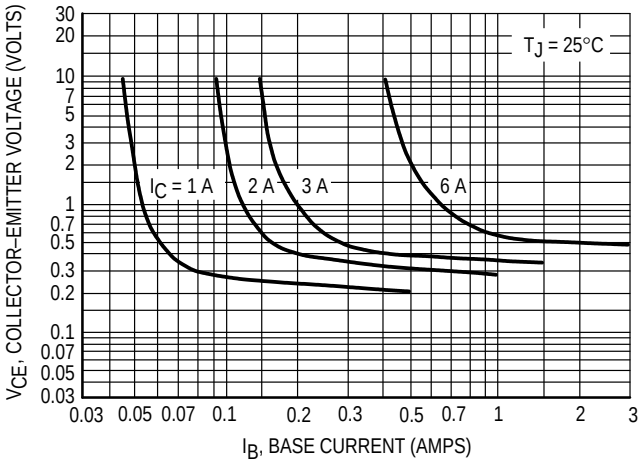


Figure 3. Typical Collector–Emitter Saturation Region

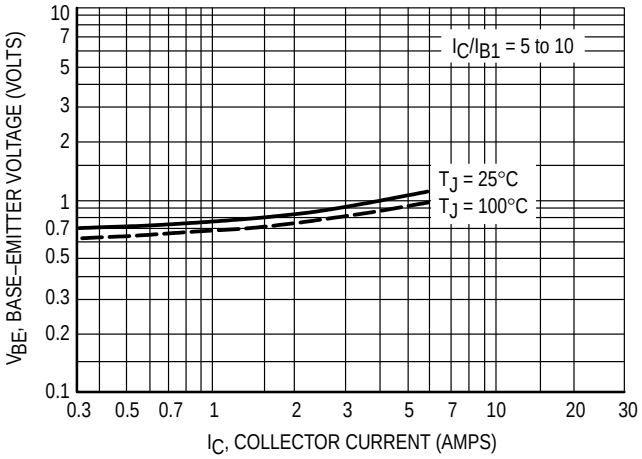


Figure 4. Typical Base–Emitter Saturation Voltage

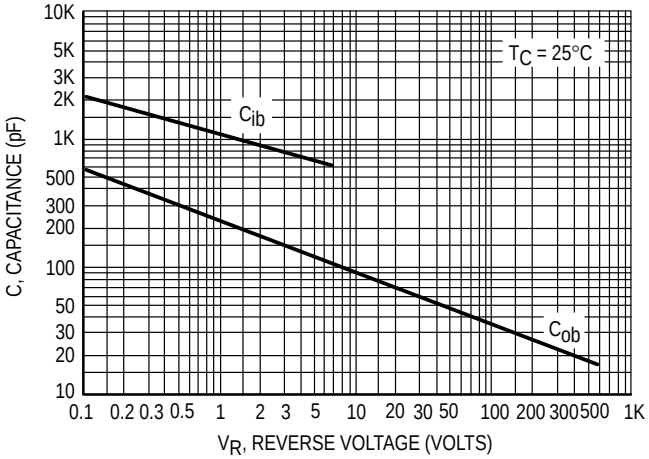


Figure 5. Typical Capacitance

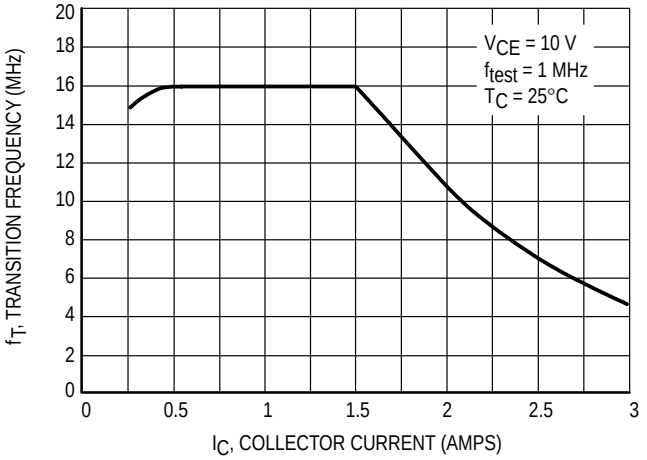


Figure 6. Typical Transition Frequency

SAFE OPERATING AREA

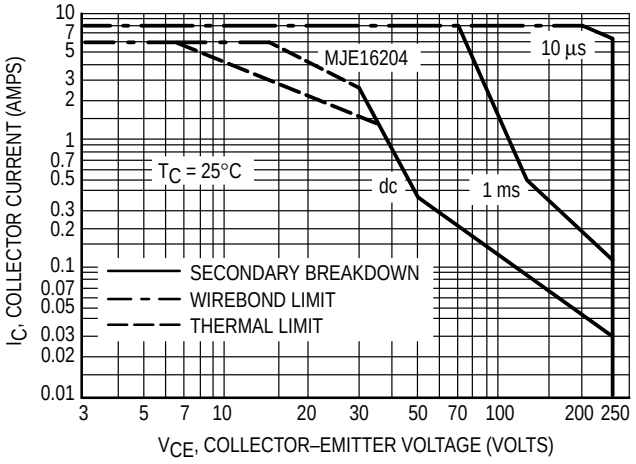


Figure 7. Maximum Forward Biased Safe Operating Area

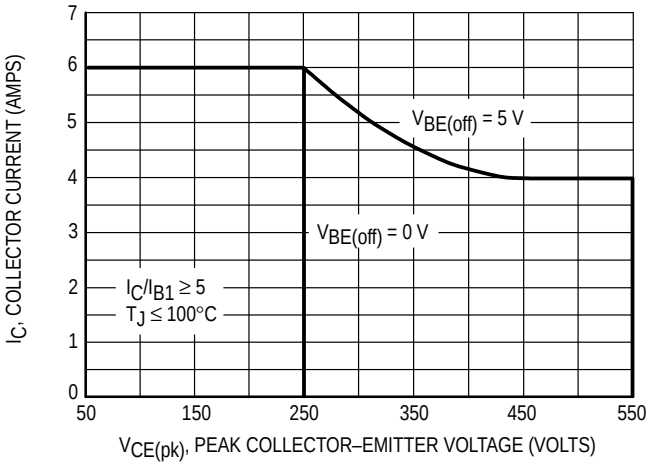


Figure 8. Maximum Reverse Biased Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

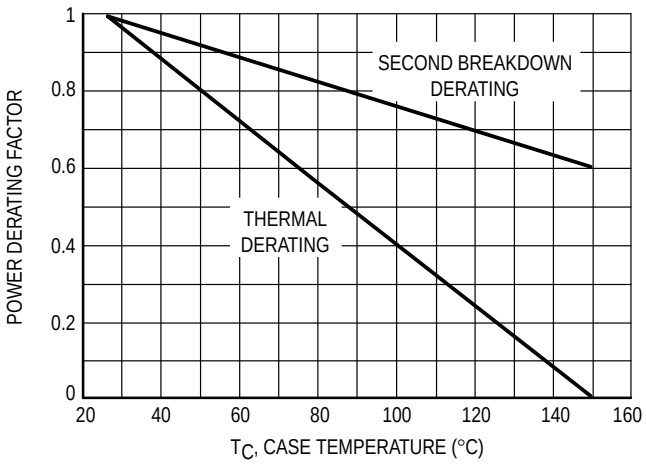


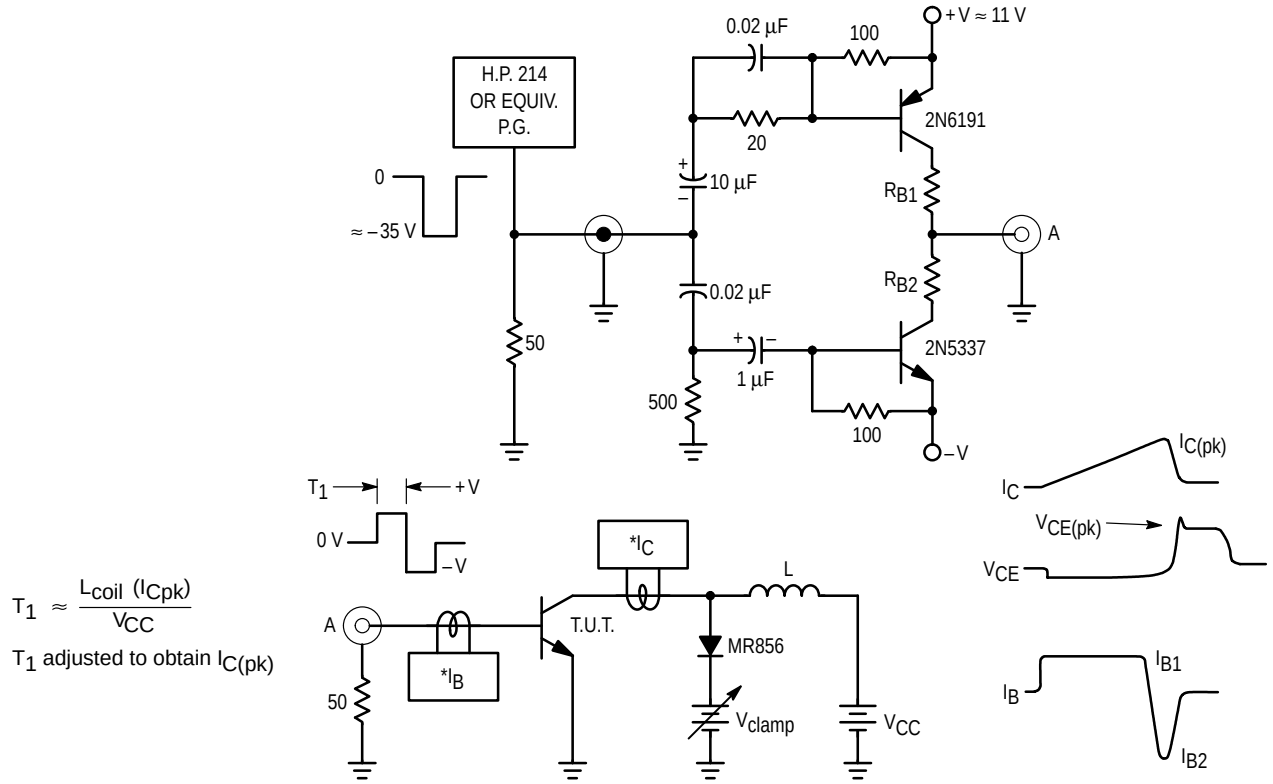
Figure 9. Power Derating

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc.

The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the RBSOA characteristics.

Table 1. RBSOA/$V_{(BR)CEO(sus)}$ Test Circuit



$$T_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

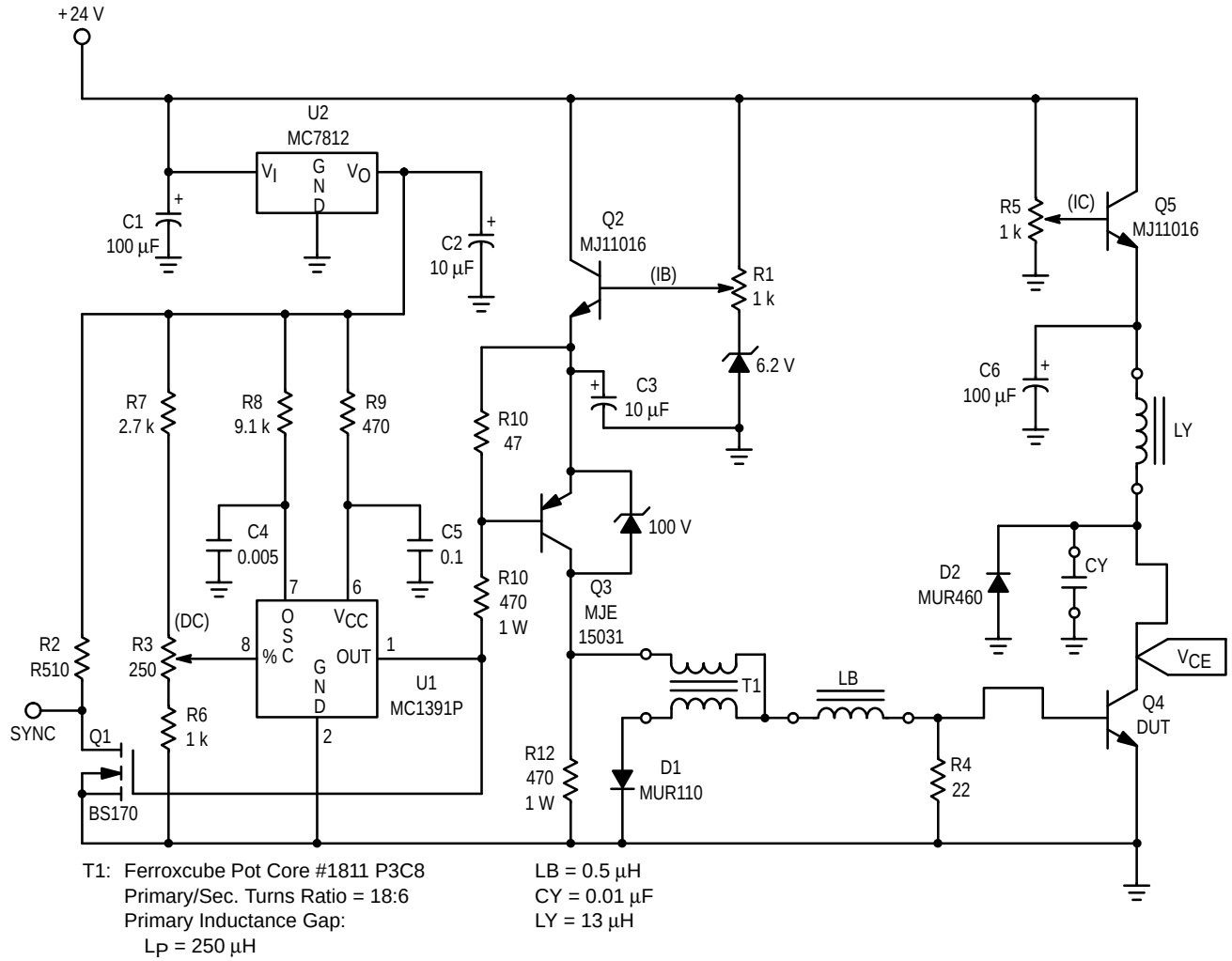
$V_{(BR)CEO}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

*Tektronix
P–6042 or
Equivalent

RBSOA
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

Table 2. High Resolution Deflection Application Simulator



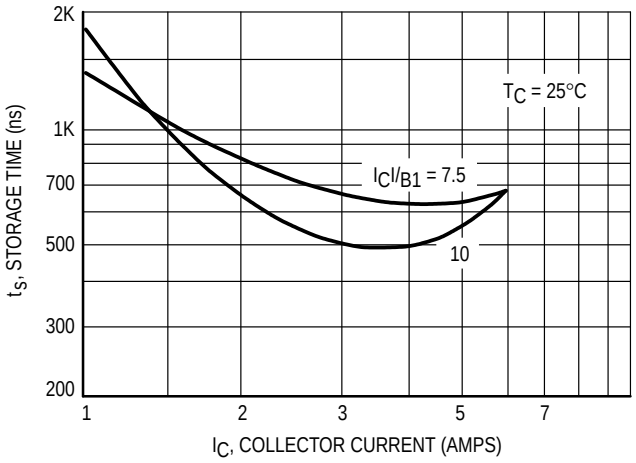


Figure 10. Typical Collector Current Storage Time in Deflection Circuit Simulator

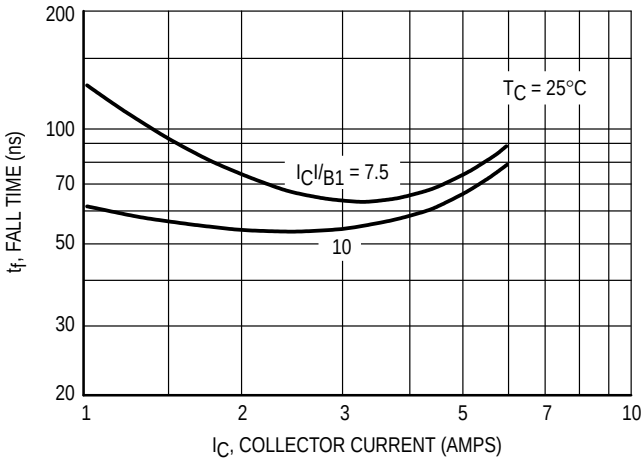


Figure 11. Typical Collector Current Fall Time in Deflection Circuit Simulator

DYNAMIC DESATURATIION

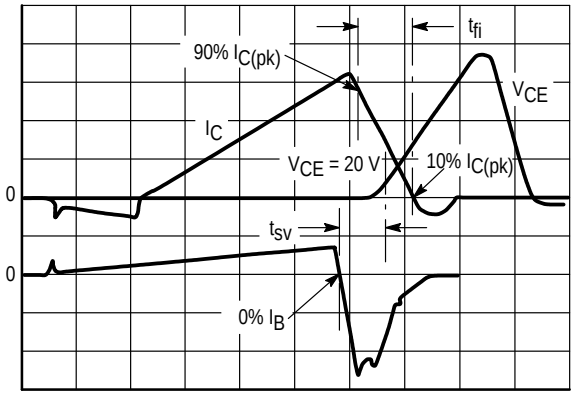


Figure 12. Deflection Simulator Switching Waveforms From Circuit in Table 2

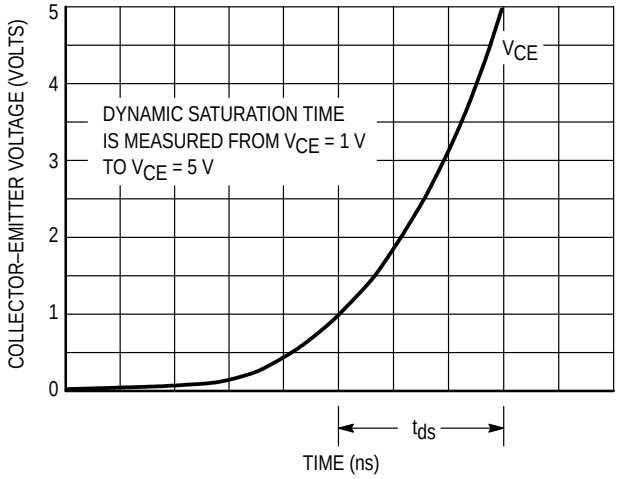


Figure 13. Definition of Dynamic Saturation Measurement

The SCANSWITCH series of bipolar power transistors are specifically designed to meet the unique requirements of horizontal deflection circuits in computer monitor applications. Historically, deflection transistor design was focused on minimizing collector current fall time. While fall time is a valid figure of merit, a more important indicator of circuit performance as scan rates are increased is a new characteristic, “dynamic desaturation.” In order to assure a linear collector current ramp, the output transistor must remain in hard saturation during storage time and exhibit a rapid turn–off transition. A sluggish transition results in serious consequences. As the saturation voltage of the output transistor increases, the voltage across the yoke drops. Roll off in the collector current ramp results in improper beam deflection and distortion of the image at the right edge of the screen. Design changes have been made in the structure of the SCANSWITCH series of devices which minimize the dynamic desaturation interval. Dynamic desaturation has been defined in terms of the time required for the V_{CE} to rise from 1.0 to 5.0 volts (Figures 12 and 13) and typical performance at optimized drive conditions has been specified. Optimization of device structure results in a linear collector current ramp, excellent turn–off switching performance, and significantly lower overall power dissipation.

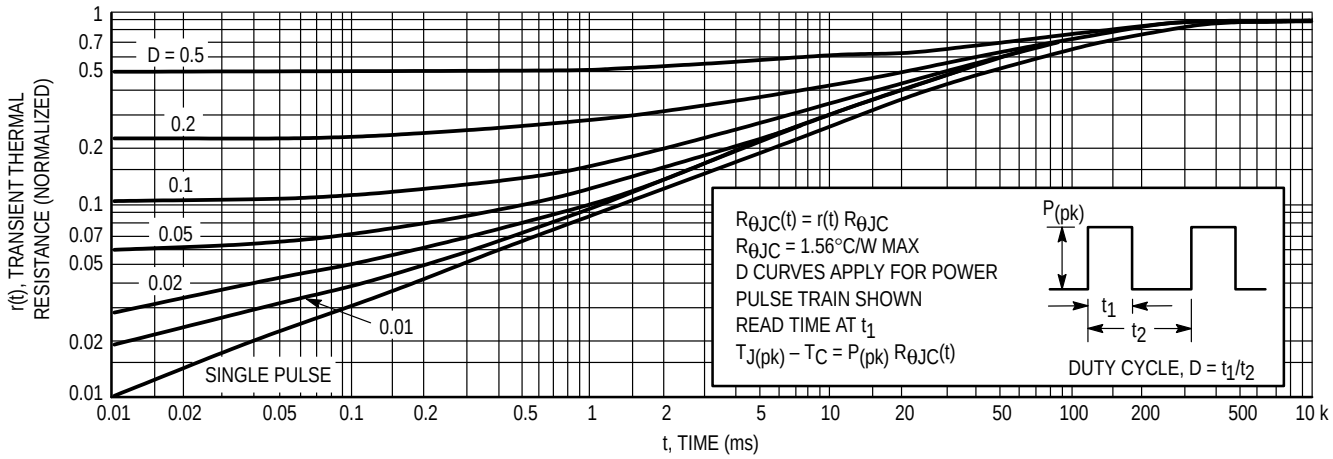
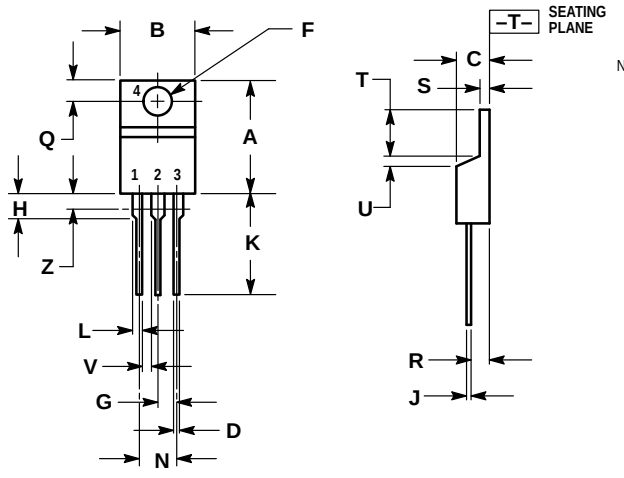


Figure 14. Typical Thermal Response for MJE16204

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–06
TO–220AB
ISSUE Y

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters can and do vary in different applications. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298