T73LVP20

3.3V LVTTL/LVCMOS-to-Differential LVPECL Translator

Applications

- LVPECL clock source

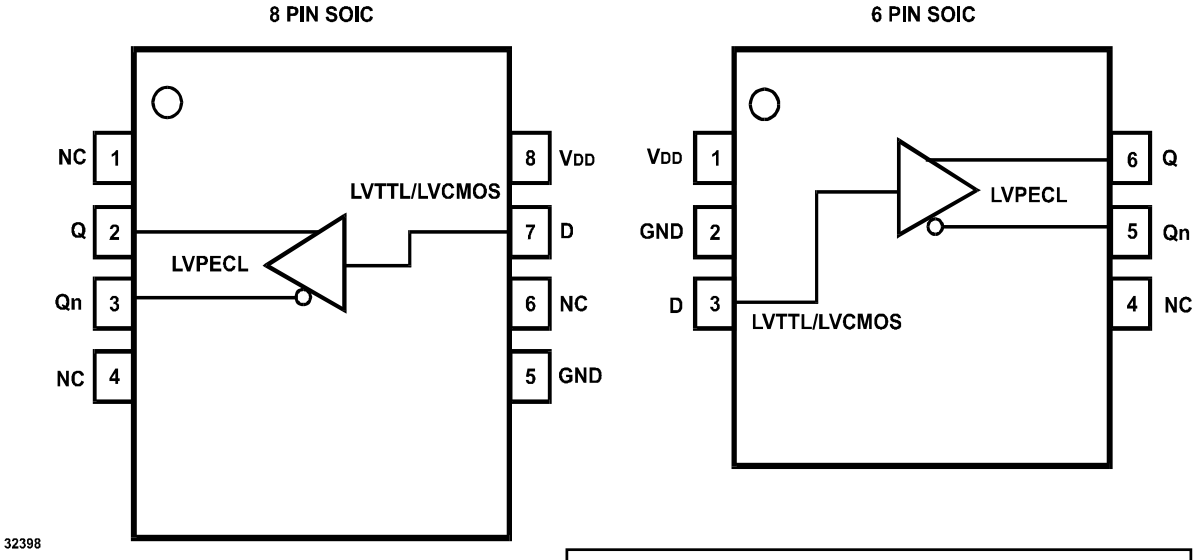
General Description

The TLSI T73LVP20 is a general-purpose LVTTL/LVCMOS-to-differential LVPECL translator operating from a single +3.3V supply. The device accepts an LVTTL or LVCMOS input and provides differential LVPECL outputs referenced to the positive supply rail. Both the tiny 6-pin SOT and 8-pin SOIC packages make it ideal for applications which require the translation of a clock or a data signal, and where cost, performance and size are of critical importance. The T73LVP20 is 100K PECL compatible and is **a pin-for-pin replacement for the MC100EPT20D (8-pin SOIC only).**

Features

- 350pS typical propagation delay
- Operating Frequency > 1 GHz
- Differential LVPECL outputs
- Flow-through pinout
- Q output defaults low with input (D) open
- ESD rating >2000V (Human Body Model) or >200V (Machine Model)
- -40 °C to +85 °C operating temperature range
- Available as die, in tiny 6-pin SOT or standard 8-pin SOIC packages

Figure 1. Functional Block Diagrams & Pin Assignments (Top View)



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See pages 4 & 5 for package outline drawings and ordering information.

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Table 1. Pin Description

Name	Description	Type	8-SOIC Pin #	6-SOT Pin #
NC	No Connection	-	1, 4, 6	4
Q	PECL data output	O	2	6
Q_n	PECL complementary data output	O	3	5
V_{DD}	Connect to +3.3V	P	8	1
D	LVTTL/LVCMOS data input	I	7	3
GND	Connect to ground	P	5	2

Legend: I = Input
O = Output
P = Power supply connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply voltage	Referenced to GND			+5.0	V
V_{IN}	Input voltage	Referenced to GND	-0.5		V_{DD}	V
I_{OUT}	Output current	Continuous			50	mA
T_{STG}	Storage temperature		-65		+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply Voltage		+3.0	+3.3	+3.6	V
T_A	Ambient Temperature		-40		+85	°C
V_{IH}	Input HIGH Voltage		+2.0			V
V_{IL}	Input LOW Voltage				+0.8	V

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Table 4. DC Characteristics

T_A = -40°C to +85°C, V_{DD} = +3.0V to +3.6V unless otherwise stated below.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	Input HIGH Current	V_{IN} =+2.7V				100	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V				1	µA
V_{IK}	Input Clamp Diode Voltage	I_{IN} = -18mA				-1.2	V
V_{OH}	Output HIGH Voltage(1, 2)	-40°C	V_{DD} = +3.3V	2220	2320	2420	mV
		+25°C		2220	2320	2420	mV
		+85°C		2220	2320	2420	mV
V_{OL}	Output LOW Voltage(1, 2)	-40°C	V_{DD} = +3.3V	1420	1520	1620	mV
		+25°C		1420	1520	1620	mV
		+85°C		1420	1520	1620	mV
I_{DD}	Power Supply Current	No Load			23		mA

Notes: 1. The T73LVP20 is designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board.
2. Q and Qn outputs are loaded with 50 ohms to V_{DD}-2 volts.

Table 5. AC Characteristics

T_A = -40°C to +85°C, V_{DD} = +3.0V to +3.6V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay (1)	To Output Differential		350	500	ps
t_{PHL}	Propagation Delay (1)	To Output Differential		350	500	ps
t_r/t_f	Output Rise/Fall time	20%-80%, Q, Q_n	80	130	200	ps
f_{MAX}	Maximum Input Frequency	LVTTL or LVCMOS input		> 1		GHz
f_{MAX}	Maximum Input Frequency (2)	750mV peak-to-peak sine wave centered around 1.5V		> 1		GHz

Notes: 1. Q and Qn outputs are loaded with 50 ohms to V_{DD}-2 volts.
2. Measured using a 750mV peak-to-peak, 50% duty cycle clock source.

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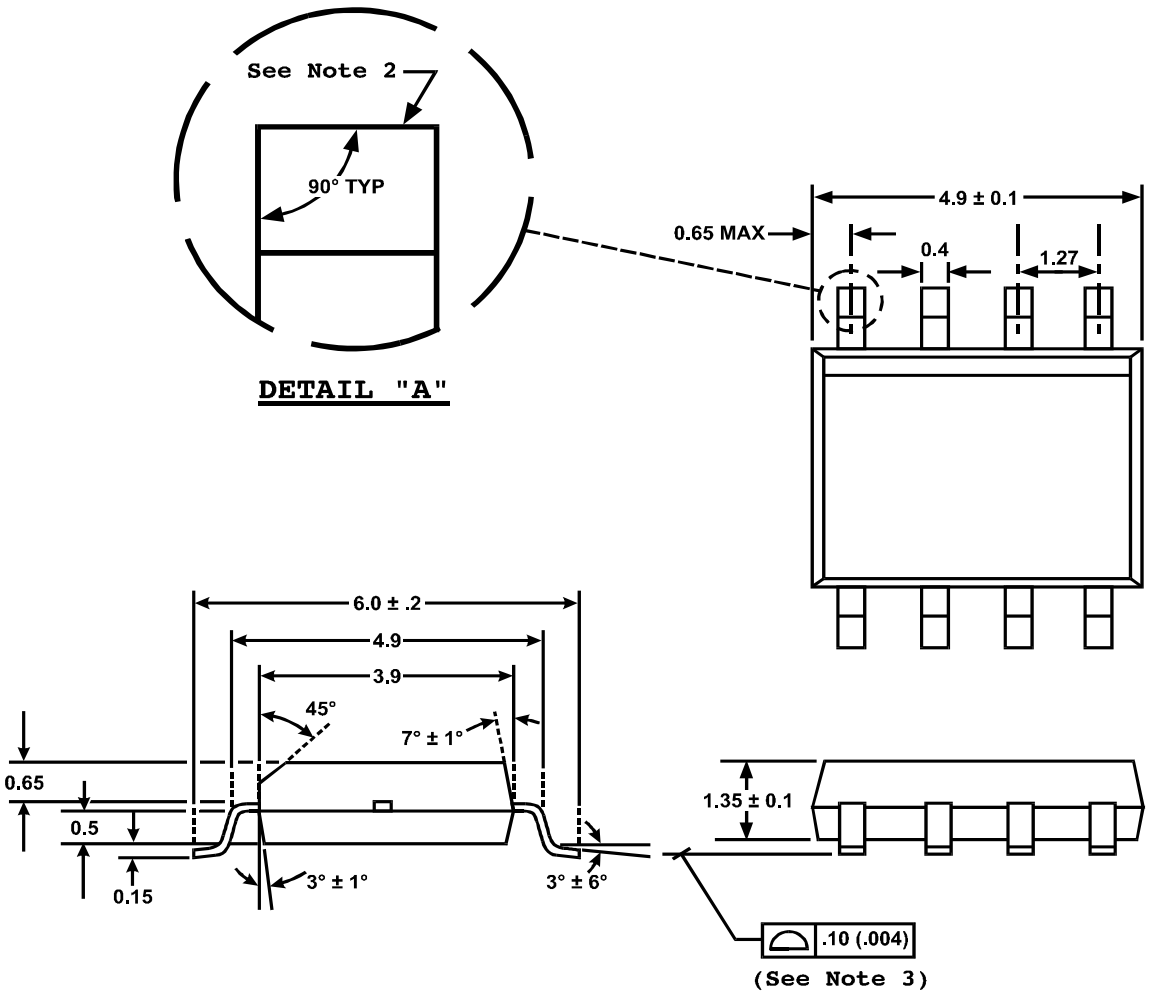
Figure 2. Package Outline (8-pin SOIC)



Note: 1) All dimensions are in mm.
2) All leads must be blunt cut. (See DETAIL "A")
3) Lead coplanarity not to exceed 0.004" maximum.

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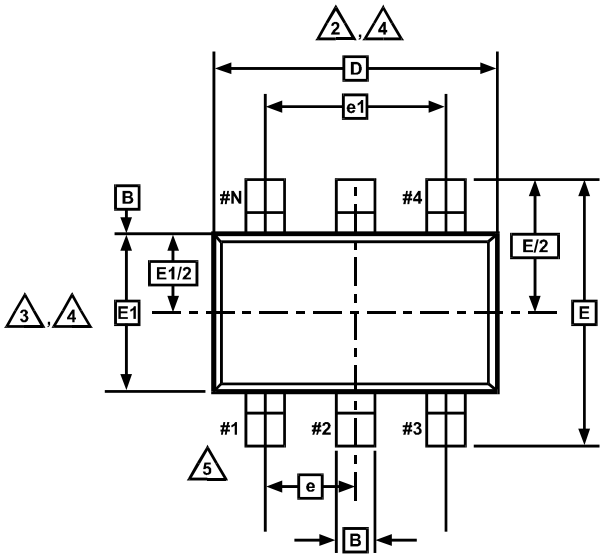
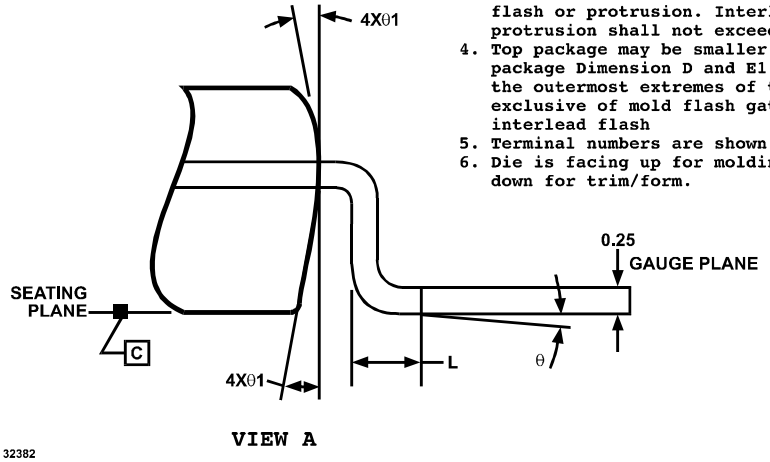
Figure 3. Package Outline (6-pin SOT)



SYMBOL	ALL DIMENSIONS IN MILLIMETERS	
	MINIMUM	MAXIMUM
A	1.20	1.40
A1	0.05	0.15
A2	1.15	1.25
B	0.35	0.50
c	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC.	
e1	1.90 BSC.	
L	0.35	0.55
θ	0"	8"
θ1	10" TYP.	

1. Dimensions are in millimeters.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.15 mm per side.
3. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
4. Top package may be smaller than the bottom package Dimension D and E1 are determine at the outermost extremes of the plastic body exclusive of mold flash gate burrs and interlead flash
5. Terminal numbers are shown for reference only.
6. Die is facing up for molding. Die is facing down for trim/form.



VIEW A

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Table 6. Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T73LVP20-S08	T73LVP20	Tubes	8	SOIC	-40°C to +85°C
T73LVP20-S08-TNR	T73LVP20	Tape & Reel	8	SOIC	-40°C to +85°C
T73LVP20-SOT	LVP20	Tubes	6	SOT	-40°C to +85°C
T73LVP20-SOT-TNR	LVP20	Tape & Reel	6	SOT	-40°C to +85°C
T73LVP20-DIE	N/A	Dice	6	N/A	-40°C to +85°C

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