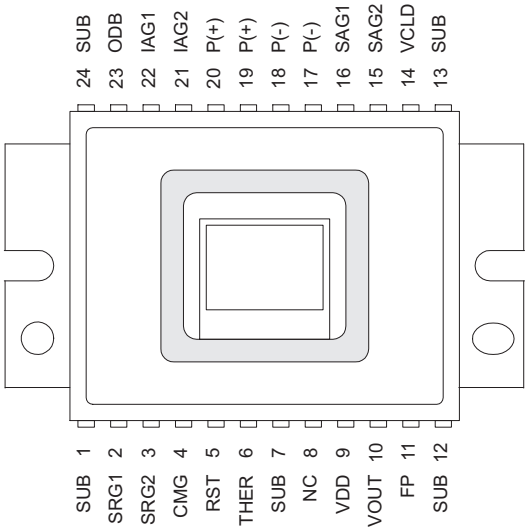
680 x 500 PIXEL IMPACTRON™ COLOR CCD IMAGE SENSOR

Check for Samples: TC246

FEATURES

- **Very Low Noise, Very High Sensitivity, Electronically Variable Charge Domain Gain**
- **1/2-in Format, Solid State Charge-Coupled Device (CCD) Frame Interline Transfer Color Image Sensor for Low Light Level Applications with 30 Frames/s or 60 Fields/s Readout Speed**
- **Color Mosaic Filters On Chip**
- **340,000 Pixels per Field**
- **Frame Memory**
- **658 (H) x 496 (V) Active Pixels in Image Sensing Area**
- **Multimode Readout Capability**
  - **Progressive Scan**
  - **Pseudo-Interlace Scan**
  - **Line Summing**
  - **Pixel Summing**
- **0-8 V Serial Operation Except CMG Gate**
- **Continuous Electronic Exposure Control from 1/30 s to 1/2,000 s**
- **Advanced Lateral Overflow Drain**
- **10.0-µm Square Pixels**
- **Low Dark Current**
- **RoHS-Compliant Product**
- **High Photoresponse Uniformity Over a Wide Spectral Range**
- **Solid State Reliability With No Image Burn-in, Residual Imaging, Image Distortion, or Microphonics**
- **Package with Built-in Peltier Cooler and Temperature Sensor**

DUAL-IN-LINE PACKAGE
(TOP VIEW)



DESCRIPTION

The TC246 is a frame interline transfer CCD image sensor designed for use in single-chip color NTSC TV, computer, and special-purpose applications requiring low noise, high sensitivity, high speed, and low smear.

The TC246 is a new device of the IMPACTRON™ family of very-low noise, high sensitivity, high speed and low smear sensors that multiply charge directly in the charge domain before conversion to voltage. The charge carrier multiplication (CCM) is achieved by using a low-noise single-carrier, impact ionization process that occurs during repeated carrier transfers through high field regions. Applying multiplication pulses to specially designed gates activates the CCM. Multiplication gain is variable by adjusting the amplitude of the multiplication pulses. The device function resembles the function of an image intensifier implemented in solid state.

The image-sensing area of the TC246 is configured into 500 lines with 680 pixels in each line. 20 pixels are reserved in each line for dark reference. The blooming protection is based on an advanced lateral overflow drain concept that does not reduce NIR response. The frame interline transfer from the image sensing area to the memory area is implemented to minimize image smear. After charge is integrated and stored in the memory it is available for readout in the next cycle. This is accomplished by using a unique serial register design that includes special charge multiplication pixels.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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The TC246 sensor is built using TI-proprietary advanced Split-Gate Virtual-Phase CCD (SGVPCCD) technology, which provides devices with wide spectral response, high quantum efficiency (QE), low dark current, and high response uniformity.

This MOS device contains limited built-in protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to Vss. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUT to Vss during operation to prevent damage to the amplifier. The device can also be damaged if the output and ADB terminals are reverse-biased and excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication "Electrostatic Discharge (ESD)" available from Texas Instruments.

NOTE

Attention to EMCCD users:

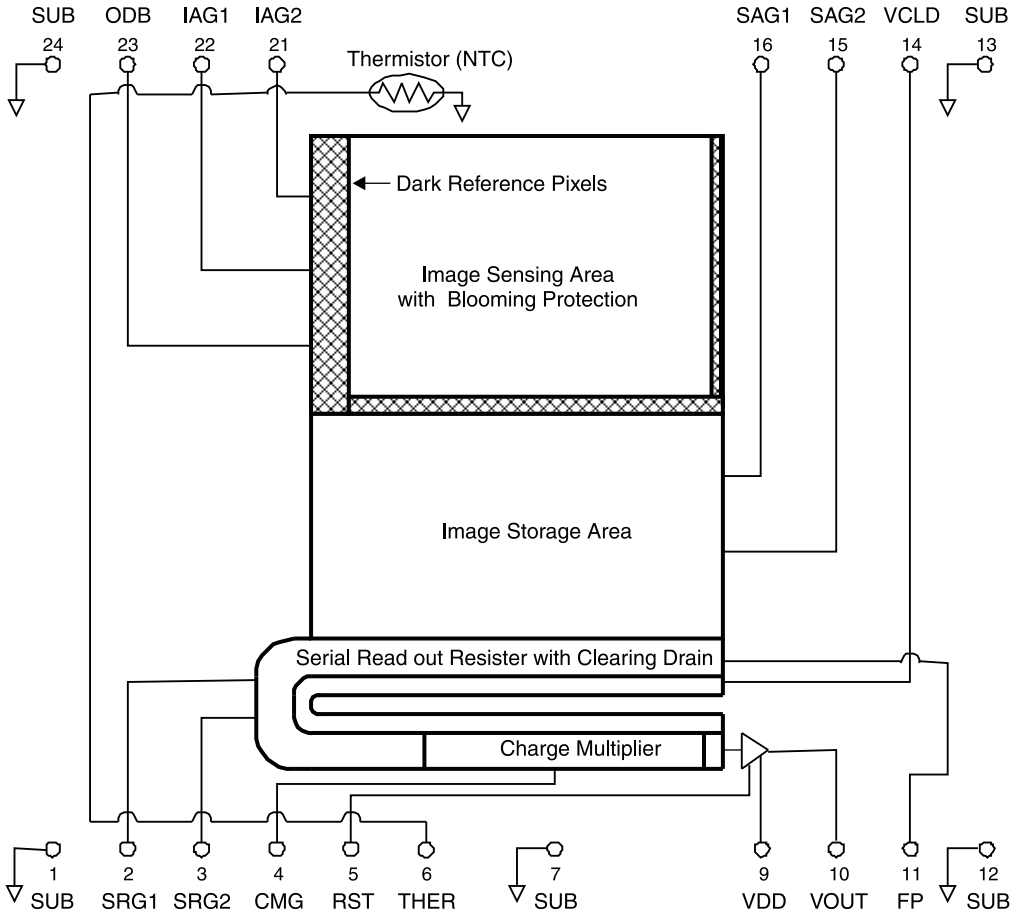
The charge carrier multiplication (CCM) gain shift can be observed over a period of time. As a results, a property fluctuation will occur under certain usage environment. In order to minimize the change in characteristics with time, it is better not to use CCM gains beyond necessity. Also exposing a sensor to a strong light source should be avoided.

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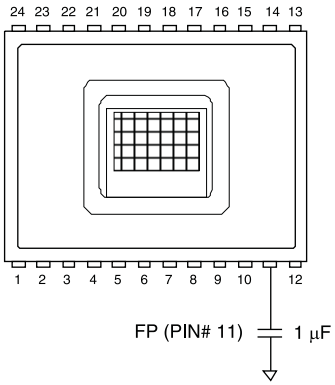
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

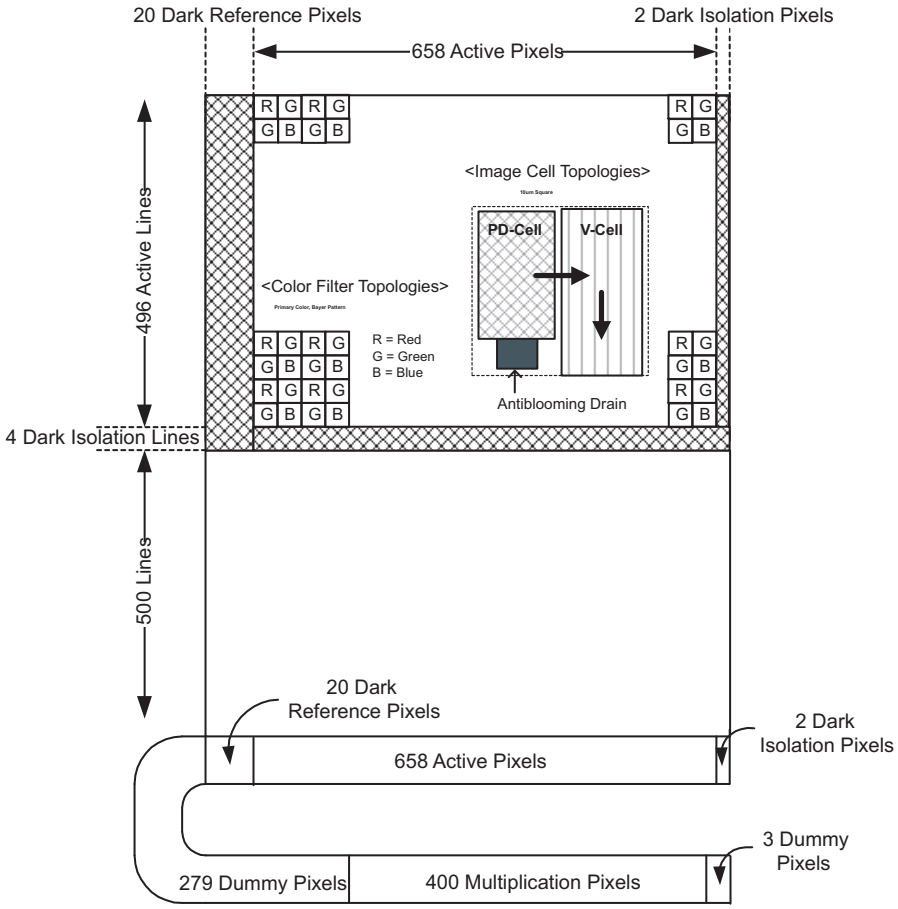
FUNCTIONAL BLOCK DIAGRAM



For stable operation, a decoupling capacitor (1 µF, >5 V) needs to be connected externally from the package FP pin to SUB.

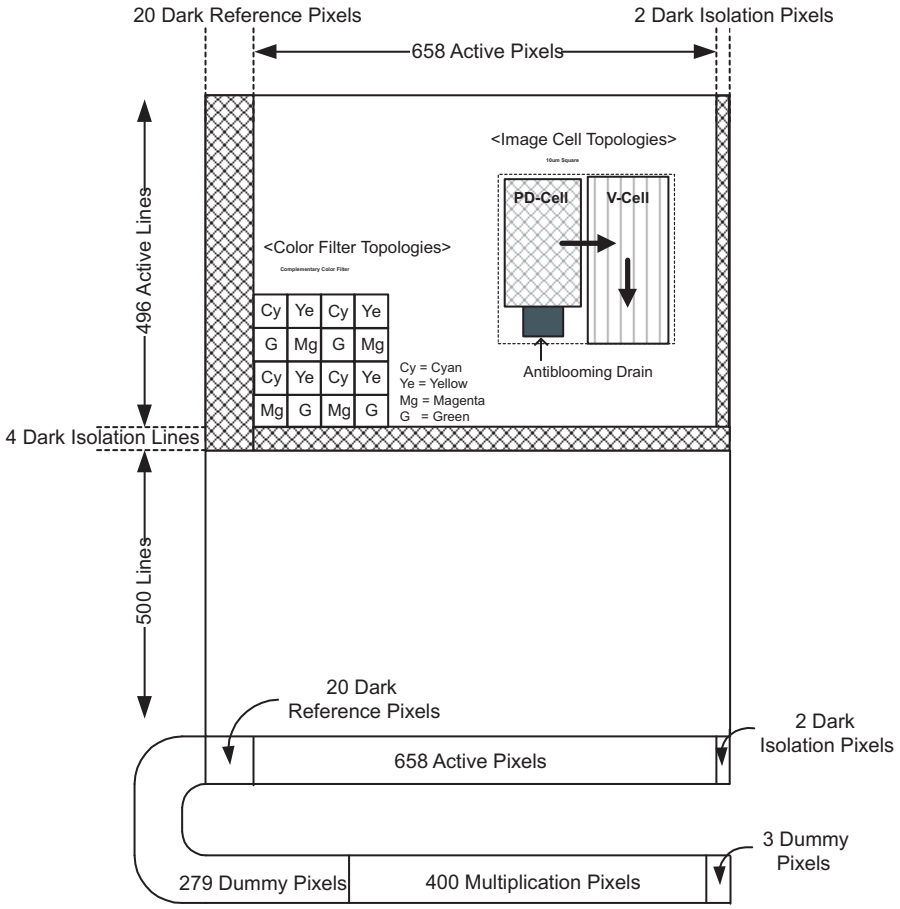


Sensor Topology Diagram - TC246RGB-B0



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Sensor Topology Diagram - TC246CYM-B0



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CMG	4	I	Charge multiplication gate
FP	11	-	Field plate (connect external capacitor)
IAG1	22	I	Image area gate 1
IAG2	21	I	Image area gate 2
NC	8	-	No connection
ODB	23	I	Supply voltage for anti-blooming drain
OUT	10	O	Output signal, multiplier channel
P(-)	17, 18	I	Peltier cooler negative power supply
P(+)	19, 20	I	Peltier cooler positive power supply
RST	5	I	Reset gate
SAG1	16	I	Storage area gate 1
SAG2	15	I	Storage area gate 2
SRG1	2	I	Serial register gate 1
SRG2	3	I	Serial register gate 2
SUB	1, 7, 12, 13, 24		Chip substrate
THER	6	I	Thermistor (NTC: negative temperature coefficient)
VCLD	14	I	Supply voltage for clearing drain and ESD protection circuits
VDD	9	I	Supply voltage for amplifiers

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DETAILED DESCRIPTION

The TC246 consists of five basic functional blocks: The image-sensing area, the image-storage area, the serial register, the charge multiplier, and the charge detection node with buffer amplifier. The location of each of these blocks is identified in the functional block diagram.

Image Sensing and Storage areas

As light enters the silicon in the image-sensing area, electrons are generated and collected in potential wells of the pixels. Color is accomplished by on-chip color mosaic filter. (see the sensor topology diagram for a mapping of the color filter) Applying a suitable DC bias to the antiblooming drain provides blooming protection. The electrons that exceed a specific level, determined by the ODB bias, are drained away from the pixels. After the integration cycle is completed by applying a PD-cell readout pulse to IAG2, charge is transferred from the PD-cell into the V-cell and then quickly transferred into the storage cell where it waits for readout. TC246CYM-B0 enables 2 lines to sum together to implement the pseudo-interlace scan.

Additionally, 4 dark lines, located between the image sensing area and the image-storage area, were added to the array for isolation.

Advanced Lateral Overflow Drain

Each pixel is constructed with the advanced lateral overflow drain structure. By varying the DC bias of the anti-blooming drain it is possible to control the blooming protection level and trade it for well capacity.

Electronic Exposure Control

Precise exposure control timing on a frame-by-frame basis is possible. The integration time can be arbitrarily shortened from its nominal length by clearing residual charge from the PD-cell. To do this, apply a PD-cell clear pulse to IAG2, which marks the beginning of integration.

Serial Register and Charge Multiplier

The serial register of TC246 image sensor consists of only poly-silicon gates. It operates at high speed, being clocked from 0 V to 8 V. This allows the sensor to work at 30 frames/s. The serial register is used for transporting charge stored in the pixels of the memory lines to the output amplifier. The TC246 device has a serial register with twice the standard length. The first half has a conventional design that interfaces with the memory as it would in any other CCD sensor. The second half, however, is unique and includes 400 charge multiplication stages with a number of dummy pixels that are needed to transport charge between the active register blocks and the output amplifier. Charge is multiplied as it progresses from stage to stage in the multiplier toward the charge detection node. The charge multiplication level depends on the amplitude of the multiplication pulses (approximately 15 V to 22 V) applied to the multiplication gate. Due to the double length of the register, first two lines in each field or frame scan do not contain valid data and should be discarded.

Charge Detection Node and Buffer Amplifier

The last element of the charge detection and readout chain is the charge detection node with the buffer amplifier. The charge detection node is using a standard Floating Diffusion (FD) concept followed by an on-chip, dual-stage, source-follower buffer. Applying a pulse to the RST pin resets the detection node. Pixel charge summing function can be easily implemented by skipping the RST pulses. To achieve the ultimate sensor performance it is necessary to eliminate kTC noise. This is typically accomplished by using CDS (correlated double sampling) processing techniques. IMPACTRON devices have the potential for detecting single electrons (photons) when cooled sufficiently.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

V_{SS}	Supply voltage range	VDD, VCLD(2)	0 V to 15 V
		ODB	0 V to 22 V
V_I	Input voltage range	IAG1, SAG1, SAG2	-10 V to 10 V
		IAG2	-10 V to 13 V
		SRG1, SRG2, RST	0 V to 10 V
		CMG	-5 V to 22 V
V_{cool}	Supply voltage range(3)	P+	0 V to 5.5 V
I_{cool}	Supply current range(3)	P+	0 A to 1.4 A
I_{th}	Supply current range	THER	0 mA to 0.31 mA
T_A	Operating free-air temperature range		-20°C to 75°C
T_{stg}	Storage temperature range		-30°C to 85°C
T_C	Operating case temperature range		-20°C to 75°C
	Dew point inside the package(3)		Lower than -20°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to substrate terminal.
(3) The peltier cooler generates heat during cooling process. Heat must be removed through an external heat sink. To avoid condensation upon the surface, do not cool the CCD to less than -20°C.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{SS}	Substrate bias				0		V
V_{DD}	Supply voltage	VDD		13.5	14	14.5	V
		VCLD		13.5	14	14.5	
		ODB (1)		4.5		6.5	
V_I	Input voltage	IAG1	High	3	3.3	3.6	V
			Low	-5.8	-5.5	-5.2	
		IAG2	High	9.5	10	10.5	
			Mid	3	3.3	3.6	
			Low	-5.8	-5.5	-5.2	
		SAG1	High	3	3.3	3.6	
			Low	-5.8	-5.5	-5.2	
		SAG2	High	3	3.3	3.6	
			Low	-5.8	-5.5	-5.2	
		SRG1	High	7.5	8	8.5	
			Low		0		
		SRG2	High	7.5	8	8.5	
			Low		0		
		CMG (2)	High	7		22	
			Low	-3	-2.5	-2	
		RST	High	5.5	6	6.5	
			Low		0		
f_{CLK}	Clock frequency	SAG1, SAG2			1.5		MHz
		IAG1, IAG2			1.5		
		SRG1, SRG2, RST			12.5	25	
		CMG			12.5	25	
	Load capacitance	OUT				6	
	Dew point inside the package (3)					-20	°C
T_A	Operating free-air temperature			-20	25	55	°C

(1) Adjustment within the specified MIN/MAX range is required to optimize performance.
(2) Charge multiplication gain depends on high level of the CMG and temperature.
(3) -20°C should be the minimum temperature of the cooled CCD.

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ELECTRICAL CHARACTERISTICS

T_A = 25°C, integration time = 16.67 ms (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Charge multiplication gain		1	100		
Excess noise factor for typical CCM gain(1)		1	1.4		
Dynamic range without CCM gain			63		dB
Dynamic range with typical CCM gain (2)			75		dB
Charge conversion gain without CCM gain(3)			14		µV/e
Signal-response delay time(4)			16		ns
Output resistance			320		Ω
Amplifier noise-equivalent signal without CCM gain(5)			20		e
Amplifier noise-equivalent signal with typical CCM gain(5)			1		e
Response linearity with no CCM gain			1		
Response linearity with typical CCM gain			1		
Charge-transfer efficiency(6)	Parallel transfer	0.99994		1	
	Serial transfer	0.99994		1	
Supply current			2		mA
Input capacitance	IAG1		3		nF
	IAG2		7		
	IAG1, IAG2		3		
	SAG1		4		
	SAG2		5		
	SAG1, SAG2		3		
	SRG1		85		pF
	SRG2		55		
	CMG		25		
	ODB		2000		
	RST		7		

(1) Excess noise factor "F" is defined as the ratio of noise sigma after multiplication divided by M times the noise sigma before multiplication where M is the charge multiplication gain.
(2) Dynamic range is -20 times the logarithm of the noise sigma divided by the saturation-output signal amplitude
(3) Charge conversion factor is defined as the ratio of output signal to input number of electrons.
(4) Signal-response delay time is the time between the falling edge of the SRG1 pulse and the output-signal valid state.
(5) The values in the table are quoted using correlated double sampling (CDS). CDS is a signal processing technique that improves performance by minimizing undesirable effects of reset noise.
(6) Charge transfer efficiency is one minus the charge loss per transfer in the CCD register. The test is performed in the dark using either electrical or optical input.

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OPTICAL CHARACTERISTICS

T_A = 25°C, integration time = 16.67 ms (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Sensitivity(1) RGB Type TC246RGB-B0 Progressive scan operation	With typical CCM gain	Without IR-cut filter	Red		2700		V/lx sec
			Green		1700		
			Blue		1300		
		With IR-cut filter	Red		150		
			Green		200		
			Blue		110		
	Without CCM gain	Without IR-cut filter	Red		27		
			Green		17		
			Blue		13		
		With IR-cut filter	Red		1.5		
			Green		2		
			Blue		1.1		
Sensitivity(1) CYM Type TC246CYM-B0 Progressive scan operation	With typical CCM gain	Without IR-cut filter	Cyan		2420		V/lx sec
			Yellow		3735		
			Magenta		3195		
			Green		2100		
		With IR-cut filter	Cyan		280		
			Yellow		475		
			Magenta		275		
			Green		240		
	Without CCM gain	Without IR-cut filter	Cyan		24		
			Yellow		37		
			Magenta		32		
			Green		21		
		With IR-cut filter	Cyan		2.8		
			Yellow		4.8		
			Magenta		2.7		
			Green		2.4		
		No CCM gain			400		
Saturation signal output(2)	Anti blooming enabled, no CCM gain				180		mV
	With typical CCM gain				1500		
Zero input offset output(3)					100		mV
Blooming overload ratio(4)					500:1		
Image area well capacity					28k		e
Smear(5)					-84		dB
Dark current(6)					0.01		nA/cm^2
Dark signal(7)					0.01		mV

(1) Light source temperature is 2856 °K. The IR filter used is CM500 1 mm thick.
(2) Saturation is the condition in which further increase in exposure does not lead to further increases in output signal.
(3) Zero input offset is the residual output signal measured from the reset level with no input charge present. This level is not caused by the dark current and remains approximately constant independent of temperature. It may vary with the amplitude of SRG1.
(4) Blooming is the condition in which charge induced by light in one element spills over to the neighboring elements.
(5) Smear is the measure of error signal introduced into the pixels by transferring them through the illuminated region into the memory. The illuminated region is 1/10 of the image area height. The value in the table is obtained for the integration time of 33.3 ms and 1.5 MHz vertical clock transfer frequency.
(6) Dark current depends on temperature and approximately doubles every 8 Co. Dark current is also multiplied by CCM operation. The value given in the table is with the multiplier turned off and it is a calculated value.
(7) Dark signal is actual device output measured in dark.

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OPTICAL CHARACTERISTICS (continued)

T_A = 25°C, integration time = 16.67 ms (unless otherwise noted)

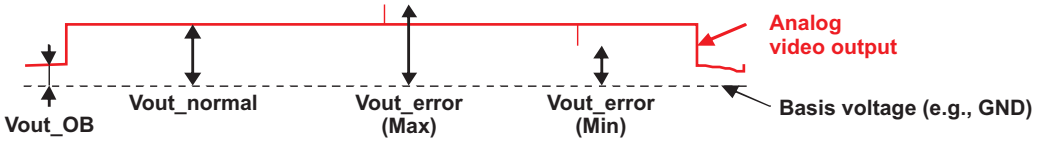
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Column uniformity(8)					2	%
Electronic-shutter capability			1/2000	1/30		s
Defect(9)	Dark (zone A) (see Figure 1), -15°C, CCM gain 100	Exceed 20mV			0	dot
		12mV to 20mV			10	
	Illuminated (zone A) (see Figure 1), 25°C, 100-mV output		-20		20	%
Vertical belt noise(10)	-15°C, CCM gain 1000				6	mV
Horizontal streaking(11)	-15°C, CCM gain 1000				70	mV

(8) Column uniformity is obtain by summing all the lines in the array, finding the maximum of the difference of two neighboring columns anywhere in the array, and dividing the result by the number of lines.
(9) There shall be no pixel defect which continued horizontally.
(10) Vertical belt noise is dark current from CMG stage, when CCD generates CMG 1000 times with -15°C at thermistor. When 0 digress, this value is multiplied by about 2.5 times. These values are under the condition of non-aging test when factory out.
(11) Streaking is a phenomenon that pixel in the right of blight pixels which are generated by huge light intensity source responses blighter data, when CCD generates CMG 1000 times with -15°C at thermistor. When 0°C, this value is multiplied by about 0.8 times. These values are under the condition of non-aging test when factory out.

How to Check Pixel Error Under Blight Condition

This value is calculated using Equation 1:

$$\text{error}(\%) = \frac{|\text{Vout_normal} - \text{Vout_error}| - \text{Vout_OB}}{\text{Vout_normal} - \text{Vout_OB}} \times 100 \quad (1)$$



Vout_xx means analog video output voltage (mV) at the several pixels. Vout_error is at error pixel, Vout_normal is at non-error pixel, and Vout_OB is at Optical Black pixel. This test is done when CCD receives white light whose intensity becomes about 60mV video data value at non-error pixel, which is calculated by (Vout_normal - Vout_OB).

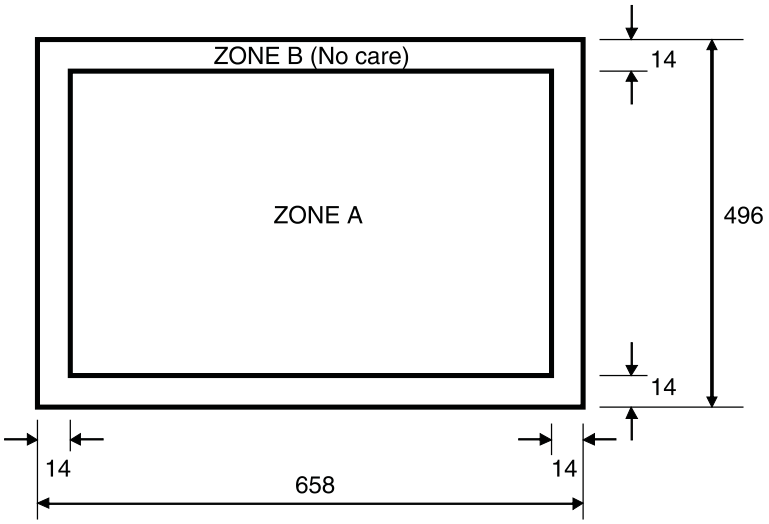
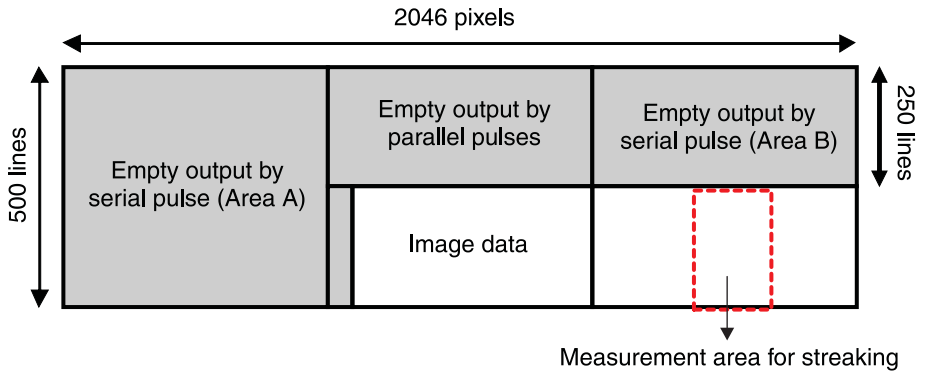


Figure 1. Defect Area

How to Measure Streaking Value

Driving timing:

1. The electron in V-cell is cleared by 750 lines (1.5 times normal operation) vertical transferring from V-cell to storage area.
2. The electron in PD-cell is moved to V-cell.
3. The electron in 250 V-cell is moved to storage area by 250 parallel pulses (0.5 times as normal operation).
4. The electron in the last line of storage area is moved to serial resister.
5. The electron in serial resister is moved out by 2046 serial pulses (3 times as normal operation).
6. All the electrons in storage area are moved out by repeated 500 times both (4) and (5). Then the following image is out.



Measurement condition:

CMG: 1000 times

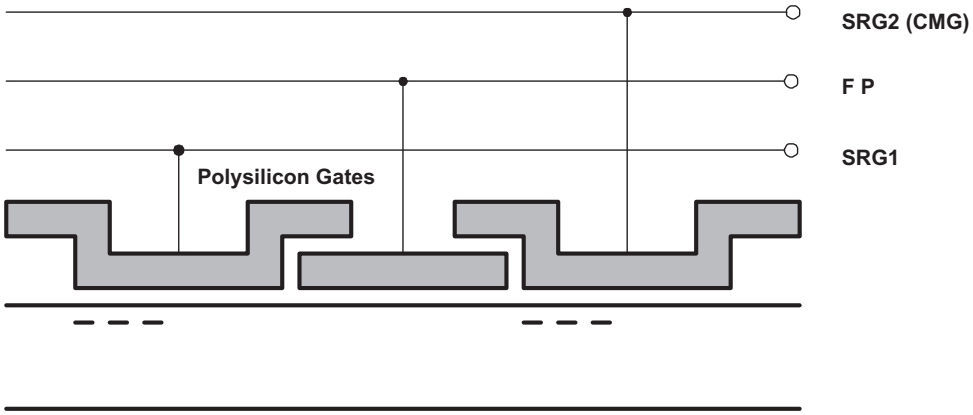
Thermistor temperature: -15°C

Light intensity: 10 Lx

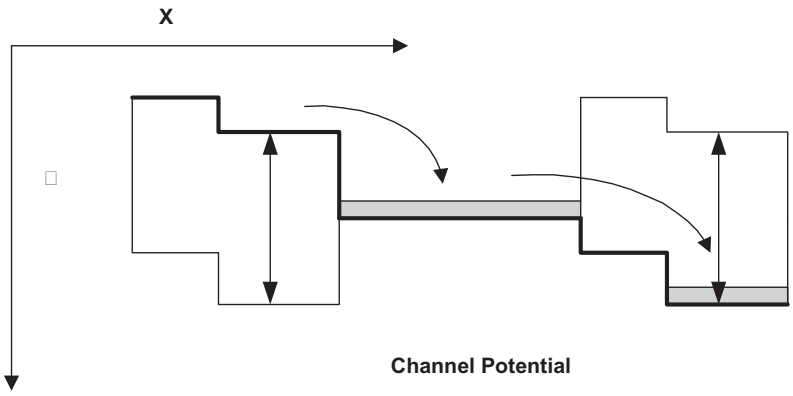
Calculation:

The value of streaking is difference between the average of the electron in streaking area and the one in area B.

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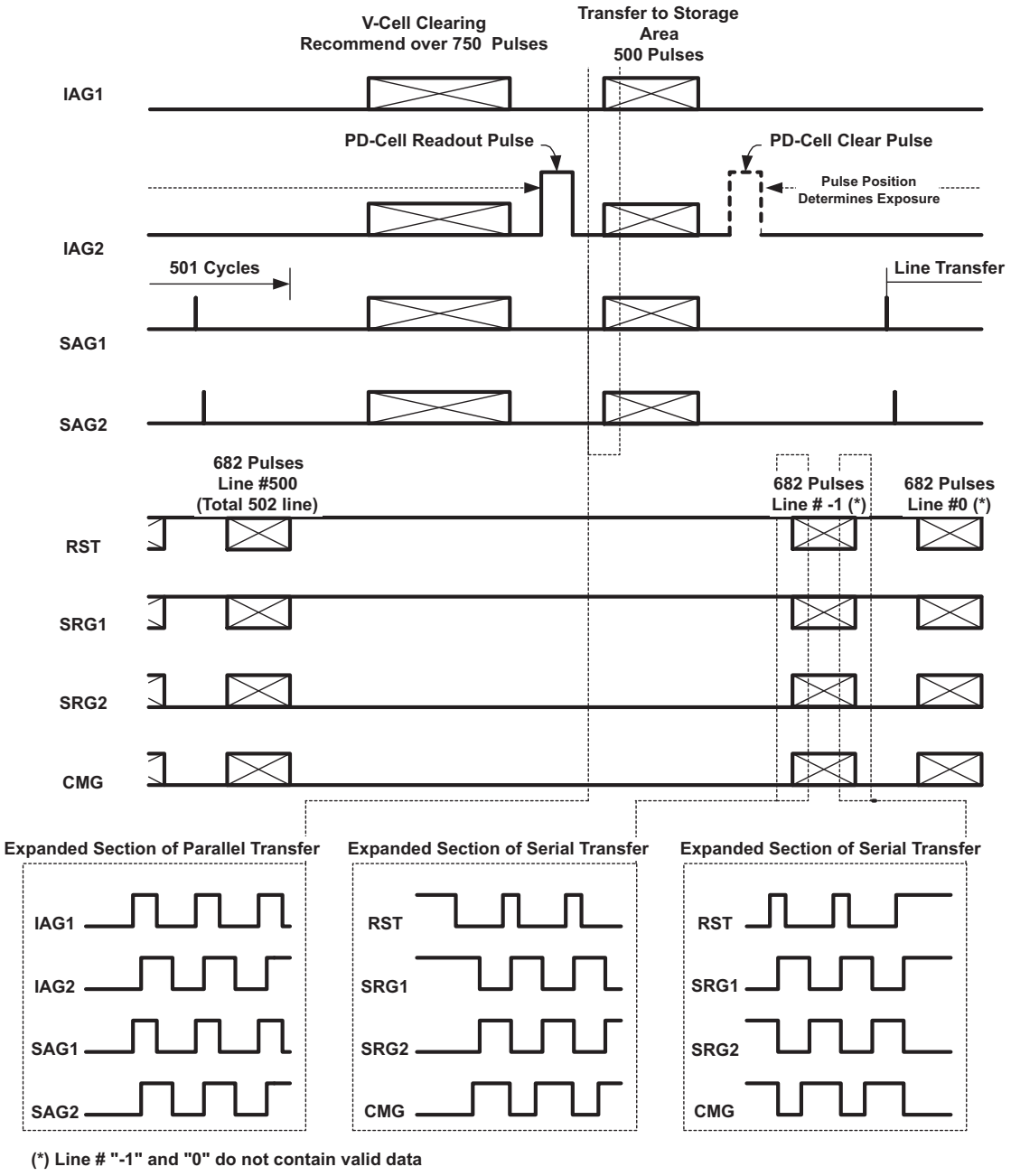


Pixel Cross Section



Channel Potential

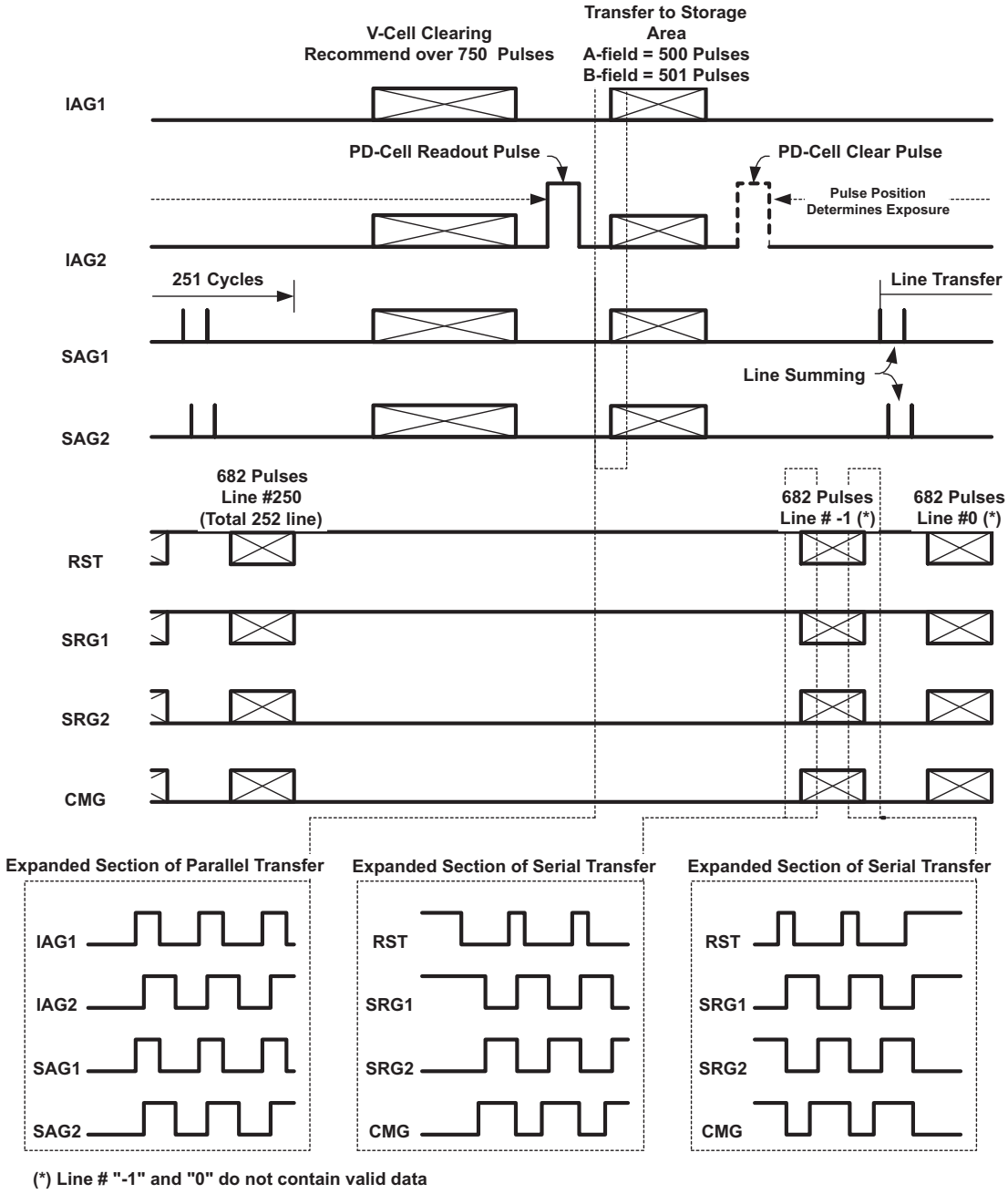
Figure 2. Serial Register Pixel Cross-Section



(*) Line # "-1" and "0" do not contain valid data

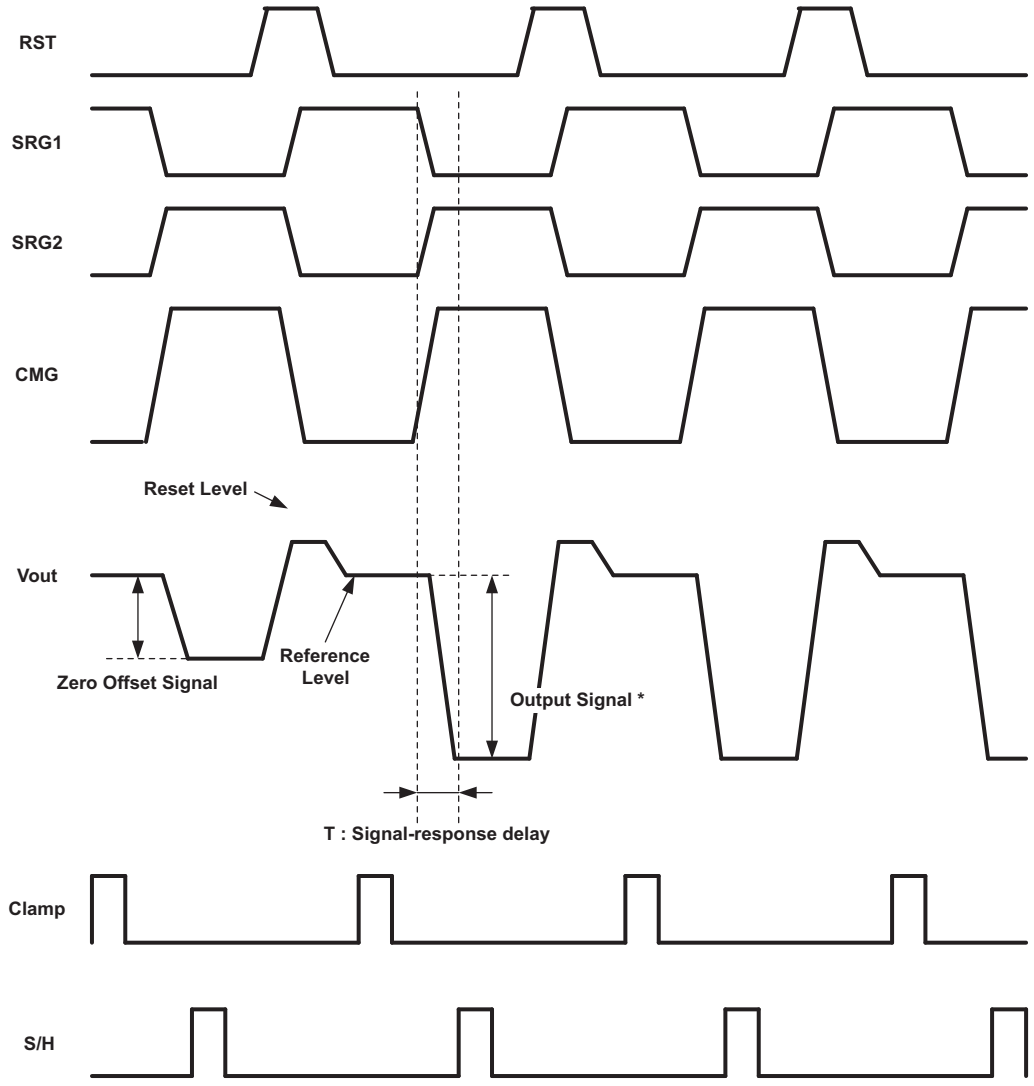
Figure 3. Progressive Scan Timing

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(*) Line # "-1" and "0" do not contain valid data

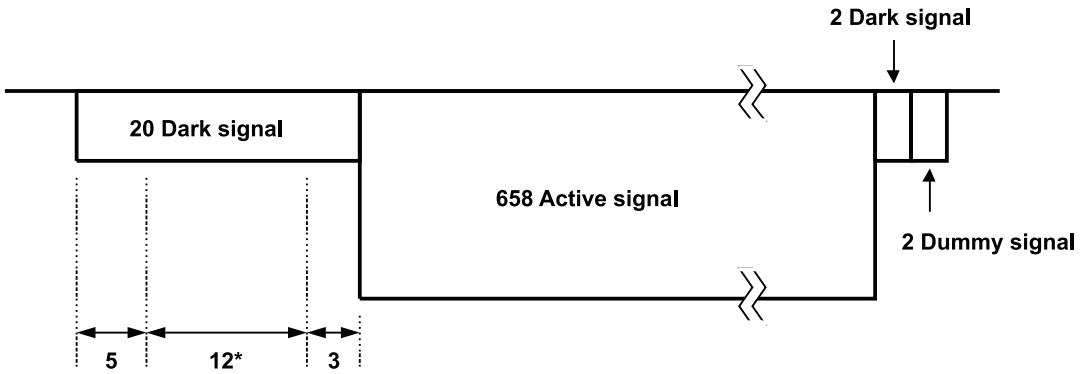
Figure 4. Interlace Timing of Line Summing Mode



* Output signal may not be zero for zero input charge.

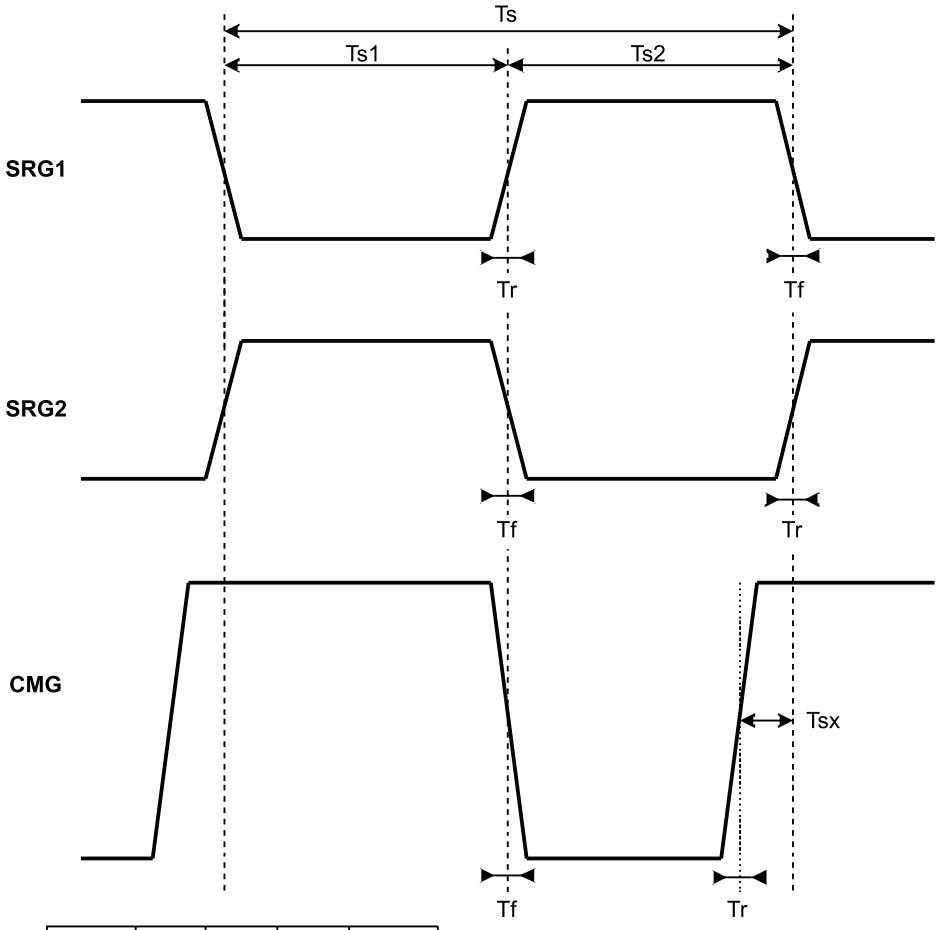
Figure 5. Serial Register Clock Timing for CDS Implementation

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* Due to light leakage into the edge pixels of the 20 dark reference pixels it is recommended that these 12 pixels be used for true dark reference.

Figure 6. Detailed Output Signal



	MIN	TYP	MAX	UNIT
Ts	75	80	85	ns
Ts1	35	40	45	
Ts2	35	40	45	
Tsx		8		

		MIN	MAX	UNIT
Tr	CMG	3	8	ns
	SRG1	3	8	
	SRG2	3	8	
Tf	CMG	3	8	
	SRG1	3	8	
	SRG2	3	8	

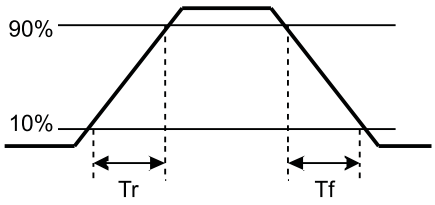
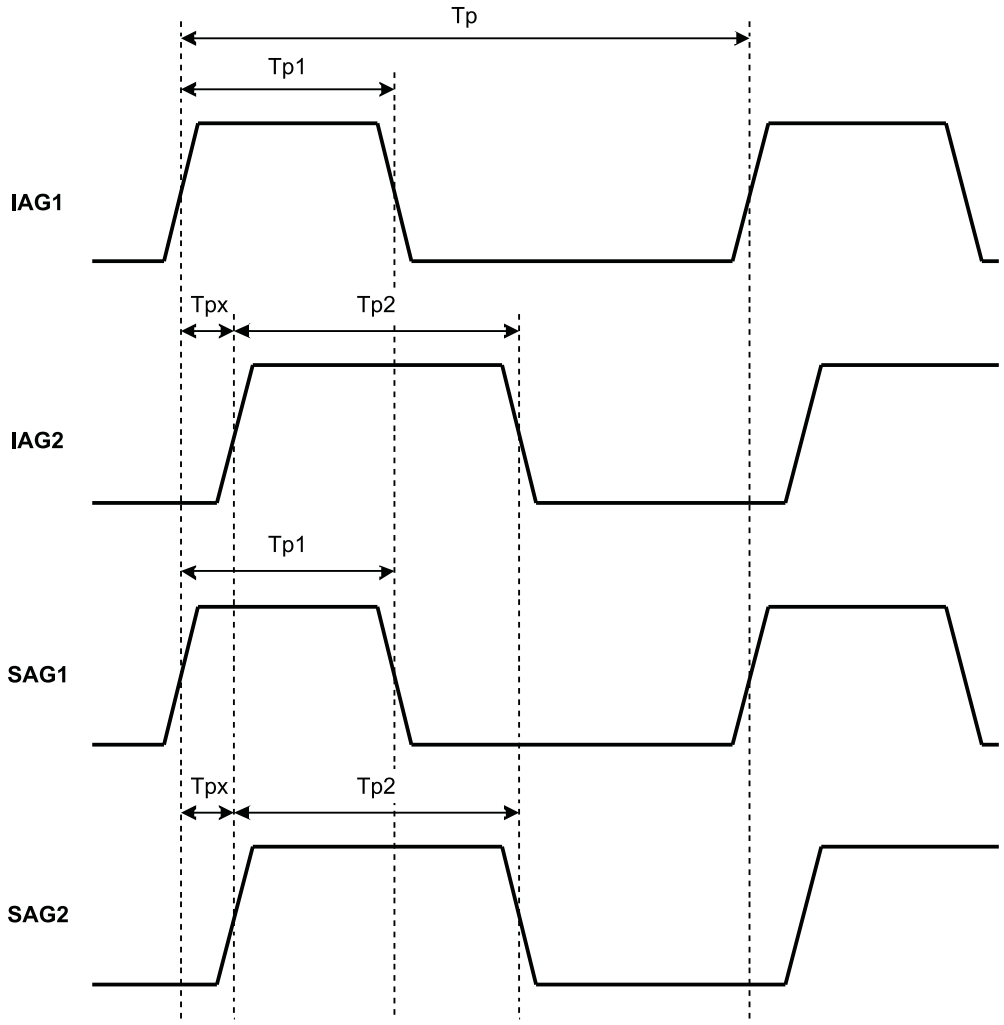


Figure 7. Serial Transfer Timing (12.5 MHz Applications)

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	MIN	TYP	MAX	UNIT
Tp		664		ns
Tp1	230	260	290	
Tp2	300	330	360	
Tpx	40	50	60	

		MIN	MAX	UNIT
Tr	IAG1,2	15	25	ns
	SAG1,2	15	25	
Tf	IAG1,2	15	25	
	SAG1,2	15	25	

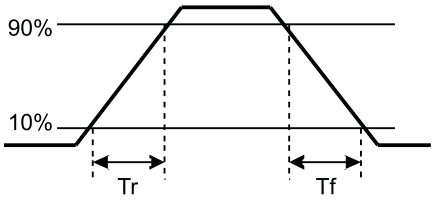
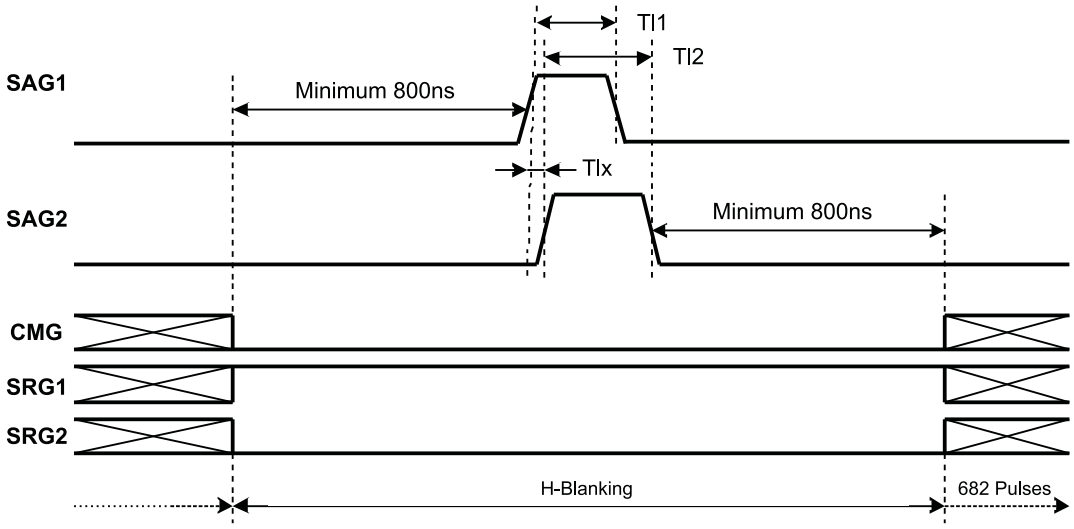


Figure 8. Vertical Transfer Timing (1.5 MHz Application)

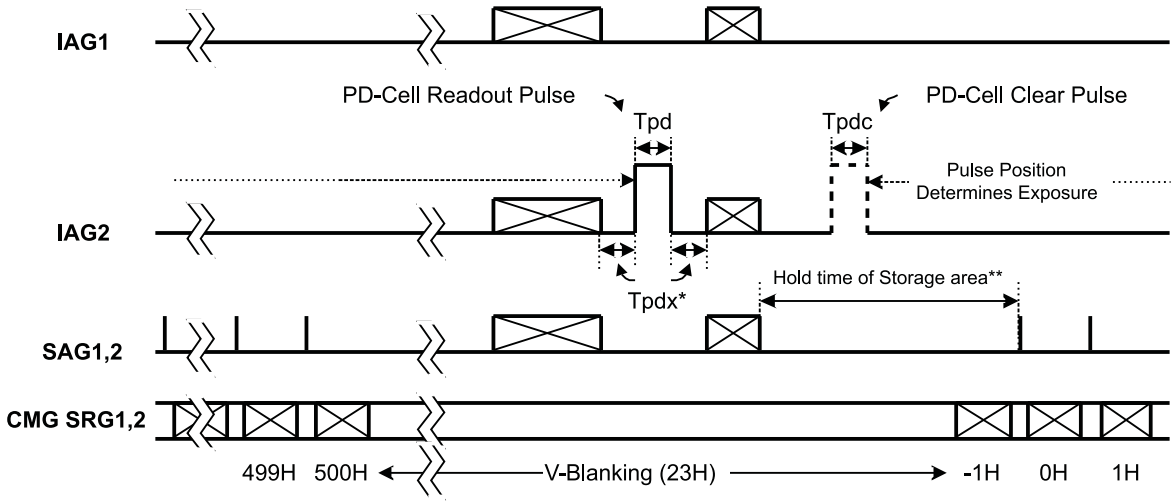
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	MIN	TYP	MAX	UNIT
TI1*	230	260	290	ns
TI2*	300	330	360	
TIx*	40	50	60	

* Line Transfer Timing : Same timing as 1.5MHz vertical transfer

Figure 9. Typical Line Transfer Timing



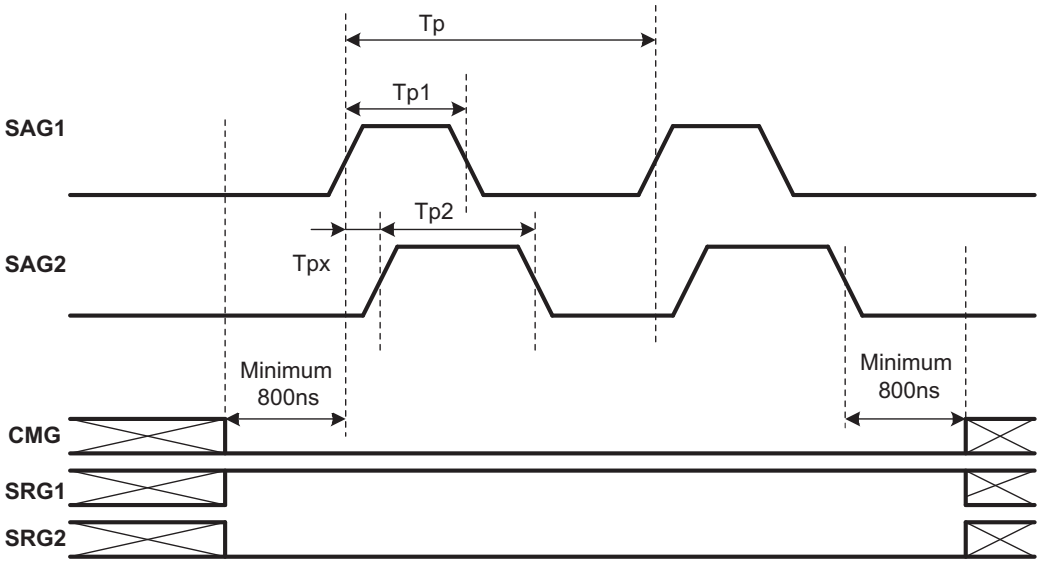
	MIN	TYP	MAX	UNIT
Tpd	1.0	1.5	2.0	us
Tpdc	1.0	1.5	2.0	
Tpdx*		1.0		

		MIN	MAX	UNIT
Tr	Tpd,Tpdc	250	1000	ns
Tf	Tpd,Tpdc	100	1000	

* Tpdx : as shorter as possible
** Hold time of Storage area : Recommend shorter than 300usec

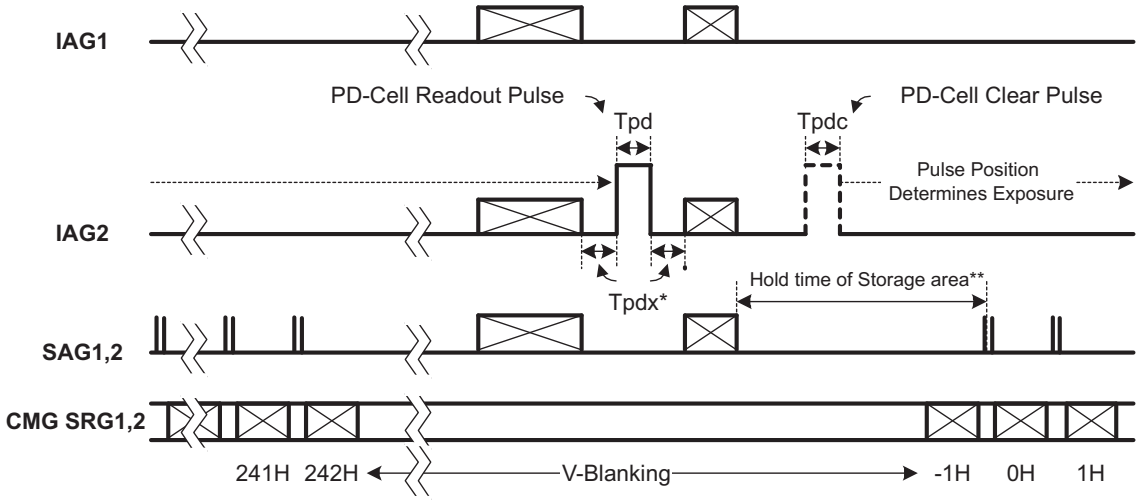
Figure 10. Typical PD-Readout and Exposure Control Timing

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	MIN	TYP	MAX	UNIT
Tp*		667		ns
Tp1*	230	260	290	
TI2*	300	330	390	
Tpx*	40	50	60	

Figure 11. Typical Line Summing and Transfer Timing (1.5-MHz Application)



	MIN	TYP	MAX	UNIT
Tpd	1.0	1.5	2.0	us
Tpdc	1.0	1.5	2.0	
Tpdx*		1.0		

		MIN	MAX	UNIT
Tr	Tpd,Tpdc	250	1000	ns
Tf	Tpd,Tpdc	100	1000	

* Tpdx : as shorter as possible
** Hold time of Storage area : Recommend shorter than 300usec

Figure 12. Typical PD-Readout and Exposure Control Timing

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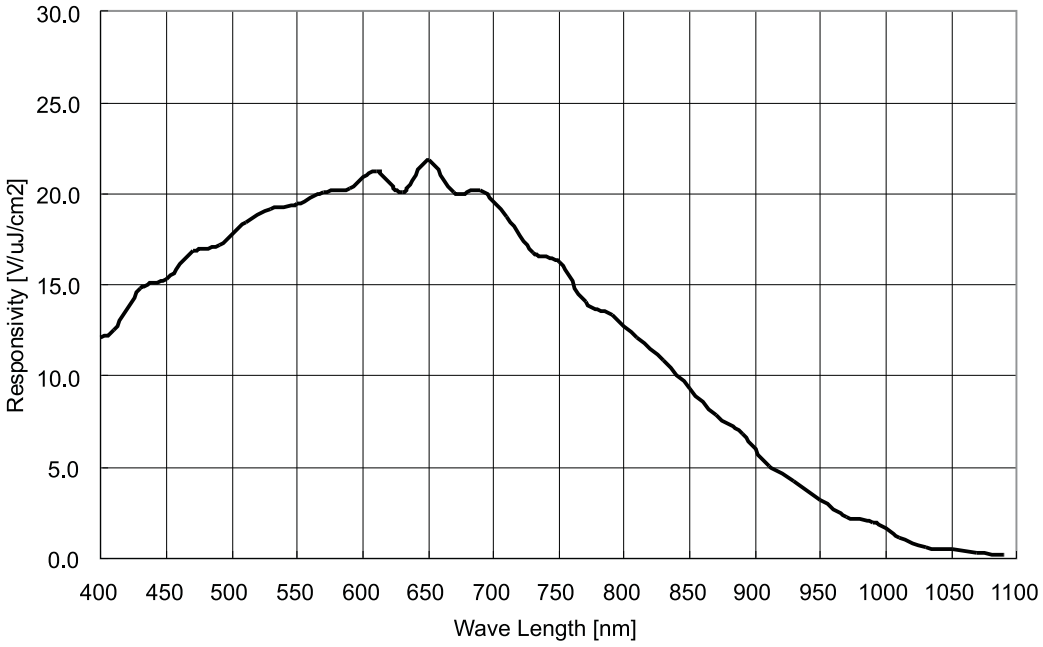


Figure 13. Typical Spectral Responsivity (Without On-Chip Color Filter)

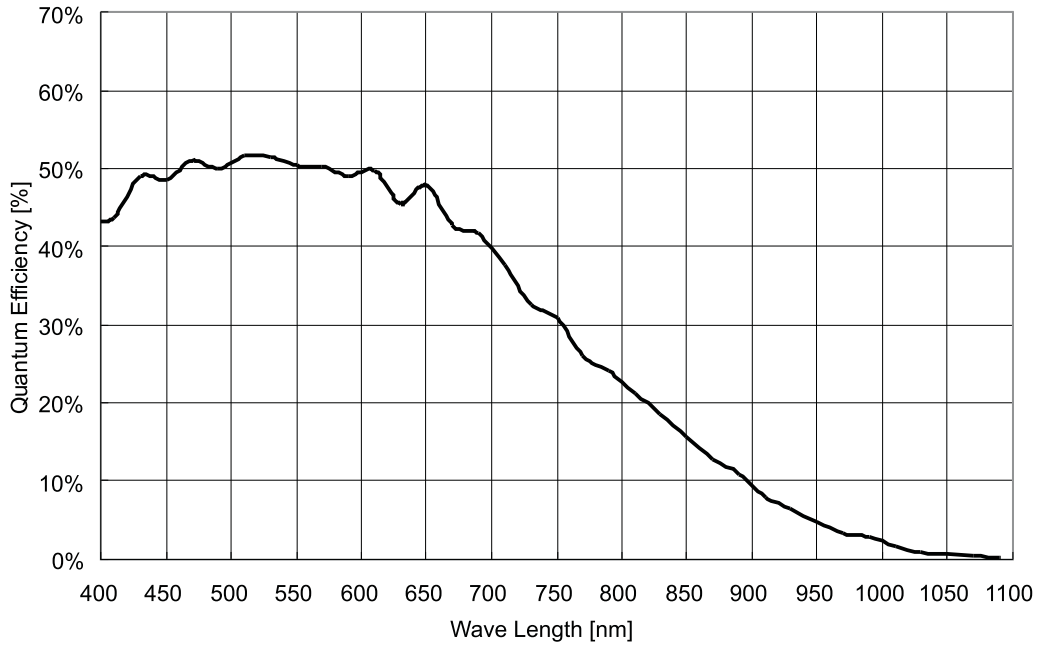


Figure 14. Typical Spectral Quantum Efficiency (Without On-Chip Color Filter)

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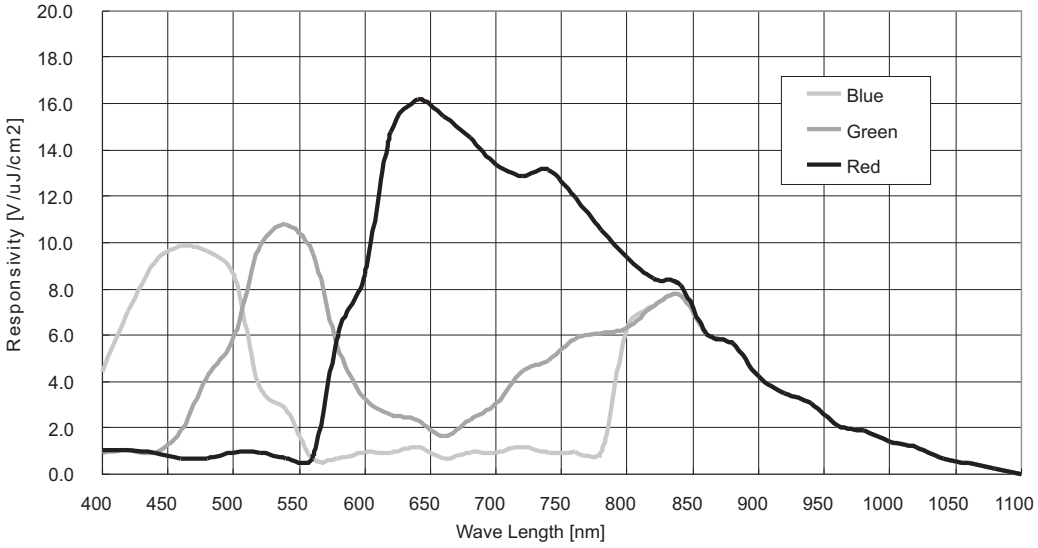


Figure 15. TC246RGB-B0 Typical Spectral Quantum Efficiency

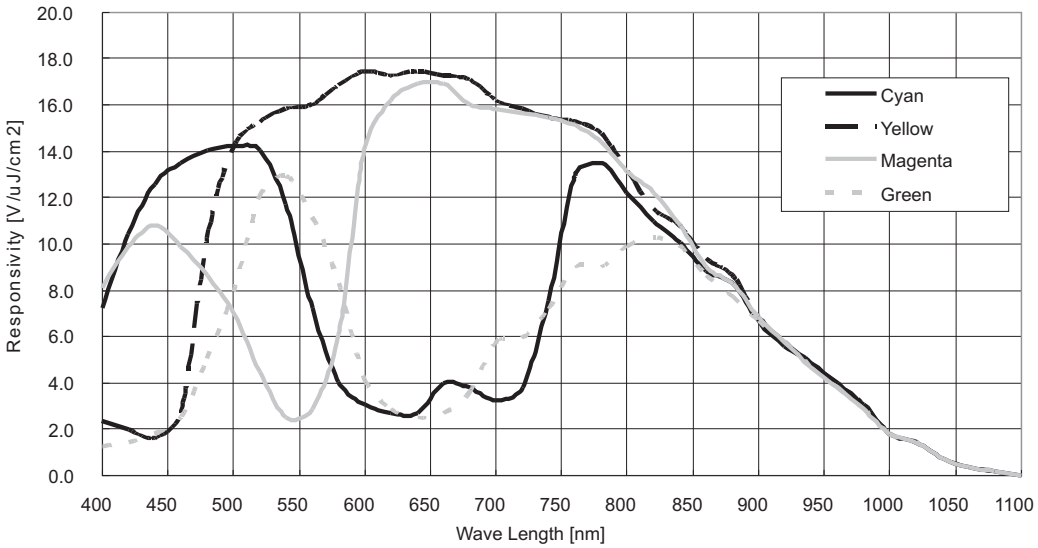


Figure 16. TC246CYM-B0 Typical Spectral Quantum Efficiency

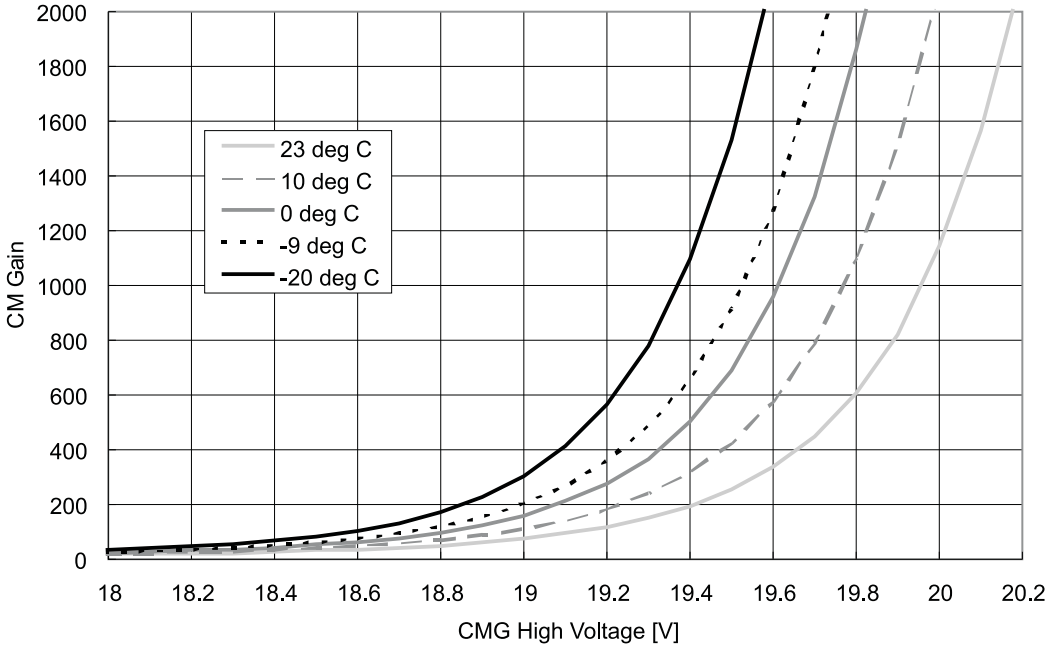


Figure 17. Typical Variation of Multiplication Gain with CMG High Voltage

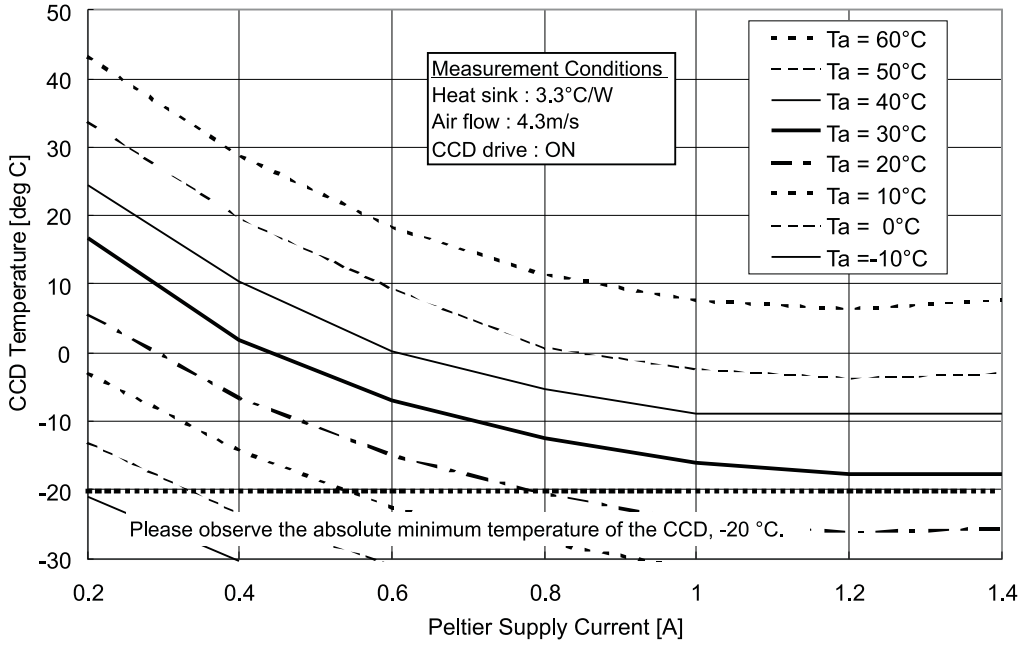


Figure 18. Typical Cooling Capability

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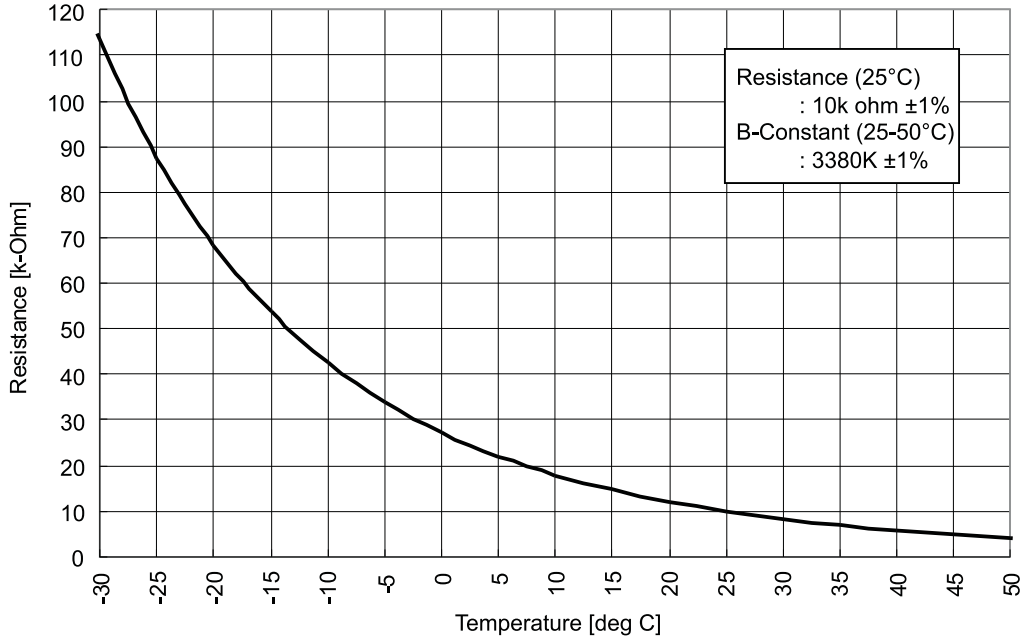


Figure 19. Typical Thermistor Characteristics

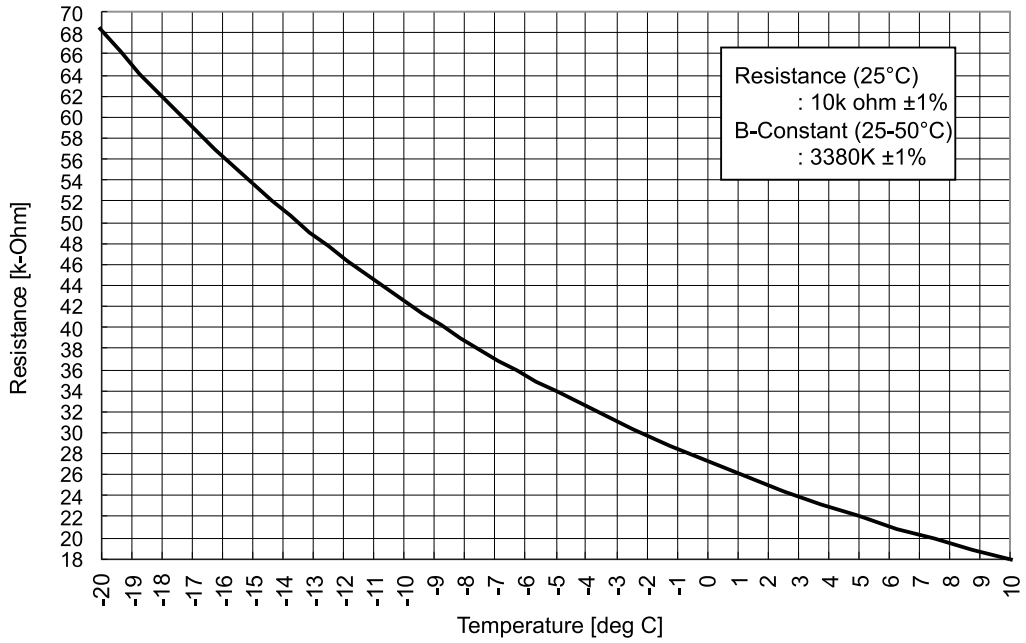


Figure 20. Typical Thermistor Characteristics (Detail)

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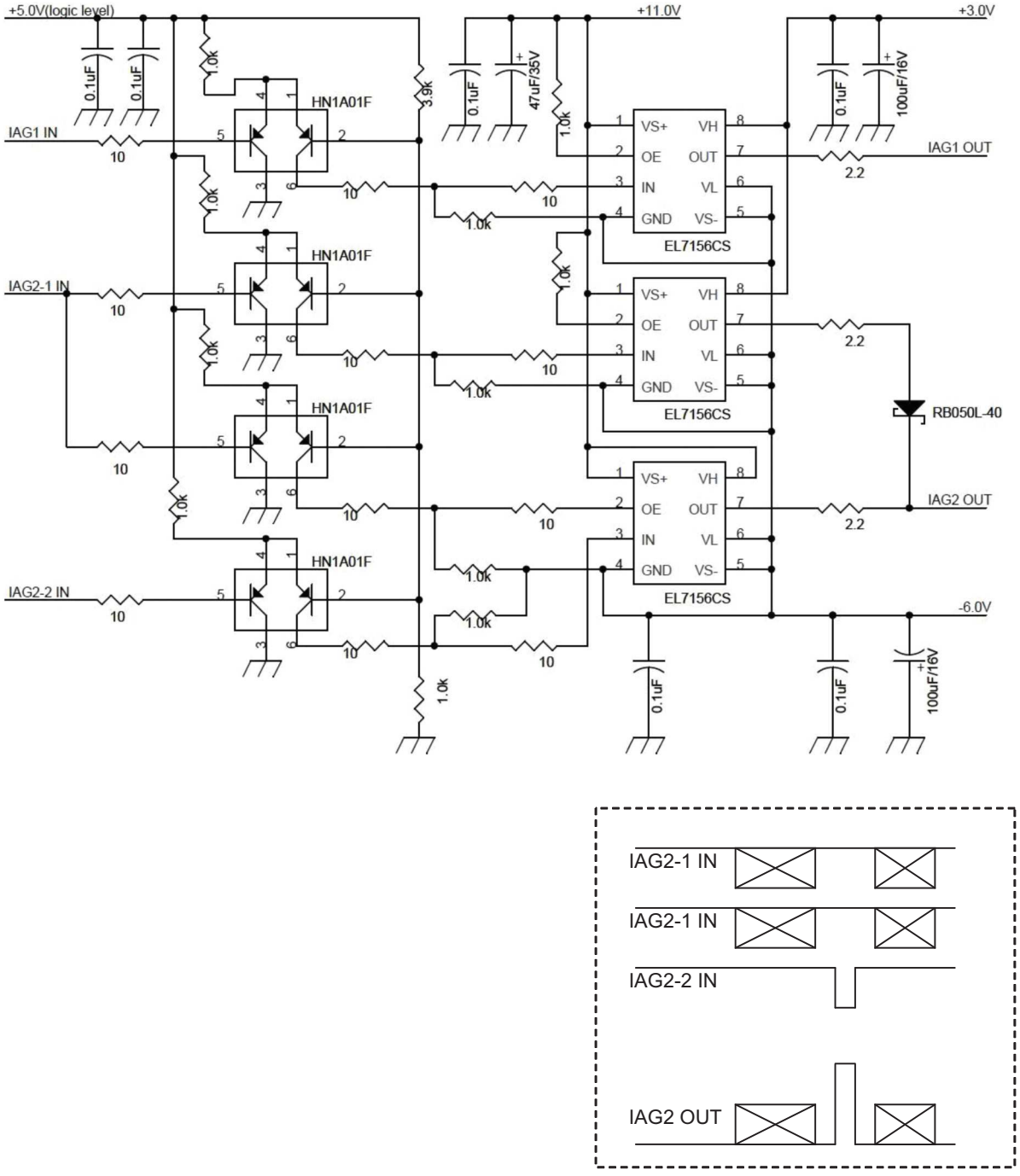


Figure 21. Typical IAG Driver Circuits

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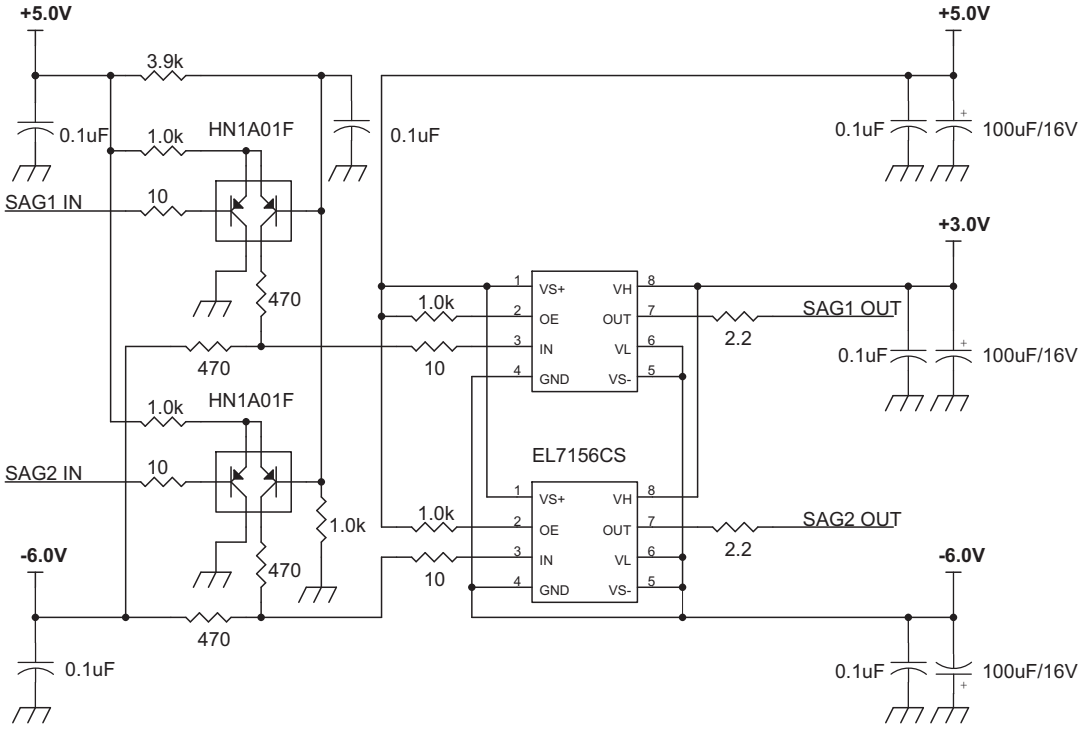


Figure 22. Typical SAG Driver Circuits

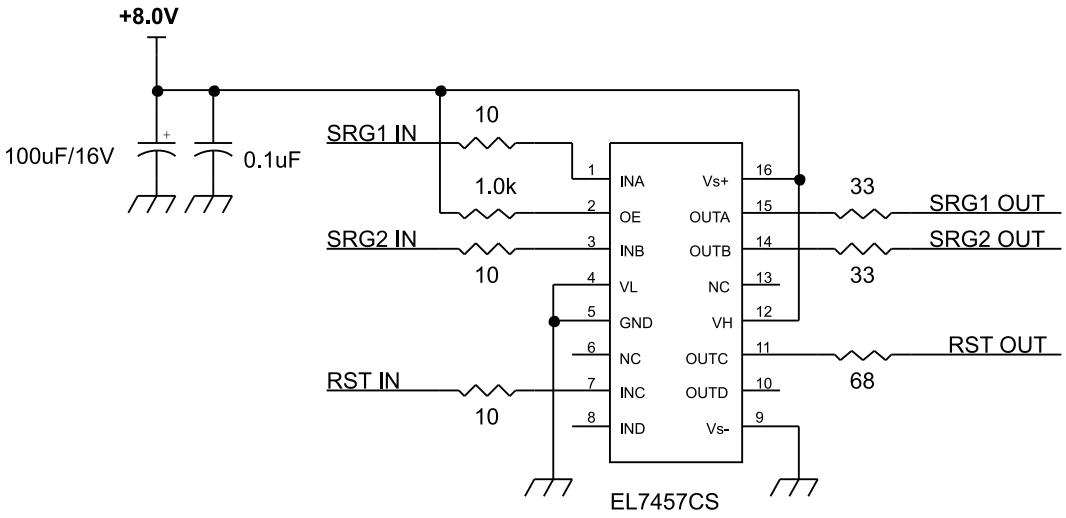


Figure 23. Typical SRG and RST Driver Circuits

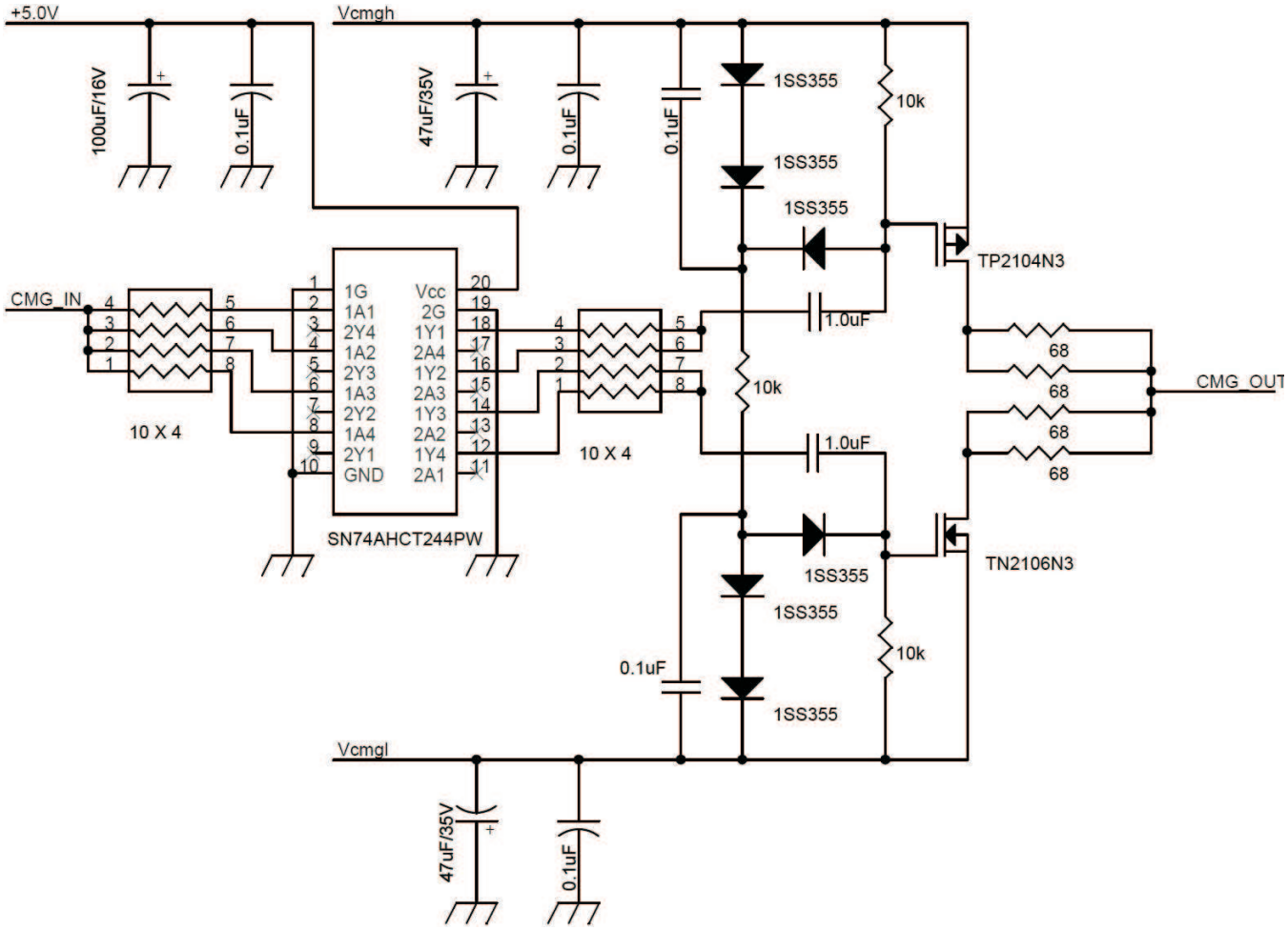


Figure 24. Typical CMG Driver Circuits

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Mechanical Data

The package for the TC246 consists of a ceramic base, a glass window, and a 24-pin lead frame. The glass window is hermetically sealed to the package. The package leads are configured in a dual-in-line arrangement and fit into mounting holes with 1,78 mm center-to-center spacing.

CAUTION

The TC246 glass window is very weak for the mechanical internal stress. Be careful when attaching an external heat sink to the package. Fastening it too strongly may crack or puncture the package, making it susceptible to moisture or humidity.

Recommended conditions are:

1. Torque control for the screw (M1.6 micro screw) should be under 0.5 kgf*cm.
2. Paste "Lock Tight" on the screw. Recommendation is Three Bond 1401B.
3. As for the soldering condition, do not exceed 80ºC for the package temperature. Since a reflow or solder dip may cause glass lid crack or fracture, the grounded soldering iron shall be used and the operation shall be less than 2 seconds per pin.

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