# CY7C1166KV18, CY7C1177KV18
# CY7C1168KV18, CY7C1170KV18

# 18-Mbit DDR II+ SRAM Two-Word Burst Architecture (2.5 Cycle Read Latency)

## Features

- 18 Mbit density (2 M x 8, 2 M x 9, 1 M x 18, 512 K x 36)
- 550-MHz clock for high bandwidth
- Two-word burst for reducing address bus frequency
- Double data rate (DDR) interfaces (data transferred at 1100 MHz) at 550 MHz
- Available in 2.5 clock cycle latency
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high-speed systems
- Data valid pin (QVLD) to indicate valid data on the output
- Synchronous internally self-timed writes
- DDR II+ operates with 2.5 cycle read latency when $\overline{DOFF}$ is asserted HIGH
- Operates similar to DDR I device with one cycle read latency when $\overline{DOFF}$ is asserted LOW
- Core $V_{DD}$ = 1.8 V ± 0.1 V; I/O $V_{DDQ}$ = 1.4 V to $V_{DD}$[1]
  - Supports both 1.5 V and 1.8 V I/O supply
- HSTL inputs and variable drive HSTL output buffers
- Available in 165-Ball FBGA package (13 x 15 x 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- JTAG 1149.1 compatible test access port
- Phase-locked loop (PLL) for accurate data placement

## Configurations

***With Read Cycle Latency of 2.5 cycles:***

CY7C1166KV18 – 2 M x 8

CY7C1177KV18 – 2 M x 9

CY7C1168KV18 – 1 M x 18

CY7C1170KV18 – 512 K x 36

## Functional Description

The CY7C1166KV18, CY7C1177KV18, CY7C1168KV18, and CY7C1170KV18 are 1.8 V synchronous pipelined SRAMs equipped with DDR II+ architecture. The DDR II+ consists of an SRAM core with advanced synchronous peripheral circuitry. Addresses for read and write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and $\overline{K}$. Read data is driven on the rising edges of K and $\overline{K}$. Each address location is associated with two 8-bit words (CY7C1166KV18), 9-bit words (CY7C1177KV18), 18-bit words (CY7C1168KV18), or 36-bit words (CY7C1170KV18) that burst sequentially into or out of the device.

Asynchronous inputs include an output impedance matching input (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs D) are tightly matched to the two output echo clocks CQ/$\overline{CQ}$, eliminating the need for separately capturing data from each individual DDR SRAM in the system design.

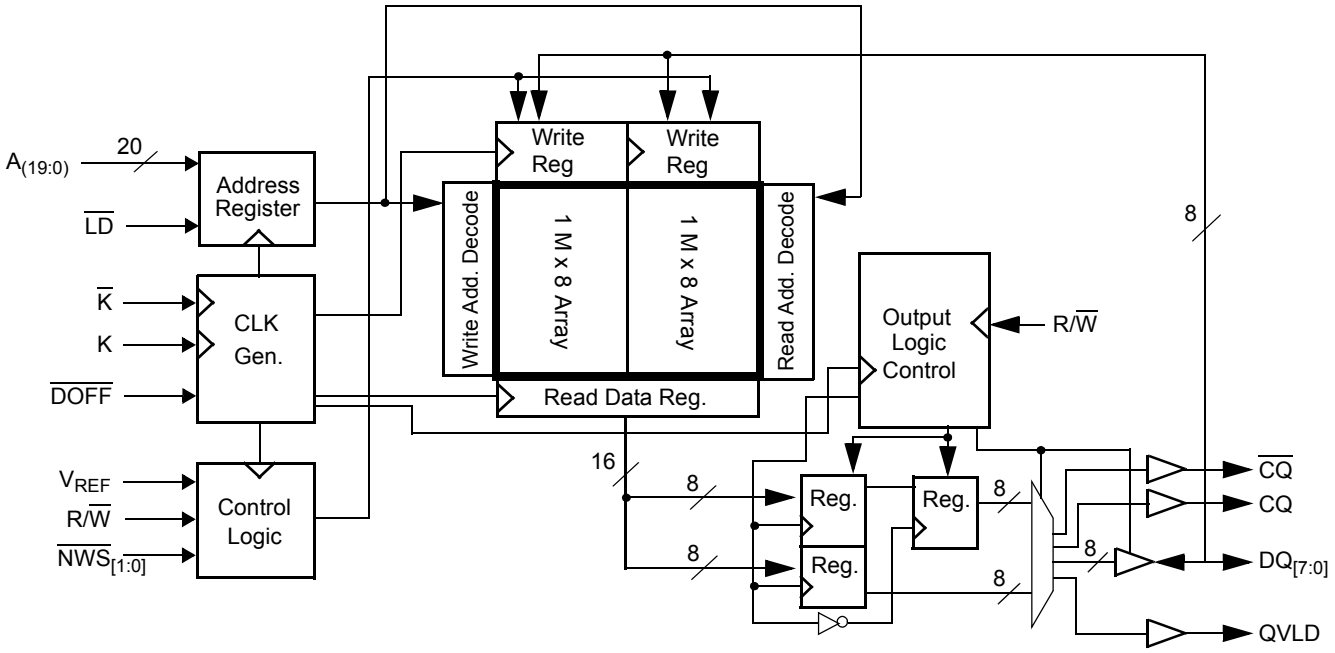
All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the K or $\overline{K}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

**Table 1. Selection Guide**

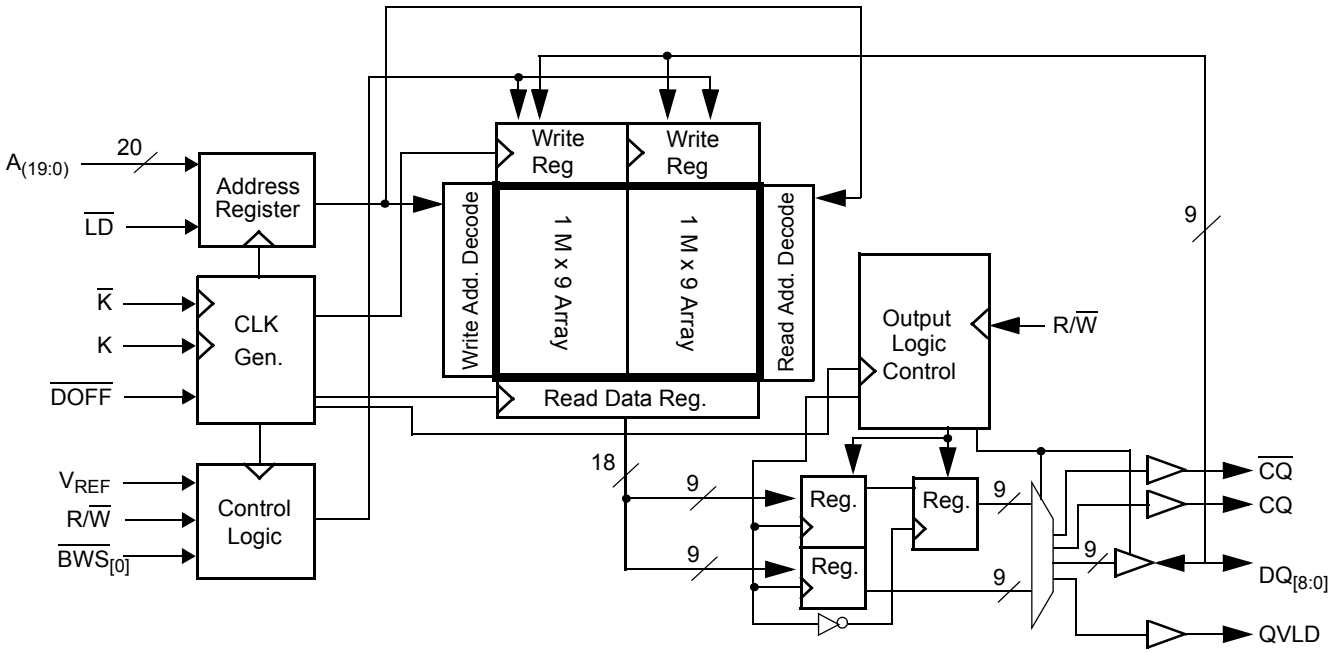
| Description | | 550 MHz | 500 MHz | 450 MHz | 400 MHz | Unit |
|---|---|---|---|---|---|---|
| Maximum operating frequency | | 550 | 500 | 450 | 400 | MHz |
| Maximum operating current | x8 | 630 | 590 | 550 | 500 | mA |
| | x9 | 630 | 590 | 550 | 500 | |
| | x18 | 650 | 600 | 560 | 510 | |
| | x36 | 820 | 760 | 700 | 640 | |

**Note**
1. The Cypress QDR II+ devices surpass the QDR consortium specification and can support $V_{DDQ}$ = 1.4 V to $V_{DD}$.

## Logic Block Diagram (CY7C1166KV18)



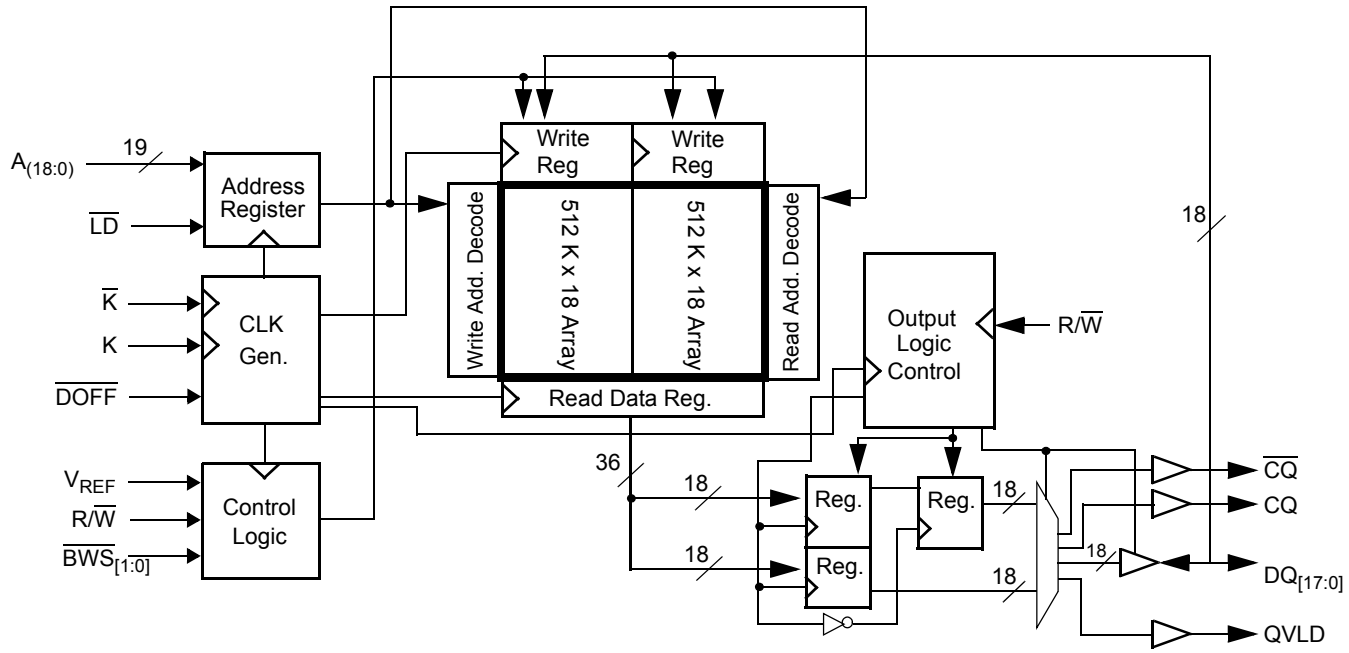

## Logic Block Diagram (CY7C1177KV18)



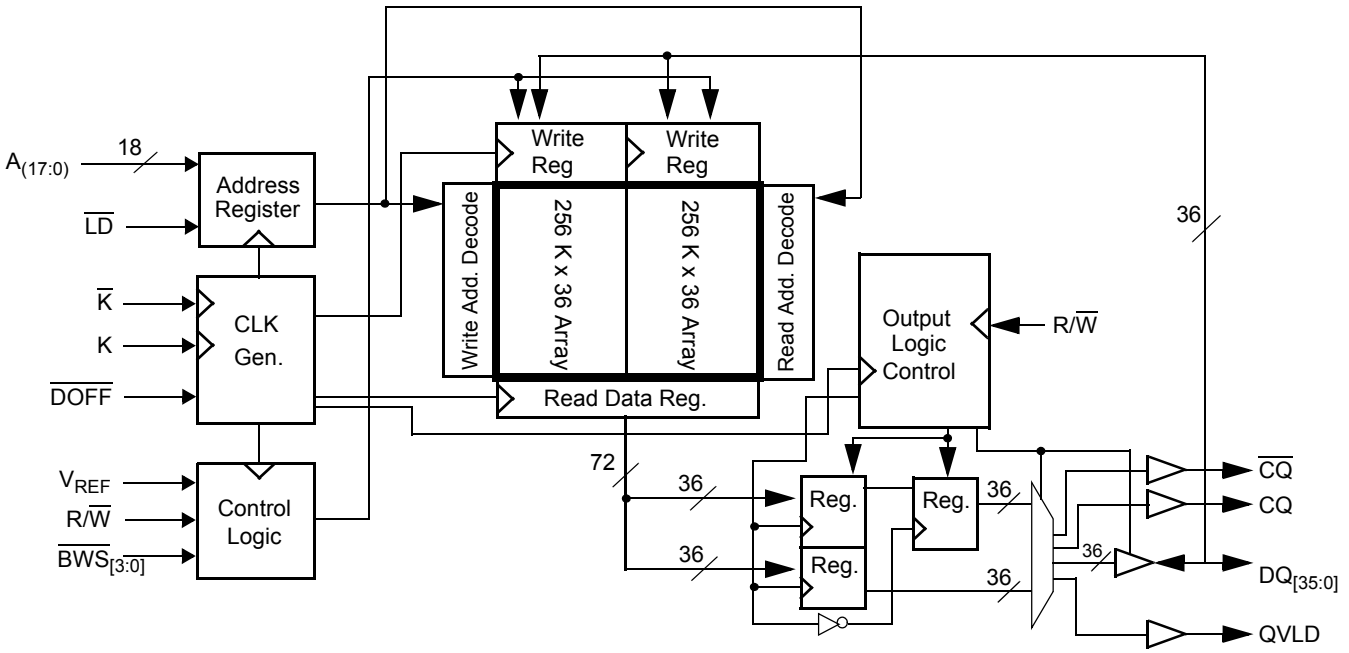



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## Logic Block Diagram (CY7C1168KV18)




## Logic Block Diagram (CY7C1170KV18)






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## Pin Configuration

The pin configurations for CY7C1166KV18, CY7C1177KV18, CY7C1168KV18, and CY7C1170KV18 follow. [2]

**165-Ball FBGA (13 x 15 x 1.4 mm) Pinout**

**CY7C1166KV18 (2 M x 8)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{CQ}$ | NC/72M | A | R/$\overline{W}$ | $\overline{NWS_1}$ | $\overline{K}$ | NC/144M | $\overline{LD}$ | A | NC/36M | CQ |
| **B** | NC | NC | NC | A | NC/288M | K | $\overline{NWS_0}$ | A | NC | NC | DQ3 |
| **C** | NC | NC | NC | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | NC |
| **D** | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| **E** | NC | NC | DQ4 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ2 |
| **F** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **G** | NC | NC | DQ5 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **H** | $\overline{DOFF}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| **J** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQ1 | NC |
| **K** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **L** | NC | DQ6 | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ0 |
| **M** | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| **N** | NC | NC | NC | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | NC |
| **P** | NC | NC | DQ7 | A | A | QVLD | A | A | NC | NC | NC |
| **R** | TDO | TCK | A | A | A | NC | A | A | A | TMS | TDI |

**CY7C1177KV18 (2 M x 9)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{CQ}$ | NC/72M | A | R/$\overline{W}$ | NC | $\overline{K}$ | NC/144M | $\overline{LD}$ | A | NC/36M | CQ |
| **B** | NC | NC | NC | A | NC/288M | K | $\overline{BWS_0}$ | A | NC | NC | DQ3 |
| **C** | NC | NC | NC | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | NC |
| **D** | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| **E** | NC | NC | DQ4 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ2 |
| **F** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **G** | NC | NC | DQ5 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **H** | $\overline{DOFF}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| **J** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQ1 | NC |
| **K** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **L** | NC | DQ6 | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ0 |
| **M** | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| **N** | NC | NC | NC | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | NC |
| **P** | NC | NC | DQ7 | A | A | QVLD | A | A | NC | NC | DQ8 |
| **R** | TDO | TCK | A | A | A | NC | A | A | A | TMS | TDI |

**Note**
2. NC/36M, NC/72M, NC/144M, and NC/288M are not connected to the die and can be tied to any voltage level.



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## Pin Configuration (continued)

The pin configurations for CY7C1166KV18, CY7C1177KV18, CY7C1168KV18, and CY7C1170KV18 follow. [2]

**165-Ball FBGA (13 x 15 x 1.4 mm) Pinout**

**CY7C1168KV18 (1 M x 18)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{CQ}$ | NC/72M | A | R/$\overline{W}$ | $\overline{BWS_1}$ | $\overline{K}$ | NC/144M | $\overline{LD}$ | A | NC/36M | CQ |
| **B** | NC | DQ9 | NC | A | NC/288M | K | $\overline{BWS_0}$ | A | NC | NC | DQ8 |
| **C** | NC | NC | NC | $V_{SS}$ | A | NC | A | $V_{SS}$ | NC | DQ7 | NC |
| **D** | NC | NC | DQ10 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| **E** | NC | NC | DQ11 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ6 |
| **F** | NC | DQ12 | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | DQ5 |
| **G** | NC | NC | DQ13 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **H** | $\overline{DOFF}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| **J** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQ4 | NC |
| **K** | NC | NC | DQ14 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | DQ3 |
| **L** | NC | DQ15 | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ2 |
| **M** | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | DQ1 | NC |
| **N** | NC | NC | DQ16 | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | NC |
| **P** | NC | NC | DQ17 | A | A | QVLD | A | A | NC | NC | DQ0 |
| **R** | TDO | TCK | A | A | A | NC | A | A | A | TMS | TDI |

**CY7C1170KV18 (512 K x 36)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{CQ}$ | NC/144M | NC/36M | R/$\overline{W}$ | $\overline{BWS_2}$ | $\overline{K}$ | $\overline{BWS_1}$ | $\overline{LD}$ | A | NC/72M | CQ |
| **B** | NC | DQ27 | DQ18 | A | $\overline{BWS_3}$ | K | $\overline{BWS_0}$ | A | NC | NC | DQ8 |
| **C** | NC | NC | DQ28 | $V_{SS}$ | A | NC | A | $V_{SS}$ | NC | DQ17 | DQ7 |
| **D** | NC | DQ29 | DQ19 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | DQ16 |
| **E** | NC | NC | DQ20 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | DQ15 | DQ6 |
| **F** | NC | DQ30 | DQ21 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | DQ5 |
| **G** | NC | DQ31 | DQ22 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | DQ14 |
| **H** | $\overline{DOFF}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| **J** | NC | NC | DQ32 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQ13 | DQ4 |
| **K** | NC | NC | DQ23 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | DQ12 | DQ3 |
| **L** | NC | DQ33 | DQ24 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | DQ2 |
| **M** | NC | NC | DQ34 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | DQ11 | DQ1 |
| **N** | NC | DQ35 | DQ25 | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | DQ10 |
| **P** | NC | NC | DQ26 | A | A | QVLD | A | A | NC | DQ9 | DQ0 |
| **R** | TDO | TCK | A | A | A | NC | A | A | A | TMS | TDI |



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## Pin Definitions

| Pin Name | I/O | Pin Description |
|---|---|---|
| $DQ_{[x:0]}$ | Input output-synchronous | Data Input Output Signals. Inputs are sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. These pins drive out the requested data when the read operation is active. Valid data is driven out on the rising edge of both the K and $\overline{K}$ clocks during read operations. When read access is deselected, $Q_{[x:0]}$ are automatically tristated.<br>CY7C1166KV18 – $DQ_{[7:0]}$<br>CY7C1177KV18 – $DQ_{[8:0]}$<br>CY7C1168KV18 – $DQ_{[17:0]}$<br>CY7C1170KV18 – $DQ_{[35:0]}$ |
| $\overline{LD}$ | Input-synchronous | Synchronous Load. Sampled on the rising edge of the K clock. This input is brought LOW when a bus cycle sequence is defined. This definition includes address and read/write direction. All transactions operate on a burst of 2 data. $\overline{LD}$ must meet the setup and hold times around edge of K. |
| $\overline{NWS_0}$, $NWS_1$ | Input-synchronous | Nibble Write Select 0, 1 – Active LOW (CY7C1166KV18 only). Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which nibble is written into the device during the current portion of the write operations. Nibbles not written remain unaltered.<br>$\overline{NWS_0}$ controls $D_{[3:0]}$ and $\overline{NWS_1}$ controls $D_{[7:4]}$.<br>All the Nibble Write Selects are sampled on the same edge as the data. Deselecting a Nibble Write Select ignores the corresponding nibble of data and it is not written into the device. |
| $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$ | Input-synchronous | Byte Write Select 0, 1, 2, and 3 – Active LOW. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered.<br>CY7C1177KV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$<br>CY7C1168KV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$ and $\overline{BWS_1}$ controls $D_{[17:9]}$.<br>CY7C1170KV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$, $\overline{BWS_2}$ controls $D_{[26:18]}$ and $\overline{BWS_3}$ controls $D_{[35:27]}$.<br>All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and it is not written into the device. |
| A | Input-synchronous | Address Inputs. Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 2M x 8 (2 arrays each of 1M x 8) for CY7C1166KV18 and 2M x 9 (2 arrays each of 1M x9) for CY7C1177KV18, 1M x 18 (2 arrays each of 512K x 18) for CY7C1168KV18, and 512K x 36 (2 arrays each of 256K x 36) for CY7C1170KV18. |
| R/$\overline{W}$ | Input-synchronous | Synchronous Read or Write Input. When $\overline{LD}$ is LOW, this input designates the access type (read when R/$\overline{W}$ is HIGH, write when R/$\overline{W}$ is LOW) for loaded address. R/$\overline{W}$ must meet the setup and hold times around edge of K. |
| QVLD | Valid output indicator | Valid Output Indicator. The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$. |
| K | Input clock | Positive Input Clock Input. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$. All accesses are initiated on the rising edge of K. |
| $\overline{K}$ | Input clock | Negative Input Clock Input. $\overline{K}$ is used to capture synchronous data being presented to the device and to drive out data through $Q_{[x:0]}$. |
| CQ | Echo clock | Synchronous Echo Clock Outputs. This is a free running clock and is synchronized to the input clock (K) of the DDR II+. The timing for the echo clocks is shown in the Switching Characteristics on page 24. |
| $\overline{CQ}$ | Echo clock | Synchronous Echo Clock Outputs. This is a free running clock and is synchronized to the input clock ($\overline{K}$) of the DDR II+. The timing for the echo clocks is shown in the Switching Characteristics on page 24. |
| ZQ | Input | Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to $V_{DDQ}$, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected. |



[+] Feedback

## Pin Definitions (continued)

| Pin Name | I/O | Pin Description |
|---|---|---|
| $\overline{DOFF}$ | Input | PLL Turn Off – Active LOW. Connecting this pin to ground turns off the PLL inside the device. The timing in the PLL turned off operation differs from those listed in this data sheet. For normal operation, this pin can be connected to a pull up through a 10 KΩ or less pull up resistor. The device behaves in DDR I mode when the PLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with DDR I timing. |
| TDO | Output | TDO for JTAG |
| TCK | Input | TCK Pin for JTAG |
| TDI | Input | TDI Pin for JTAG |
| TMS | Input | TMS Pin for JTAG |
| NC | N/A | Not Connected to the Die. Can be tied to any voltage level. |
| NC/36M | Input | Not Connected to the Die. Can be tied to any voltage level. |
| NC/72M | Input | Not Connected to the Die. Can be tied to any voltage level. |
| NC/144M | Input | Not Connected to the Die. Can be tied to any voltage level. |
| NC/288M | Input | Not Connected to the Die. Can be tied to any voltage level. |
| $V_{REF}$ | Input-reference | Reference Voltage Input. Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points. |
| $V_{DD}$ | Power supply | Power supply Inputs to the Core of the Device |
| $V_{SS}$ | Ground | Ground for the Device |
| $V_{DDQ}$ | Power supply | Power Supply Inputs for the Outputs of the Device |

## Functional Overview

The CY7C1166KV18, CY7C1177KV18, CY7C1168KV18, and CY7C1170KV18 are synchronous pipelined Burst SRAMs equipped with a DDR interface, which operates with a read latency of two and half cycles when DOFF pin is tied HIGH. When DOFF pin is set LOW or connected to $V_{SS}$ the device behaves in DDR I mode with a read latency of one clock cycle.

Accesses are initiated on the rising edge of the positive input clock (K). All synchronous input and output timing is referenced from the rising edge of the input clocks (K and $\overline{K}$).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the input clocks (K and $\overline{K}$).

All synchronous control ($R/\overline{W}$, $\overline{LD}$, $\overline{NWS}_{[X:0]}$, $\overline{BWS}_{[X:0]}$) inputs pass through input registers controlled by the rising edge of the input clock (K).

CY7C1168KV18 is described in the following sections. The same basic descriptions apply to CY7C1166KV18, CY7C1177KV18, and CY7C1170KV18.

### Read Operations

The CY7C1168KV18 is organized internally as two arrays of 512 K x 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting $R/\overline{W}$ HIGH and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to the address inputs is stored in the read address register. Following the next two $\overline{K}$ clock rise, the corresponding 18-bit word of data from this address location is driven onto the $Q_{[17:0]}$ using $\overline{K}$ as the output timing reference. On the subsequent rising edge of K, the next 18-bit data word is driven onto the $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the input clock (K and $\overline{K}$). To maintain the internal logic, each read access must be allowed to complete. Read accesses can be initiated on every rising edge of the positive input clock (K).

When read access is deselected, the CY7C1168KV18 first completes the pending read transactions. Synchronous internal circuitry automatically tri-states the output following the next rising edge of the negative input clock ($\overline{K}$). This enables for a transition between devices without the insertion of wait states in a depth expanded memory.

### Write Operations

Write operations are initiated by asserting $R/\overline{W}$ LOW and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the write address register. On the following K clock rise, the data presented to $D_{[17:0]}$ is latched and stored into the 18-bit write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{K}$) the information presented to $D_{[17:0]}$ is also stored into the write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. The 36 bits of data are then written into the memory array at the specified location. Write accesses can be initiated on every rising edge of the positive input clock (K). Doing so pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When the write access is deselected, the device ignores all inputs after the pending write operations have been completed.

### Byte Write Operations

Byte write operations are supported by the CY7C1168KV18. A write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$, which are sampled with each set of 18-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read, modify, or write operations to a byte write operation.

### DDR Operation

The CY7C1168KV18 enables high-performance operation through high clock frequencies (achieved through pipelining) and DDR mode of operation. The CY7C1168KV18 requires two No Operation (NOP) cycle during transition from a read to a write cycle. At higher frequencies, some applications require third NOP cycle to avoid contention.

If a read occurs after a write cycle, address and data for the write are stored in registers. The write information is stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next write cycle occurs. On the first write cycle after the read(s), the stored data from the earlier write is written into the SRAM array. This is called a Posted write.

If a read is performed on the same address on which a write is performed in the previous cycle, the SRAM reads out the most current data. The SRAM does this by bypassing the memory array and reading the data from the registers.

### Depth Expansion

Depth expansion requires replicating the $\overline{LD}$ control signal for each bank. All other control signals can be common between banks as appropriate.

### Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and $V_{SS}$ to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175Ω and 350Ω, with $V_{DDQ}$ = 1.5V. The output impedance is adjusted every 1024 cycles upon power up to account for drifts in supply voltage and temperature.

### Echo Clocks

Echo clocks are provided on the DDR II+ to simplify data capture on high-speed systems. Two echo clocks are generated by the DDR II+. CQ is referenced with respect to K and $\overline{CQ}$ is referenced with respect to $\overline{K}$. These are free-running clocks and are synchronized to the input clock of the DDR II+. The timing for the echo clocks is shown in the "Switching Characteristics" on page 24.



[+] Feedback

### Valid Data Indicator (QVLD)

QVLD is provided on the DDR II+ to simplify data capture on high speed systems. The QVLD is generated by the DDR II+ device along with data output. This signal is also edge aligned with the echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

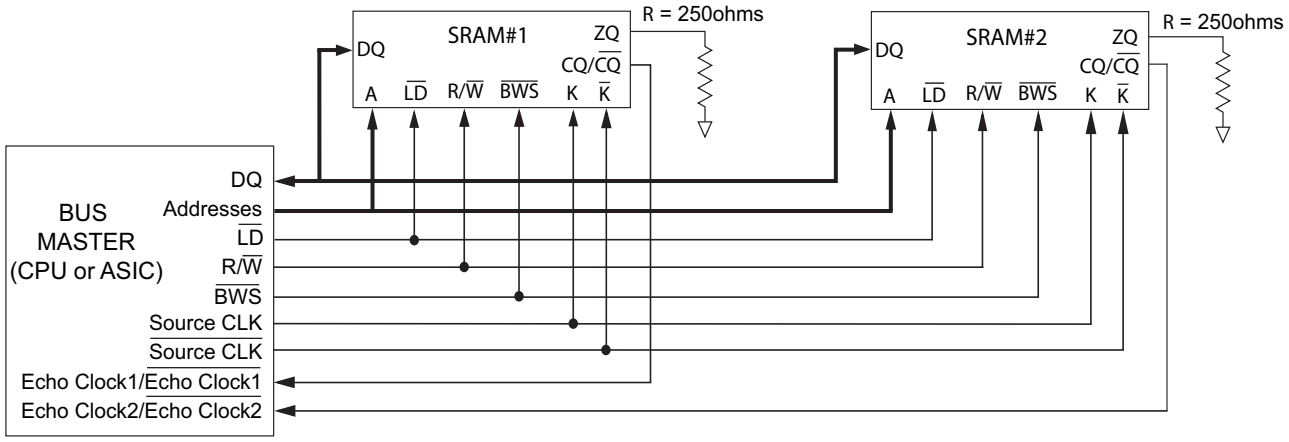
### PLL

These chips use a PLL that is designed to function between 120 MHz and the specified maximum clock frequency. During power up, when the DOFF is tied HIGH, the PLL is locked after 20 µs of stable clock. The PLL can also be reset by slowing or stopping the input clock K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary to reset the PLL to lock to the desired frequency. The PLL automatically locks 20 µs after a stable clock is presented. The PLL may be disabled by applying ground to the DOFF pin. When the PLL is turned off, the device behaves in DDR I mode (with one cycle latency and a longer access time). For information, refer to the application note, PLL Considerations in QDRII/DDRII/QDRII+/DDRII+.

## Application Example

Figure 1 shows two DDR II+ used in an application.

**Figure 1. Application Example**






[+] Feedback

## Truth Table

The truth table for the CY7C1166KV18, CY7C1177KV18, CY7C1168KV18, and CY7C1170KV18 follows. [3, 4, 5, 6, 7, 8]

| Operation | K | $\overline{LD}$ | R/$\overline{W}$ | DQ | DQ |
|---|---|---|---|---|---|
| Write cycle:<br>Load address; wait one cycle;<br>input write data on consecutive K and $\overline{K}$ rising edges. | L-H | L | L | D(A) at K(t + 1) ↑ | D(A+1) at $\overline{K}$(t + 1) ↑ |
| Read cycle: (2.5 cycle latency)<br>Load address; wait two and half cycles;<br>read data on consecutive $\overline{K}$ and K rising edges. | L-H | L | H | Q(A) at $\overline{K}$(t + 2)↑ | Q(A+1) at K(t + 3) ↑ |
| NOP: No operation | L-H | H | X | High Z | High Z |
| Standby: Clock stopped | Stopped | X | X | Previous state | Previous state |

## Write Cycle Descriptions

The write cycle description table for CY7C1166KV18 and CY7C1168KV18 follows. [3, 9]

| $\overline{BWS_0}$/ $\overline{NWS_0}$ | $\overline{BWS_1}$/ $\overline{NWS_1}$ | K | $\overline{K}$ | Comments |
|---|---|---|---|---|
| L | L | L–H | – | During the data portion of a write sequence:<br>CY7C1166KV18 – both nibbles ($D_{[7:0]}$) are written into the device.<br>CY7C1168KV18 – both bytes ($D_{[17:0]}$) are written into the device. |
| L | L | – | L-H | During the data portion of a write sequence:<br>CY7C1166KV18 – both nibbles ($D_{[7:0]}$) are written into the device.<br>CY7C1168KV18 – both bytes ($D_{[17:0]}$) are written into the device. |
| L | H | L–H | – | During the data portion of a write sequence:<br>CY7C1166KV18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered.<br>CY7C1168KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered. |
| L | H | – | L–H | During the data portion of a write sequence:<br>CY7C1166KV18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered.<br>CY7C1168KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered. |
| H | L | L–H | – | During the data portion of a write sequence:<br>CY7C1166KV18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered.<br>CY7C1168KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered. |
| H | L | – | L–H | During the data portion of a write sequence:<br>CY7C1166KV18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered.<br>CY7C1168KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered. |
| H | H | L–H | – | No data is written into the devices during this portion of a write operation. |
| H | H | – | L–H | No data is written into the devices during this portion of a write operation. |

**Notes**
3. X = 'Don't Care', H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
4. Device powers up deselected with the outputs in a tristate condition.
5. 'A' represents address location latched by the devices when transaction was initiated. A + 1 represents the address sequence in the burst.
6. 't' represents the cycle at which a read/write operation is started. t + 1 and t + 2 are the first and second clock cycles succeeding the 't' clock cycle.
7. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges as well.
8. Ensure that when clock is stopped K = K and C = C = HIGH. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
9. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{NWS_0}$, $\overline{NWS_1}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.



[+] Feedback

## Write Cycle Descriptions

The write cycle description table for CY7C1177KV18 follows. [10, 11]

| $\overline{BWS_0}$ | K | $\overline{K}$ | Comments |
|---|---|---|---|
| L | L–H | – | During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device. |
| L | – | L–H | During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device. |
| H | L–H | – | No data is written into the device during this portion of a write operation. |
| H | – | L–H | No data is written into the device during this portion of a write operation. |

## Write Cycle Descriptions

The write cycle description table for CY7C1170KV18 follows. [10, 11]

| $\overline{BWS_0}$ | $\overline{BWS_1}$ | $\overline{BWS_2}$ | $\overline{BWS_3}$ | K | $\overline{K}$ | Comments |
|---|---|---|---|---|---|---|
| L | L | L | L | L–H | – | During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device. |
| L | L | L | L | – | L–H | During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device. |
| L | H | H | H | L–H | – | During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered. |
| L | H | H | H | – | L–H | During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered. |
| H | L | H | H | L–H | – | During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered. |
| H | L | H | H | – | L–H | During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered. |
| H | H | L | H | L–H | – | During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered. |
| H | H | L | H | – | L–H | During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered. |
| H | H | H | L | L–H | – | During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered. |
| H | H | H | L | – | L–H | During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered. |
| H | H | H | H | L–H | – | No data is written into the device during this portion of a write operation. |
| H | H | H | H | – | L–H | No data is written into the device during this portion of a write operation. |

**Notes**
10. X = 'Don't Care', H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
11. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{NWS_0}$, $\overline{NWS_1}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8V I/O logic levels.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ($V_{SS}$) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to $V_{DD}$ through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

### Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

### Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

### Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller State Diagram on page 15. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

### Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see Instruction Codes on page 18). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

### Performing a TAP Reset

A Reset is performed by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

### TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

*Instruction Register*

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in TAP Controller Block Diagram on page 16. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

*Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

*Boundary Scan Register*

The boundary scan register is connected to all of the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The Boundary Scan Order on page 19 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

*Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 18.

### TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page 18. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.



[+] Feedback

*IDCODE*

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is supplied a Test-Logic-Reset state.

*SAMPLE Z*

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is supplied during the Update IR state.

*SAMPLE/PRELOAD*

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

Remember that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times ($t_{CS}$ and $t_{CH}$). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

*BYPASS*

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

*EXTEST*

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

*EXTEST OUTPUT BUS TRISTATE*

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has a special bit located at bit #47. When this scan cell, called the “extest output bus tristate,” is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

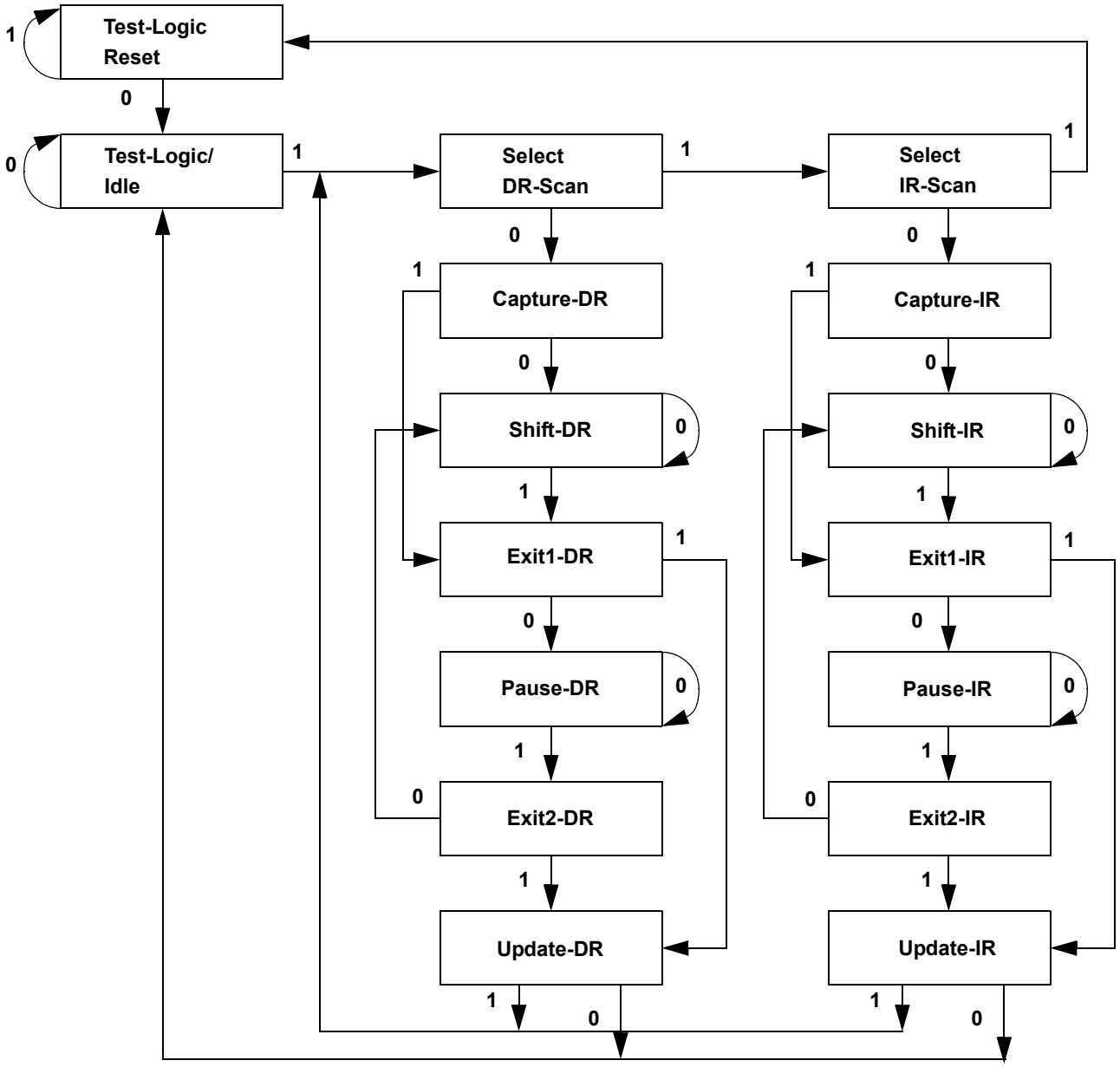
This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

*Reserved*

These instructions are not implemented but are reserved for future use. Do not use these instructions.

## TAP Controller State Diagram

The state diagram for the TAP controller follows. [12]

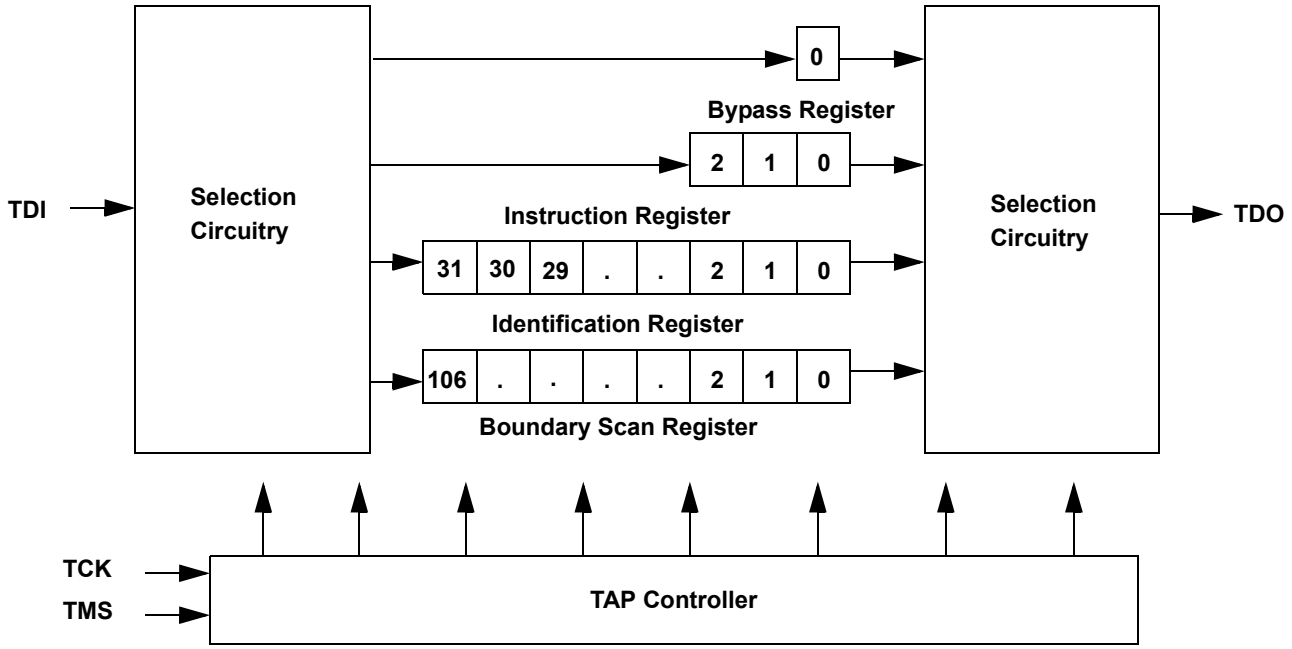



**Note**
12. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.



[+] Feedback

## TAP Controller Block Diagram




## TAP Electrical Characteristics

Over the Operating Range [13, 14, 15]

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH voltage | $I_{OH}$ = –2.0 mA | 1.4 | – | V |
| $V_{OH2}$ | Output HIGH voltage | $I_{OH}$ = –100 µA | 1.6 | – | V |
| $V_{OL1}$ | Output LOW voltage | $I_{OL}$ = 2.0 mA | – | 0.4 | V |
| $V_{OL2}$ | Output LOW voltage | $I_{OL}$ = 100 µA | – | 0.2 | V |
| $V_{IH}$ | Input HIGH voltage | – | 0.65$V_{DD}$ | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | – | –0.3 | 0.35$V_{DD}$ | V |
| $I_X$ | Input and output load current | GND ≤ $V_I$ ≤ $V_{DD}$ | –5 | 5 | µA |

**Notes**
13. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics table.
14. Overshoot: $V_{IH}$(AC) < $V_{DDQ}$ + 0.3 V (Pulse width less than $t_{CYC}$/2), Undershoot: $V_{IL}$(AC) > –0.3 V (Pulse width less than $t_{CYC}$/2).
15. All Voltage referenced to Ground.



[+] Feedback

## TAP AC Switching Characteristics

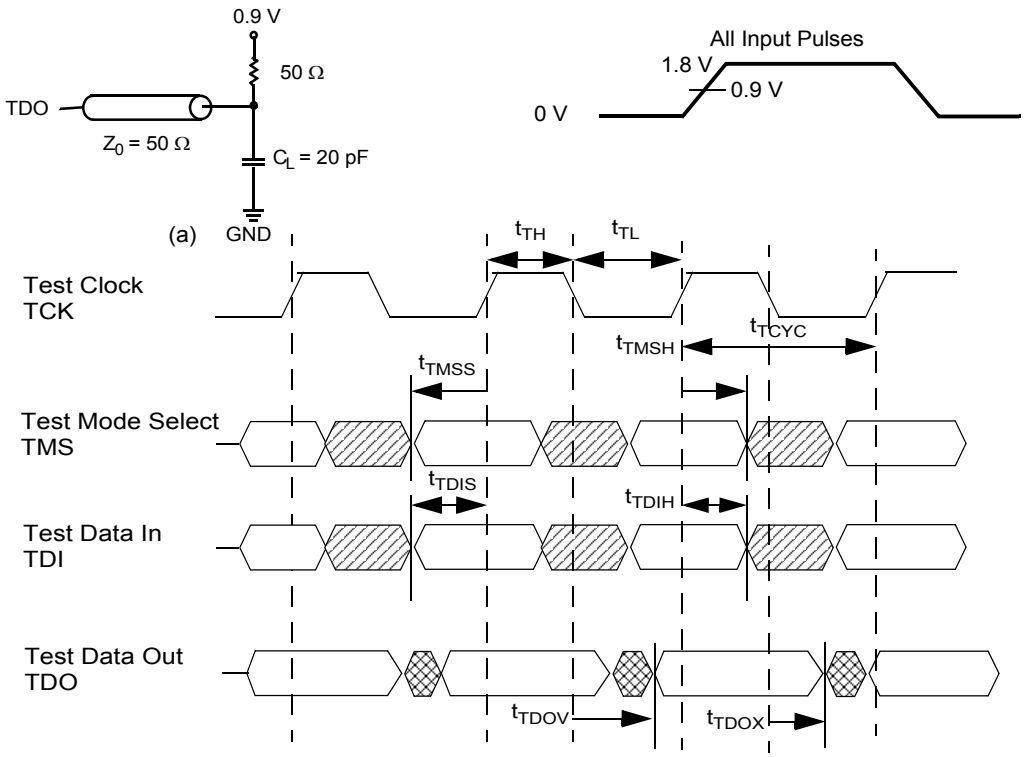
Over the Operating Range [16, 17]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{TCYC}$ | TCK Clock Cycle Time | 50 | – | ns |
| $t_{TF}$ | TCK Clock Frequency | – | 20 | MHz |
| $t_{TH}$ | TCK Clock HIGH | 20 | – | ns |
| $t_{TL}$ | TCK Clock LOW | 20 | – | ns |
| **Setup Times** | | | | |
| $t_{TMSS}$ | TMS Setup to TCK Clock Rise | 5 | – | ns |
| $t_{TDIS}$ | TDI Setup to TCK Clock Rise | 5 | – | ns |
| $t_{CS}$ | Capture Setup to TCK Rise | 5 | – | ns |
| **Hold Times** | | | | |
| $t_{TMSH}$ | TMS Hold after TCK Clock Rise | 5 | – | ns |
| $t_{TDIH}$ | TDI Hold after Clock Rise | 5 | – | ns |
| $t_{CH}$ | Capture Hold after Clock Rise | 5 | – | ns |
| **Output Times** | | | | |
| $t_{TDOV}$ | TCK Clock LOW to TDO Valid | – | 10 | ns |
| $t_{TDOX}$ | TCK Clock LOW to TDO Invalid | 0 | – | ns |

## TAP Timing and Test Conditions

Figure 2 shows the TAP timing and test conditions. [17]

**Figure 2. TAP Timing and Test Conditions**




**Notes**

16. $t_{CS}$ and $t_{CH}$ refer to the setup and hold time requirements of latching data from the boundary scan register.
17. Test conditions are specified using the load in TAP AC Test Conditions. $t_R/t_F$ = 1 ns.



[+] Feedback

## Identification Register Definitions

| Instruction Field | Value | | | | Description |
|---|---|---|---|---|---|
| | CY7C1166KV18 | CY7C1177KV18 | CY7C1168KV18 | CY7C1170KV18 | |
| Revision number (31:29) | 000 | 000 | 000 | 000 | Version number. |
| Cypress device ID (28:12) | 11010111000000101 | 11010111000001101 | 11010111000010101 | 11010111000100101 | Defines the type of SRAM. |
| Cypress JEDEC ID (11:1) | 00000110100 | 00000110100 | 00000110100 | 00000110100 | Allows unique identification of SRAM vendor. |
| ID register presence (0) | 1 | 1 | 1 | 1 | Indicates the presence of an ID register. |

## Scan Register Sizes

| Register Name | Bit Size |
|---|---|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 107 |

## Instruction Codes

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures the input and output ring contents. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation. |
| SAMPLE Z | 010 | Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state. |
| RESERVED | 011 | Do not use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. |
| RESERVED | 101 | Do not use: This instruction is reserved for future use. |
| RESERVED | 110 | Do not use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operation. |

## Boundary Scan Order

| Bit # | Bump ID |
|---|---|
| 0 | 6R |
| 1 | 6P |
| 2 | 6N |
| 3 | 7P |
| 4 | 7N |
| 5 | 7R |
| 6 | 8R |
| 7 | 8P |
| 8 | 9R |
| 9 | 11P |
| 10 | 10P |
| 11 | 10N |
| 12 | 9P |
| 13 | 10M |
| 14 | 11N |
| 15 | 9M |
| 16 | 9N |
| 17 | 11L |
| 18 | 11M |
| 19 | 9L |
| 20 | 10L |
| 21 | 11K |
| 22 | 10K |
| 23 | 9J |
| 24 | 9K |
| 25 | 10J |
| 26 | 11J |
| 27 | 11H |

| Bit # | Bump ID |
|---|---|
| 28 | 10G |
| 29 | 9G |
| 30 | 11F |
| 31 | 11G |
| 32 | 9F |
| 33 | 10F |
| 34 | 11E |
| 35 | 10E |
| 36 | 10D |
| 37 | 9E |
| 38 | 10C |
| 39 | 11D |
| 40 | 9C |
| 41 | 9D |
| 42 | 11B |
| 43 | 11C |
| 44 | 9B |
| 45 | 10B |
| 46 | 11A |
| 47 | Internal |
| 48 | 9A |
| 49 | 8B |
| 50 | 7C |
| 51 | 6C |
| 52 | 8A |
| 53 | 7A |
| 54 | 7B |
| 55 | 6B |

| Bit # | Bump ID |
|---|---|
| 56 | 6A |
| 57 | 5B |
| 58 | 5A |
| 59 | 4A |
| 60 | 5C |
| 61 | 4B |
| 62 | 3A |
| 63 | 1H |
| 64 | 1A |
| 65 | 2B |
| 66 | 3B |
| 67 | 1C |
| 68 | 1B |
| 69 | 3D |
| 70 | 3C |
| 71 | 1D |
| 72 | 2C |
| 73 | 3E |
| 74 | 2D |
| 75 | 2E |
| 76 | 1E |
| 77 | 2F |
| 78 | 3F |
| 79 | 1G |
| 80 | 1F |
| 81 | 3G |
| 82 | 2G |
| 83 | 1J |

| Bit # | Bump ID |
|---|---|
| 84 | 2J |
| 85 | 3K |
| 86 | 3J |
| 87 | 2K |
| 88 | 1K |
| 89 | 2L |
| 90 | 3L |
| 91 | 1M |
| 92 | 1L |
| 93 | 3N |
| 94 | 3M |
| 95 | 1N |
| 96 | 2M |
| 97 | 3P |
| 98 | 2N |
| 99 | 2P |
| 100 | 1P |
| 101 | 3R |
| 102 | 4R |
| 103 | 4P |
| 104 | 5P |
| 105 | 5N |
| 106 | 5R |

## Power Up Sequence in DDR II+ SRAM

DDR II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

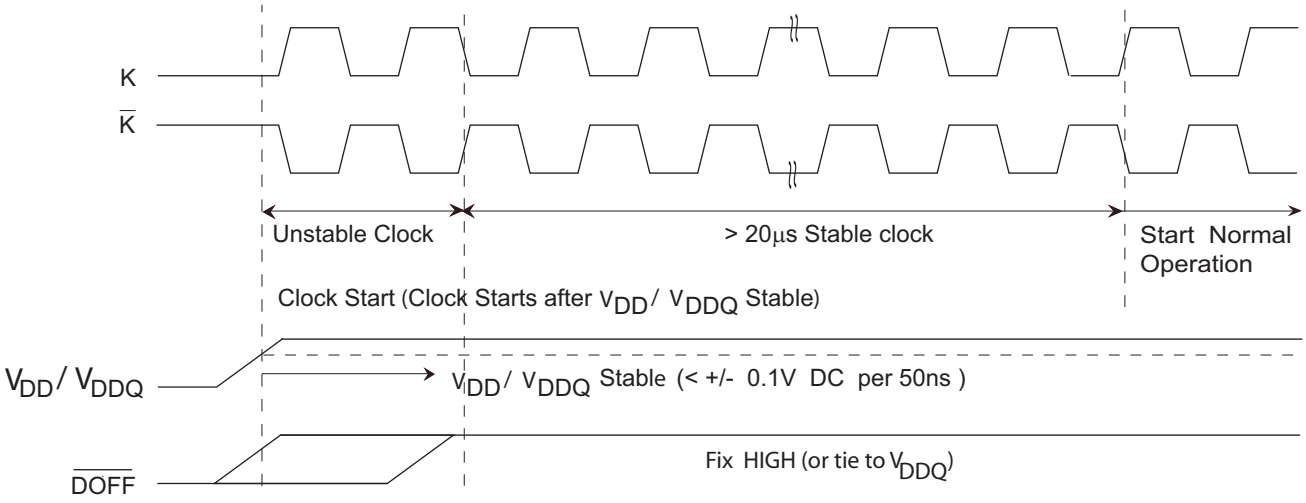
### Power Up Sequence

- Apply power and drive $\overline{DOFF}$ either HIGH or LOW (All other inputs can be HIGH or LOW).
  - Apply $V_{DD}$ before $V_{DDQ}$.
  - Apply $V_{DDQ}$ before $V_{REF}$ or at the same time as $V_{REF}$.
  - Drive $\overline{DOFF}$ HIGH.
- Provide stable $\overline{DOFF}$ (HIGH), power and clock (K, $\overline{K}$) for 20 µs to lock the PLL.

### PLL Constraints

- PLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The PLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the PLL is enabled, then the PLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 20 µs of stable clock to relock to the desired clock frequency.

**Figure 3. Power Up Waveforms**






[+] Feedback

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .....–65 °C to +150 °C

Ambient temperature with power applied ..–55 °C to +125 °C

Supply voltage on $V_{DD}$ relative to GND.....–0.5 V to +2.9 V

Supply voltage on $V_{DDQ}$ relative to GND..... –0.5 V to +$V_{DD}$

DC applied to outputs in High Z.....–0.5 V to $V_{DDQ}$ + 0.3 V

DC input voltage [18] .....–0.5 V to $V_{DD}$ + 0.3 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, M 3015)... >2,001 V

Latch up current..... >200 mA

## Operating Range

| Range | Ambient Temperature ($T_A$) | $V_{DD}$ [19] | $V_{DDQ}$ [19] |
|---|---|---|---|
| Commercial | 0 °C to +70 °C | 1.8 ± 0.1 V | 1.4 V to $V_{DD}$ |
| Industrial | –40 °C to +85 °C | | |

## Neutron Soft Error Immunity

| Parameter | Description | Test Conditions | Typ | Max* | Unit |
|---|---|---|---|---|---|
| LSBU | Logical single-bit upsets | 25 °C | 197 | 216 | FIT/ Mb |
| LMBU | Logical multi-bit upsets | 25 °C | 0 | 0.01 | FIT/ Mb |
| SEL | Single event latch up | 85 °C | 0 | 0.1 | FIT/ Dev |

* *No LMBU or SEL events occurred during testing*; this column represents a statistical $\chi^2$, 95% confidence limit calculation. For more details refer to application note, Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates - AN54908.

## Electrical Characteristics

### DC Electrical Characteristics

Over the Operating Range [19]

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | – | 1.7 | 1.8 | 1.9 | V |
| $V_{DDQ}$ | I/O supply voltage | – | 1.4 | 1.5 | $V_{DD}$ | V |
| $V_{OH}$ | Output HIGH voltage | Note 21 | $V_{DDQ}/2 – 0.12$ | – | $V_{DDQ}/2 + 0.12$ | V |
| $V_{OL}$ | Output LOW voltage | Note 22 | $V_{DDQ}/2 – 0.12$ | – | $V_{DDQ}/2 + 0.12$ | V |
| $V_{OH(LOW)}$ | Output HIGH voltage | $I_{OH}$ = –0.1 mA, nominal impedance | $V_{DDQ} – 0.2$ | – | $V_{DDQ}$ | V |
| $V_{OL(LOW)}$ | Output LOW voltage | $I_{OL}$ = 0.1 mA, nominal impedance | $V_{SS}$ | – | 0.2 | V |
| $V_{IH}$ | Input HIGH voltage | – | $V_{REF} + 0.1$ | – | $V_{DDQ} + 0.15$ | V |
| $V_{IL}$ | Input LOW voltage | – | –0.15 | – | $V_{REF} – 0.1$ | V |
| $I_X$ | Input leakage current | $GND \le V_I \le V_{DDQ}$ | –2 | – | 2 | µA |
| $I_{OZ}$ | Output leakage current | $GND \le V_I \le V_{DDQ}$, output disabled | –2 | – | 2 | µA |
| $V_{REF}$ | Input reference voltage [23] | Typical value = 0.75 V | 0.68 | 0.75 | 0.95 | V |

**Notes**

18. Overshoot: $V_{IH}(AC) < V_{DDQ} + 0.3$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -0.3$ V (Pulse width less than $t_{CYC}/2$).
19. All Voltage referenced to Ground.
20. Power up: assumes a linear ramp from 0 V to $V_{DD}$(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
21. Outputs are impedance controlled. $I_{OH} = -(V_{DDQ}/2)/(RQ/5)$ for values of $175\ \Omega \le RQ \le 350\ \Omega$.
22. Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of $175\Omega \le RQ \le 350\ \Omega$.
23. $V_{REF}$(min) = 0.68 V or 0.46 $V_{DDQ}$, whichever is larger, $V_{REF}$(max) = 0.95 V or 0.54 $V_{DDQ}$, whichever is smaller.



[+] Feedback

## Electrical Characteristics (continued)

### DC Electrical Characteristics

Over the Operating Range [19]

| Parameter | Description | Test Conditions | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $I_{DD}$ [24] | $V_{DD}$ operating supply | $V_{DD}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{CYC}$ | 550 MHz | (x8) | – | – | 630 | mA |
| | | | | (x9) | – | – | 630 | |
| | | | | (x18) | – | – | 650 | |
| | | | | (x36) | – | – | 820 | |
| | | | 500 MHz | (x8) | – | – | 590 | mA |
| | | | | (x9) | – | – | 590 | |
| | | | | (x18) | – | – | 600 | |
| | | | | (x36) | – | – | 760 | |
| | | | 450 MHz | (x8) | – | – | 550 | mA |
| | | | | (x9) | – | – | 550 | |
| | | | | (x18) | – | – | 560 | |
| | | | | (x36) | – | – | 700 | |
| | | | 400 MHz | (x8) | – | – | 500 | mA |
| | | | | (x9) | – | – | 500 | |
| | | | | (x18) | – | – | 510 | |
| | | | | (x36) | – | – | 640 | |
| $I_{SB1}$ | Automatic power down current | Max $V_{DD}$, both ports deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ f = $f_{MAX}$ = $1/t_{CYC}$, inputs static | 550 MHz | (x8) | – | – | 340 | mA |
| | | | | (x9) | – | – | 340 | |
| | | | | (x18) | – | – | 340 | |
| | | | | (x36) | – | – | 340 | |
| | | | 500 MHz | (x8) | – | – | 330 | mA |
| | | | | (x9) | – | – | 330 | |
| | | | | (x18) | – | – | 330 | |
| | | | | (x36) | – | – | 330 | |
| | | | 450 MHz | (x8) | – | – | 310 | mA |
| | | | | (x9) | – | – | 310 | |
| | | | | (x18) | – | – | 310 | |
| | | | | (x36) | – | – | 310 | |
| | | | 400 MHz | (x8) | – | – | 290 | mA |
| | | | | (x9) | – | – | 290 | |
| | | | | (x18) | – | – | 290 | |
| | | | | (x36) | – | – | 290 | |

### AC Electrical Characteristics

Over the Operating Range [25]

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH voltage | – | $V_{REF}$ + 0.2 | – | $V_{DDQ}$ + 0.24 | V |
| $V_{IL}$ | Input LOW voltage | – | –0.24 | – | $V_{REF}$ – 0.2 | V |

**Note**
24. The operation current is calculated with 50% read cycle and 50% write cycle.
25. Overshoot: $V_{IH}(AC) < V_{DDQ}$ + 0.3 V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -0.3$ V (Pulse width less than $t_{CYC}/2$).



[+] Feedback

## Capacitance

Tested initially and after any design or process change that may affect these parameters.

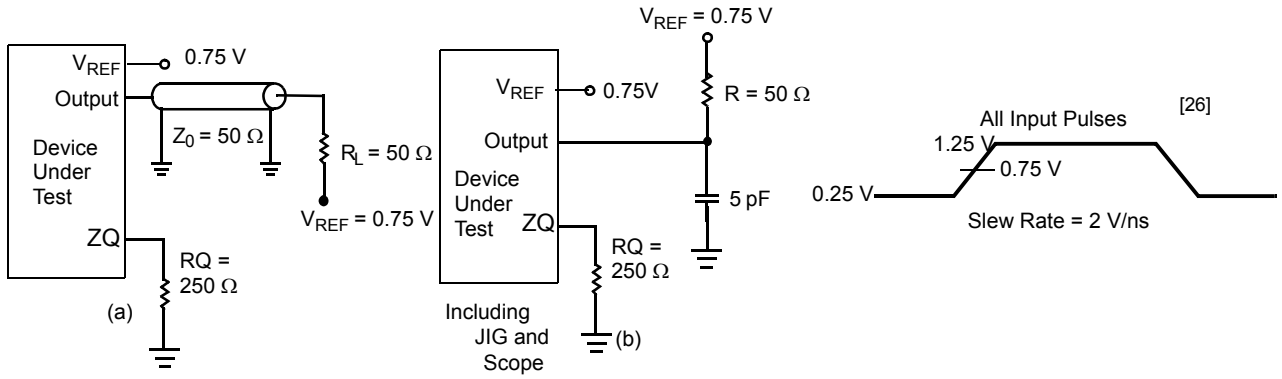
| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{DD}$ = 1.8 V, $V_{DDQ}$ = 1.5 V | 4 | pF |
| $C_O$ | Output capacitance | | 4 | pF |

## Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

| Parameter | Description | Test Conditions | 165 FBGA Package | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 13.7 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 3.73 | °C/W |

**Figure 4. AC Test Loads and Waveforms**




**Note**

26. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75 V, $V_{REF}$ = 0.75 V, RQ = 250 Ω, $V_{DDQ}$ = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified $I_{OL}/I_{OH}$ and load capacitance shown in (a) of AC Test Loads and Waveforms.



[+] Feedback

## Switching Characteristics

Over the Operating Range [27, 28]

| Cypress Parameter | Consortium Parameter | Description | 550 MHz | | 500 MHz | | 450 MHz | | 400 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{POWER}$ | | $V_{DD}$(Typical) to the First Access [29] | 1 | – | 1 | – | 1 | – | 1 | – | ms |
| $t_{CYC}$ | $t_{KHKH}$ | K Clock Cycle Time | 1.81 | 8.4 | 2.0 | 8.4 | 2.2 | 8.4 | 2.5 | 8.4 | ns |
| $t_{KH}$ | $t_{KHKL}$ | Input Clock (K/$\overline{K}$) HIGH | 0.4 | – | 0.4 | – | 0.4 | – | 0.4 | – | ns |
| $t_{KL}$ | $t_{KLKH}$ | Input Clock (K/$\overline{K}$) LOW | 0.4 | – | 0.4 | – | 0.4 | – | 0.4 | – | ns |
| $t_{KH\overline{K}H}$ | $t_{KH\overline{K}H}$ | K Clock Rise to $\overline{K}$ Clock Rise (rising edge to rising edge) | 0.77 | – | 0.85 | – | 0.94 | – | 1.06 | – | ns |
| **Setup Times** | | | | | | | | | | | |
| $t_{SA}$ | $t_{AVKH}$ | Address Setup to K Clock Rise | 0.23 | – | 0.25 | – | 0.275 | – | 0.4 | – | ns |
| $t_{SC}$ | $t_{IVKH}$ | Control Setup to K Clock Rise ($\overline{LD}$, R/$\overline{W}$) | 0.23 | – | 0.25 | – | 0.275 | – | 0.4 | – | ns |
| $t_{SCDDR}$ | $t_{IVKH}$ | Double Data Rate Control Setup to Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$) | 0.18 | – | 0.20 | – | 0.22 | – | 0.28 | – | ns |
| $t_{SD}$ | $t_{DVKH}$ | $D_{[X:0]}$ Setup to Clock (K/$\overline{K}$) Rise | 0.18 | – | 0.20 | – | 0.22 | – | 0.28 | – | ns |
| **Hold Times** | | | | | | | | | | | |
| $t_{HA}$ | $t_{KHAX}$ | Address Hold after K Clock Rise | 0.23 | – | 0.25 | – | 0.275 | – | 0.4 | – | ns |
| $t_{HC}$ | $t_{KHIX}$ | Control Hold after K Clock Rise ($\overline{LD}$, R/$\overline{W}$) | 0.23 | – | 0.25 | – | 0.275 | – | 0.4 | – | ns |
| $t_{HCDDR}$ | $t_{KHIX}$ | Double Data Rate Control Hold after Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$) | 0.18 | – | 0.20 | – | 0.22 | – | 0.28 | – | ns |
| $t_{HD}$ | $t_{KHDX}$ | $D_{[X:0]}$ Hold after Clock (K/$\overline{K}$) Rise | 0.18 | – | 0.20 | – | 0.22 | – | 0.28 | – | ns |
| **Output Times** | | | | | | | | | | | |
| $t_{CO}$ | $t_{CHQV}$ | K/$\overline{K}$ Clock Rise to Data Valid | – | 0.45 | – | 0.45 | – | 0.45 | – | 0.45 | ns |
| $t_{DOH}$ | $t_{CHQX}$ | Data Output Hold after Output K/$\overline{K}$ Clock Rise (Active to Active) | –0.45 | – | –0.45 | – | –0.45 | – | –0.45 | – | ns |
| $t_{CCQO}$ | $t_{CHCQV}$ | K/$\overline{K}$ Clock Rise to Echo Clock Valid | – | 0.45 | – | 0.45 | – | 0.45 | – | 0.45 | ns |
| $t_{CQOH}$ | $t_{CHCQX}$ | Echo Clock Hold after K/$\overline{K}$ Clock Rise | –0.45 | – | –0.45 | – | –0.45 | – | –0.45 | – | ns |
| $t_{CQD}$ | $t_{CQHQV}$ | Echo Clock High to Data Valid | – | 0.15 | – | 0.15 | – | 0.15 | – | 0.20 | ns |
| $t_{CQDOH}$ | $t_{CQHQX}$ | Echo Clock High to Data Invalid | –0.15 | – | –0.15 | – | –0.15 | – | –0.20 | – | ns |
| $t_{CQH}$ | $t_{CQHCQL}$ | Output Clock (CQ/$\overline{CQ}$) HIGH [30] | 0.655 | – | 0.75 | – | 0.85 | – | 1.00 | – | ns |
| $t_{CQH\overline{CQ}H}$ | $t_{CQH\overline{CQ}H}$ | CQ Clock Rise to $\overline{CQ}$ Clock Rise (rising edge to rising edge) [30] | 0.655 | – | 0.75 | – | 0.85 | – | 1.00 | – | ns |
| $t_{CHZ}$ | $t_{CHQZ}$ | Clock (K/$\overline{K}$) Rise to High Z (Active to High Z) [31, 32] | – | 0.45 | – | 0.45 | – | 0.45 | – | 0.45 | ns |
| $t_{CLZ}$ | $t_{CHQX1}$ | Clock (K/$\overline{K}$) Rise to Low Z [31, 32] | –0.45 | – | –0.45 | – | –0.45 | – | –0.45 | – | ns |
| $t_{QVLD}$ | $t_{CQHQVLD}$ | Echo Clock High to QVLD Valid [33] | –0.15 | 0.15 | –0.15 | 0.15 | –0.15 | 0.15 | –0.20 | 0.20 | ns |
| **PLL Timing** | | | | | | | | | | | |
| $t_{KC\ Var}$ | $t_{KC\ Var}$ | Clock Phase Jitter | – | 0.15 | – | 0.15 | – | 0.15 | – | 0.20 | ns |
| $t_{KC\ lock}$ | $t_{KC\ lock}$ | PLL Lock Time (K) | 20 | – | 20 | – | 20 | – | 20 | – | µs |
| $t_{KC\ Reset}$ | $t_{KC\ Reset}$ | K Static to PLL Reset [34] | 30 | – | 30 | – | 30 | – | 30 | – | ns |

**Notes**

27. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75 V, $V_{REF}$ = 0.75 V, RQ = 250 Ω, $V_{DDQ}$ = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified $I_{OL}/I_{OH}$ and load capacitance shown in (a) of AC Test Loads and Waveforms.
28. When a part with a maximum frequency above 400 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
29. This part has an internal voltage regulator; $t_{POWER}$ is the time that the power is supplied above $V_{DD}$ min initially before a read or write operation can be initiated.
30. These parameters are extrapolated from the input timing parameters ($t_{CYC}$/2 - 250 ps, where 250 ps is the internal jitter). These parameters are only guaranteed by design and are not tested in production.
31. $t_{CHZ}$, $t_{CLZ}$ are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms. Transition is measured ±100 mV from steady-state voltage.
32. At any voltage and temperature $t_{CHZ}$ is less than $t_{CLZ}$ and $t_{CHZ}$ less than $t_{CO}$.
33. $t_{QVLD}$ specification is applicable for both rising and falling edges of QVLD signal.
34. Hold to >$V_{IH}$ or <$V_{IL}$.

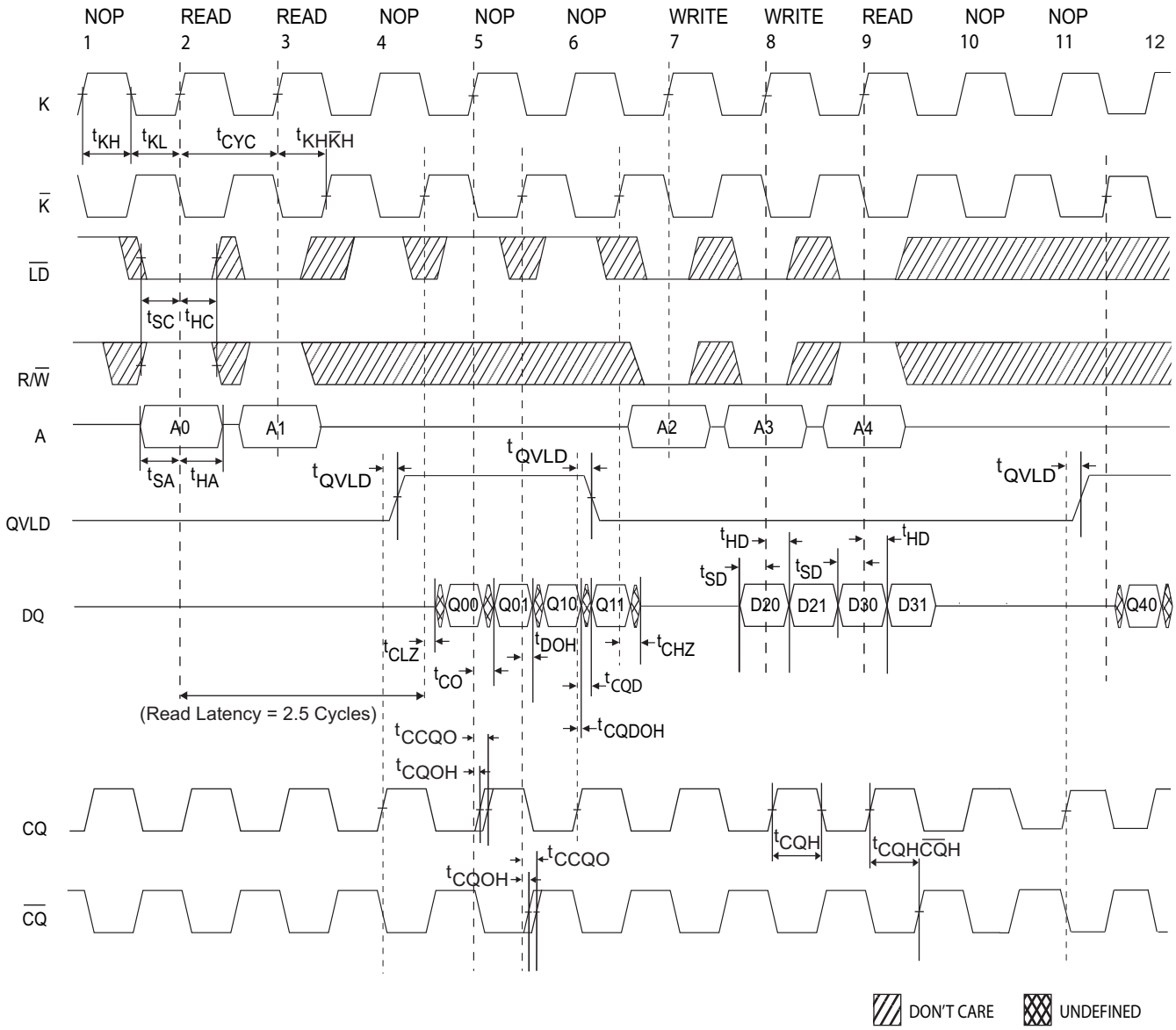


[+] Feedback

## Switching Waveforms

### Read/Write/Deselect Sequence [35, 36, 37]

**Figure 5. Waveform for 2.5 Cycle Read Latency**




**Notes**
35. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
36. Outputs are disabled (High Z) one clock cycle after a NOP.
37. In this example, if address A4 = A3, then data Q40 = D30 and Q41 = D31. Write data is forwarded immediately as read results. This note applies to the whole diagram.



[+] Feedback

## Ordering Information

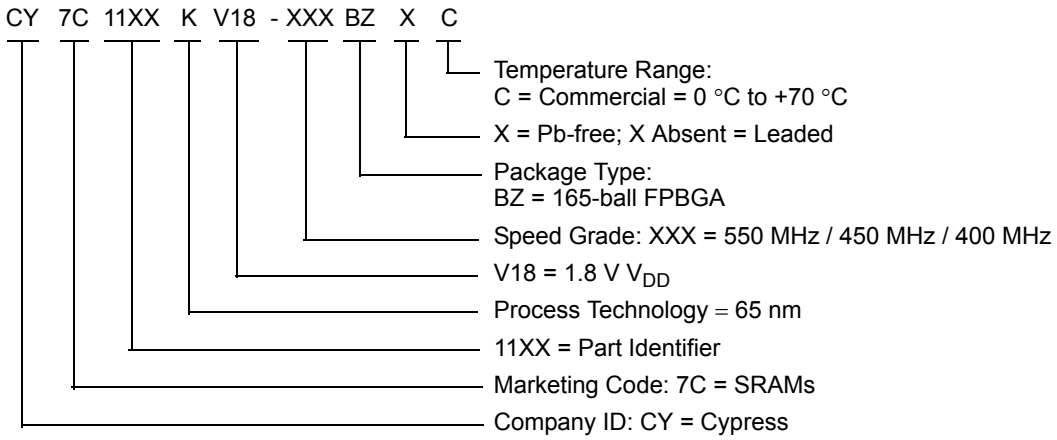
The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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**Table 2. Ordering Information**

| Speed (MHz) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 400 | CY7C1168KV18-400BZC | 51-85180 | 165-ball fine pitch ball grid array (13 x 15 x 1.4 mm) | Commercial |
| | CY7C1168KV18-400BZXC | | 165-ball fine pitch ball grid array (13 x 15 x 1.4 mm) Pb-free | |
| | CY7C1170KV18-400BZC | | 165-ball fine pitch ball grid array (13 x 15 x 1.4 mm) | |
| | CY7C1170KV18-400BZXC | | 165-ball fine pitch ball grid array (13 x 15 x 1.4 mm) Pb-free | |
| 450 | CY7C1168KV18-450BZC | 51-85180 | 165-ball fine pitch ball grid array (13 x 15 x 1.4 mm) | Commercial |
| | CY7C1168KV18-450BZXC | | 165-ball fine pitch ball grid array (13 x 15 x 1.4 mm) Pb-free | |
| | CY7C1170KV18-450BZXC | | 165-ball fine pitch ball grid array (13 x 15 x 1.4 mm) Pb-free | |
| 550 | CY7C1168KV18-550BZXC | 51-85180 | 165-ball fine pitch ball grid array (13 x 15 x 1.4 mm) Pb-free | Commercial |
| | CY7C1170KV18-550BZC | | 165-ball fine pitch ball grid array (13 x 15 x 1.4 mm) | |

### Ordering Code Definitions

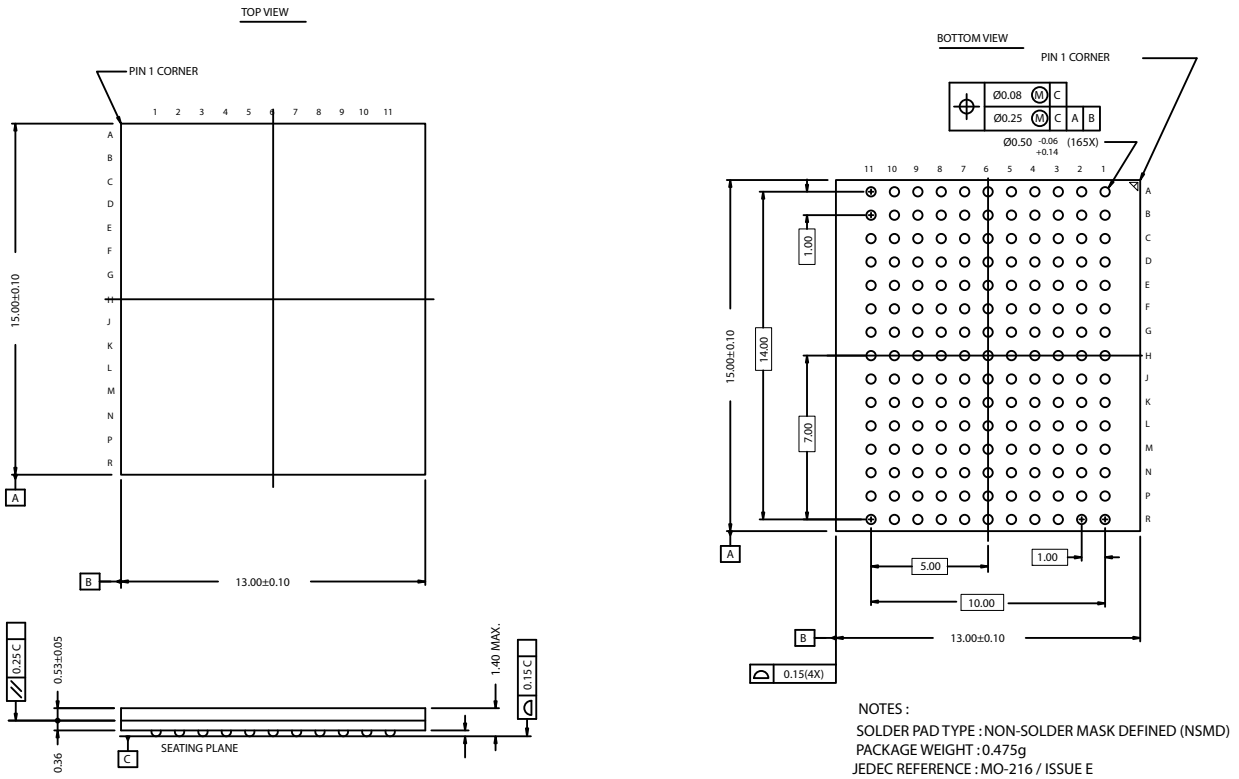





[+] Feedback

## Package Diagram

**Figure 6. 165-Ball FBGA (13 x 15 x 1.4 mm), 51-85180**






[+] Feedback

## Acronyms

| Acronym | Description |
|---|---|
| CE | chip enable |
| CEN | clock enable |
| FPBGA | fine-pitch ball grid array |
| HSTL | high-speed transceiver logic |
| I/O | input/output |
| JTAG | joint test action group |
| LMBU | logical multiple bit upset |
| LSBU | logical single bit upset |
| OE | output enable |
| PLL | phase locked loop |
| QDR | quad data rate |
| SEL | single event latch up |
| TCK | test clock |
| TMS | test mode select |
| TDI | test data-in |
| TDO | test data-out |
| TQFP | thin quad flat pack |
| WE | write enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| ns | nano seconds |
| V | Volts |
| µA | micro Amperes |
| mA | milli Amperes |
| ms | milli seconds |
| MHz | Mega Hertz |
| pF | pico Farad |
| W | Watts |
| °C | degree Celcius |



[+] Feedback

## Document History Page

| Document Title: CY7C1166KV18, CY7C1177KV18, CY7C1168KV18, CY7C1170KV18 18-Mbit DDR II+ SRAM Two-Word Burst Architecture (2.5 Cycle Read Latency)<br>Document Number: 001-58913 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 2864051 | VKN | 01/22/2010 | New data sheet |
| *A | 3083280 | NJY | 11/10/2010 | Changed status from Preliminary to Final.<br>Updated Ordering Information.<br>Added Ordering Code Definitions.<br>Added Acronyms and Document Conventions. |
| *B | 3146217 | SRIH | 01/18/2011 | Corrected the revision version error from 'B' to 'A' in the DHP. |
| *C | 3181270 | SHTC | 02/24/2011 | Added parts CY7C1168KV18-400BZC, CY7C1168KV18-450BZC, CY7C1168KV18-450BZXC, CY7C1170KV18-400BZC, and CY7C1170KV18-400BZXC in Ordering Information |

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