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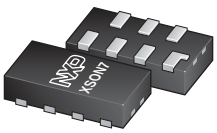


PUSB3AB6

ESD protection for ultra high-speed interfaces

Rev. 1 — 3 March 2015 Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as SuperSpeed and Hi-Speed USB combination, Secure Digital (SD) card 3.0 and Thunderbolt interfaces against ElectroStatic Discharge (ESD).

The device includes six high-level ESD protection diode structures. They protect sensitive transmitters and receivers for ultra high-speed signal lines. The device is encapsulated in a leadless ultra small DFN2111-7 (SOT1358-1) Surface-Mounted Device (SMD) plastic package.

All signal lines are protected by a special diode configuration offering snapback ultra low line capacitance of only 0.15 pF. These diodes utilize a snapback structure in order to provide protection to downstream components from ESD voltages up to ±15 kV contact exceeding IEC 61000-4-2, level 4.

1.2 Features and benefits

- System-level ESD protection for USB 2.0 and USB 3.1 combination, SD card 3.0 and Thunderbolt interfaces
- Supports SuperSpeed USB 3.1 at 10 Gbps
- Line capacitance of only 0.15 pF for each channel
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±15 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Design-friendly pass-through signal routing

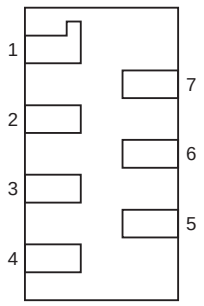
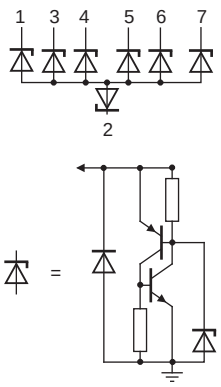
1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- Portable and wearable devices
- Smartphones, tablet computers
- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles

2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	 Transparent top view	
2	GND	ground [1]		
3	CH2	channel 2 ESD protection		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	CH5	channel 5 ESD protection		
7	CH6	channel 6 ESD protection		

[1] Any pin can be chosen for ground connection; one pin must be connected to ground.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3AB6	DFN2111-7	plastic extremely thin small outline package; no leads; 7 terminals; body 1.1 × 2.1 × 0.5 mm	SOT1358-1

4. Marking

Table 3. Marking codes

Type number	Marking code
PUSB3AB6	AB

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5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		–3.3	+3.3	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4 [1]			
		contact discharge	–15	+15	kV
		air discharge	–15	+15	kV
I_{PPM}	rated peak pulse current	t_p = 8/20 μs	–7	+7	A
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

[1] All pins to ground.

6. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_I = 1 mA	6	-	-	V
I_{LR}	reverse leakage current	per channel; V_I = 5 V	-	1	100	nA
C_{line}	line capacitance	f = 1 MHz; V_I = 1.5 V [1]	-	0.15	0.20	pF
r_{dyn}	dynamic resistance	TLP [3]				
		positive transient	-	0.4	-	Ω
		negative transient	-	0.4	-	Ω
V_{sbck}	snapback voltage	I_I = 1 A TLP; 100/10 ns	-	3	-	V
V_{CL}	clamping voltage	I_{PP} = 5 A; positive transient [2]	-	6	-	V
		I_{PP} = –5 A; negative transient [2]	-	–6	-	V

[1] This parameter is guaranteed by design.

[2] According to IEC 61000-4-5 (pulse time t_p = 8/20 μs).

[3] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 80 ns.

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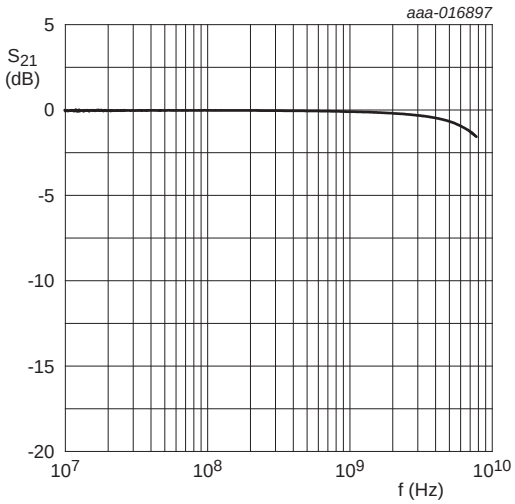
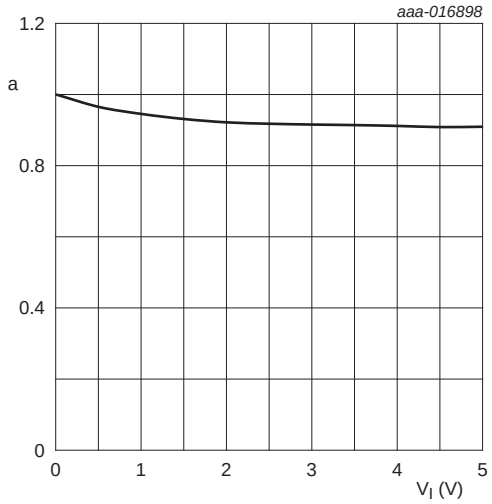


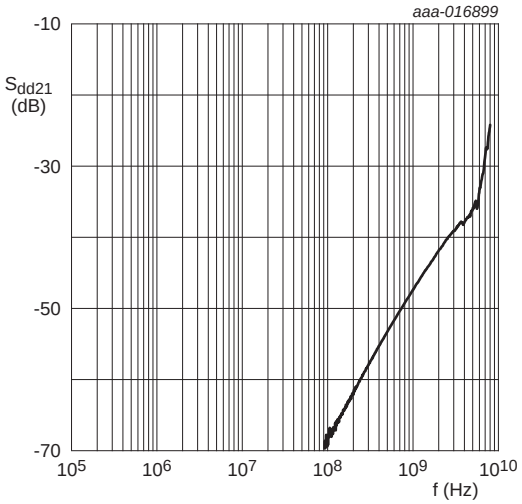
differential mode

Fig 1. Insertion loss; typical values



$$a = \frac{C_{line}}{C_{line(V_I = 0\ V)}}$$

Fig 2. Relative capacitance as a function of input voltage; typical values



Sdd21 normalized to 100 Ω

Fig 3. Crosstalk; typical values

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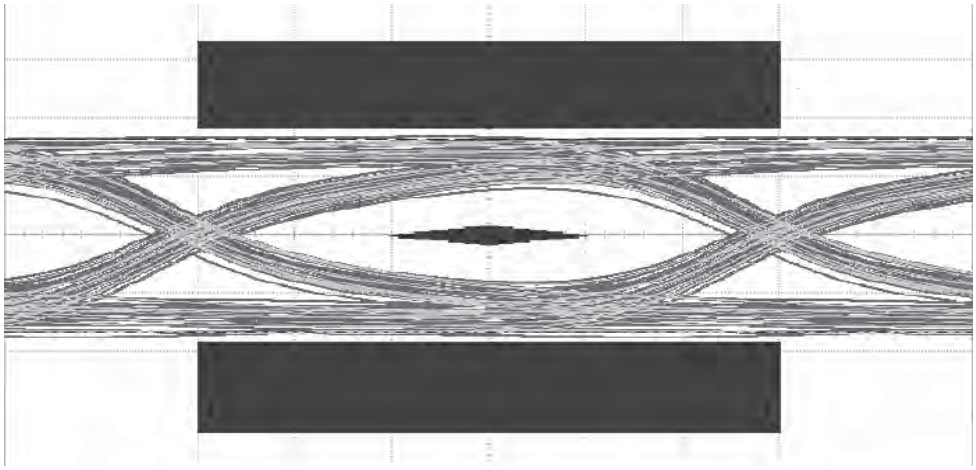


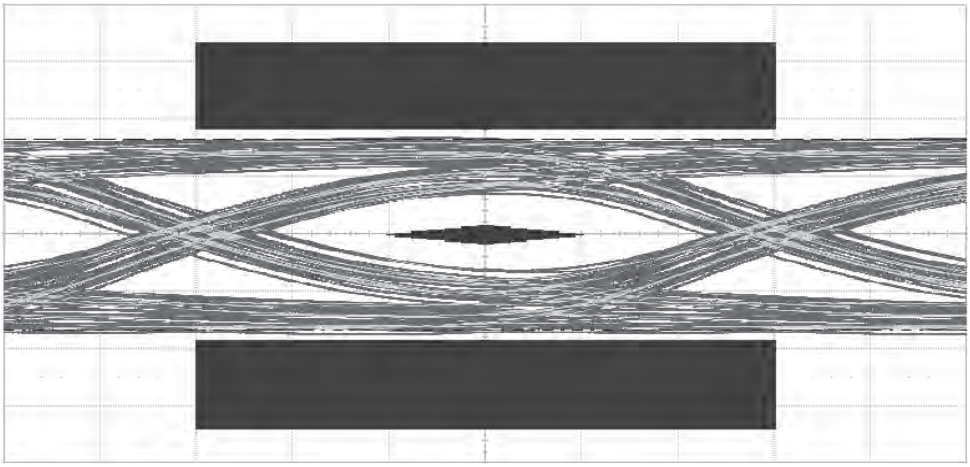
aaa-016900

Data rate: 10 Gbit/s

Vertical scale: 325 mV/div

Horizontal scale: 16.7 ps/div

Fig 4. USB 3.1 eye diagram, Printed-Circuit Board (PCB) with PUSB3AB6



aaa-016901

Data rate: 10 Gbit/s

Vertical scale: 325 mV/div

Horizontal scale: 16.7 ps/div

Fig 5. USB 3.1 eye diagram, PCB without PUSB3AB6 (reference)

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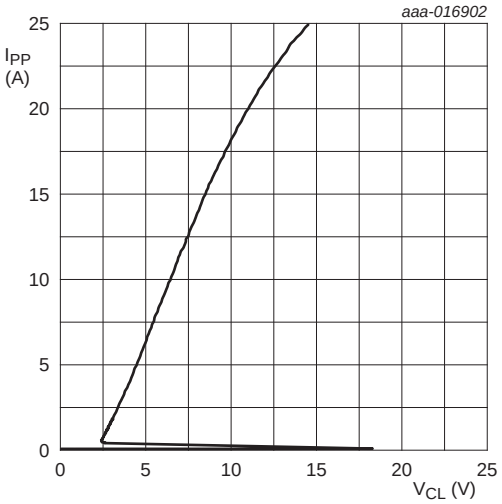
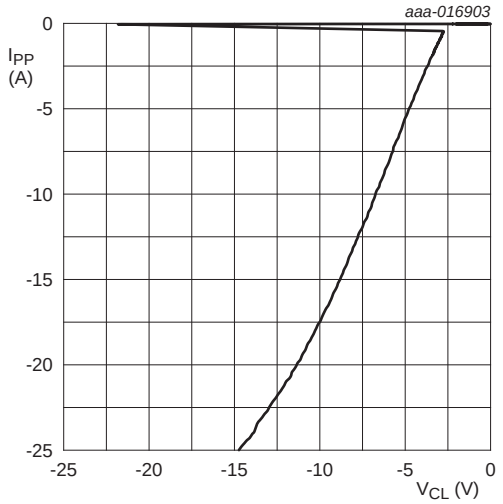


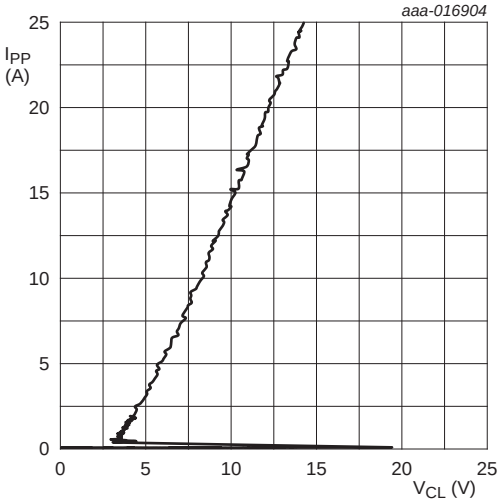
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 6. Dynamic resistance with positive clamping; typical values



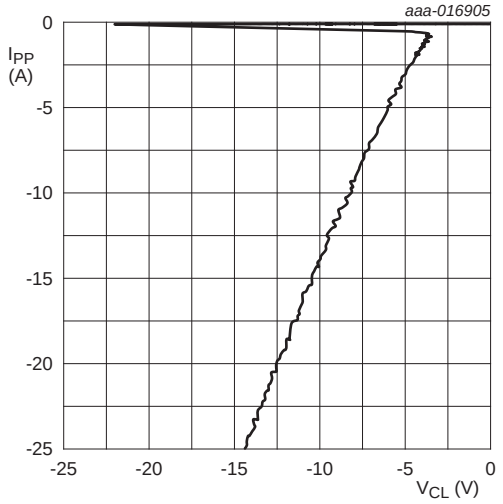
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 7. Dynamic resistance with negative clamping; typical values



t_p = 5 ns; Very-Fast Transmission-Line Pulse (VF-TLP)

Fig 8. Dynamic resistance with positive clamping; typical values



t_p = 5 ns; Very-Fast Transmission-Line Pulse (VF-TLP)

Fig 9. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snapback behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snapback state after exceeding breakdown voltage (due to an ESD pulse for instance).

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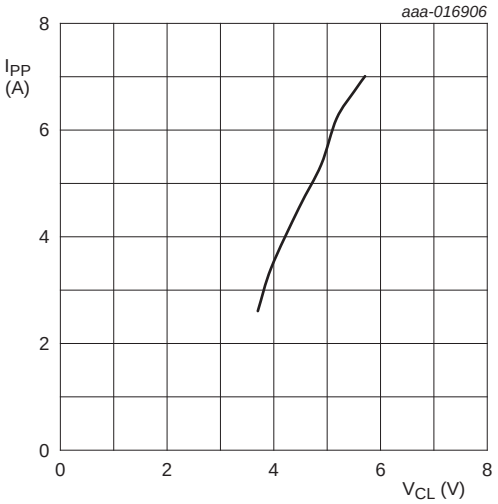
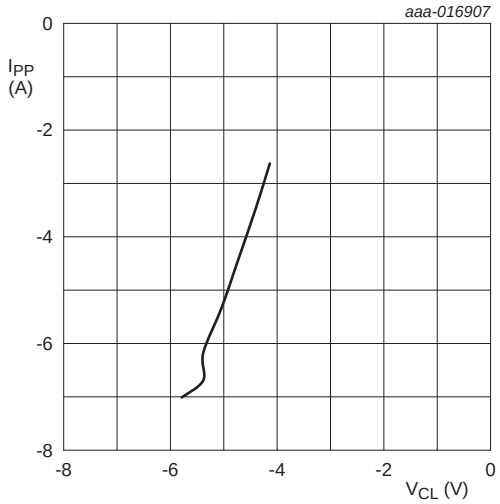


IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 10. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 11. Dynamic resistance with negative clamping; typical values

7. Package outline

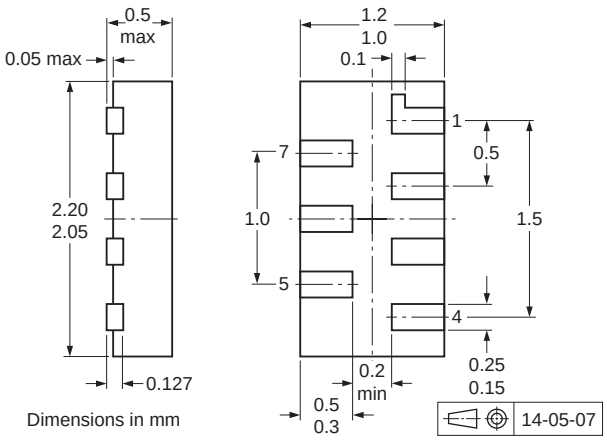


Fig 12. Package outline DFN2111-7 (SOT1358-1)

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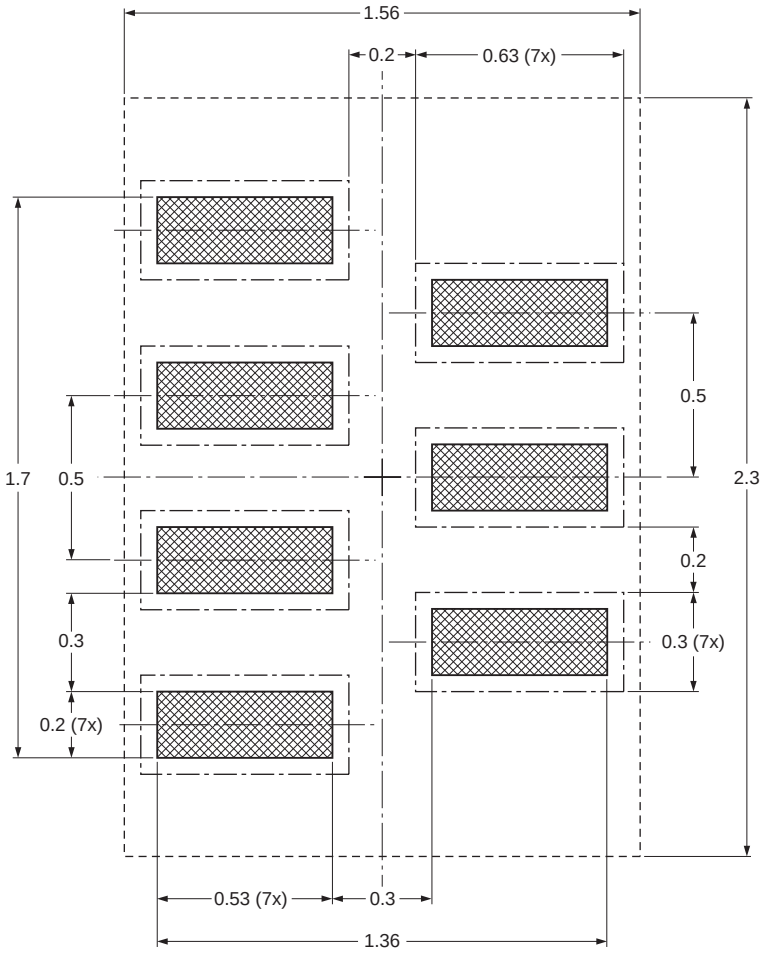
8. Soldering

Footprint information for reflow soldering of DFN2111-7 (SOT1358-1) package **SOT1358-1**



occupied area

solder resist

solder lands

solder paste

Dimensions in mm

Issue date ~~14-04-24~~ 14-05-07

sot1358-1_fr

Fig 13. Reflow soldering footprint DFN2510A-10 (SOT1176-1)

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9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3AB6 v.1	20150303	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
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