

iC-LNB 18-BIT OPTO ENCODER WITH SPI AND SER/PAR INTERFACES

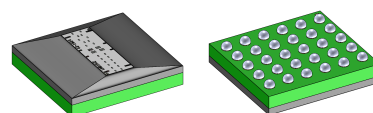
FEATURES

- System-on-chip design for excellent reliability
- Leading/trailing sampling of 10 binary tracks pitched at 400 μm
- Analog sine/cosine scanning with enlarged photodiodes, signal conditioning and fast 8-bit vector-tracking interpolation
- Absolute singleturn resolution of up to 18 bit
- Unique FlexCount[®] circuit: freely selectable resolution for absolute and incremental data
- Incremental quadrature outputs with 1 to 65,536 CPR and programmable index signal
- LED illumination control by 50 mA high-side current source ($\sin^2+\cos^2$ or sum control modes)
- Alarm indication for configuration or illumination error
- Permanent RAM monitoring by parity bits
- 3.3 V-compatible SPI and I/O ports for configuration and data
- Serial data readout in 1 μs cycles at 16 MHz clock frequency
- Parallel position data output for 16 bit
- Operation at 4 V to 5.5 V within -40°C to 110°C
- 30-pin optoBGA or 38-pin optoQFN package for SMT
- Illumination: iC-SN85 BLCC SN1C (850 nm encoder LED)
- Code discs: LNB1S 42-1024 (1024 PPR, \varnothing 42 mm/18 mm), LNB4S 26-1024 (1024 PPR, \varnothing 26.0 mm/9.6 mm)

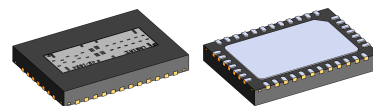
APPLICATIONS

- Optical position sensors
- Linear scales
- Absolute rotary encoders
- Programmable incremental encoders
- Motor feedback systems

PACKAGES

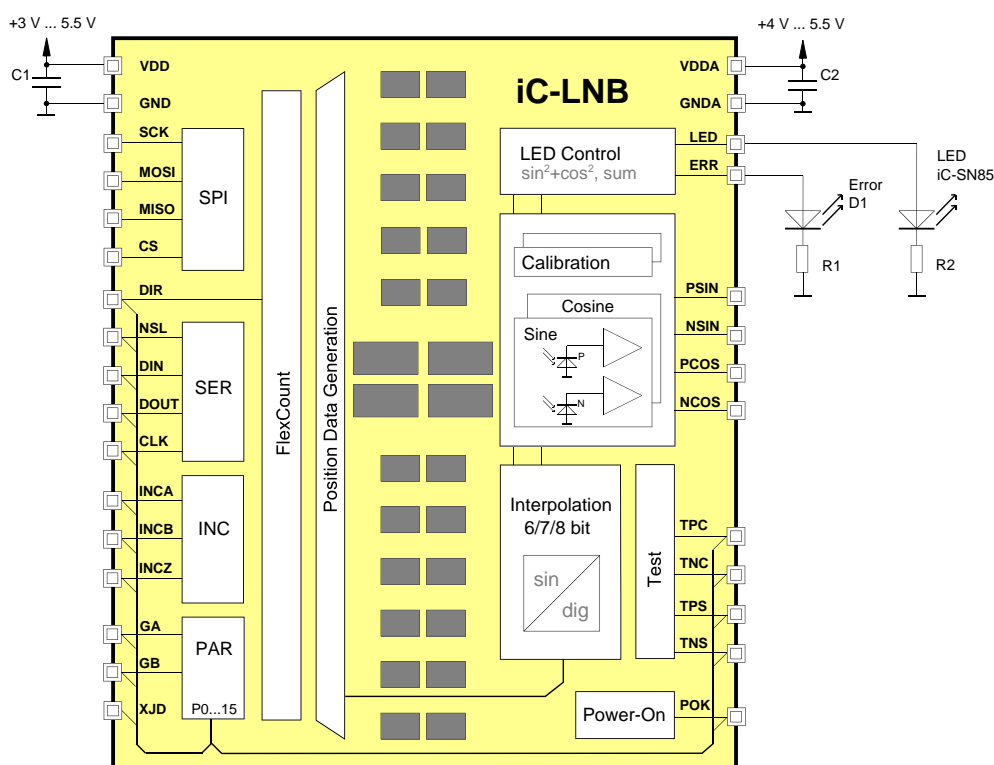


30-pin optoBGA
7.6 mm x 7.1 mm x 1.6 mm



38-pin optoQFN
7.0 mm x 5.0 mm x 0.9 mm

BLOCK DIAGRAM



DESCRIPTION

iC-LNB is an optoelectronic encoder IC for absolute linear and angle measuring systems, such as glass scales and encoders. Photodiodes, amplifiers, and comparators, the entire signal conditioning unit, and interfaces for position data output have been monolithically integrated into the device.

An integrated LED current control with a driver stage allows a transmitting LED to be directly connected (e.g. iC-SN85). The optical receive power is kept constant by the control unit, regardless of temperature and aging effects. The receive power setpoint can be programmed. Should the LED current control exceed its operating range, this is indicated at the error message output (end-of-life alarm at pin ERR).

The photocurrent offset and photocurrent amplitude of the analog sine/cosine signals can be calibrated.

These calibrated voltage signals are lead out to pins PSIN, NSIN, PCOS, and NCOS and are used by the integrated 8-bit vector-tracking interpolation circuit.

iC-LNB synchronizes the interpolator and singleturn data to form a contiguous Gray-coded position data word. 16 parallel ports, a scalable shift-register, the SPI interface, as well as incremental A/B/Z signals are available for data output. By help of the unique 'FlexCount' circuit any angle resolution between 4 to 2^{18} angle steps per revolution can be preset for the incremental signals and the absolute position value.

After startup iC-LNB is configured using the SPI interface. To make connection to a 3.3V microcontroller easier, all digital I/O ports, including the SPI, can be run on 3.3V.

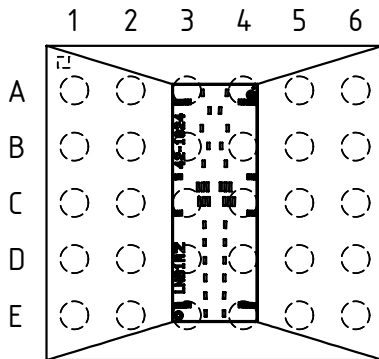
CONTENTS

PACKAGING INFORMATION	4	Radial adjustment to code disc	24
PIN CONFIGURATION		SIGNAL CONDITIONING	25
oBGA LNB2C		Gain	25
(7.6 mm x 7.1 mm x 1.6 mm)	4	Sine calibration	25
PIN CONFIGURATION		Cosine calibration	25
oQFN38-7x5		Square control	26
(7.0 mm x 5.0 mm x 0.9 mm)		LED POWER CONTROL	27
(in qualification)	5	Error monitoring	27
PAD LAYOUT	6	INTERPOLATOR	27
PACKAGE DIMENSIONS oQFN38-7x5	7	Interpolator resolution	27
		Interpolator filter	27
ABSOLUTE MAXIMUM RATINGS	8	FLEXCOUNT®	28
THERMAL DATA	8	Enable/disable	28
ELECTRICAL CHARACTERISTICS	9	Resolution	28
OPERATING CONDITIONS: SPI Interface	14	Reset	28
OPERATING CONDITIONS: Shift Register	15	Hysteresis	29
CONFIGURATION PARAMETERS	16	Incremental outputs	29
PROGRAMMING iC-LNB	17	Position offset	29
Address range	17	INCREMENTAL OUTPUT	30
RAM monitoring (parity check)	17	Selecting the output	30
Reset values	18	Tristate	30
Programming sequence	18	SHIFT REGISTER OUTPUT	30
OPERATING MODES	19	PARALLEL ENCODER MODE	31
SPI INTERFACE	20	ALARM OUTPUT	32
General protocol description	20	OSCILLATOR	32
OPCODE description	20	TEST FUNCTIONS	33
GRAY-CODE OUTPUTS	23	DESIGN REVIEW: Notes On Chip Functions	34
ADJUSTMENT	23		
Tilt angle	23		
Example: LNB1S 42-1024	23		

PACKAGING INFORMATION

PIN CONFIGURATION

oBGA LNB2C
(7.6 mm x 7.1 mm x 1.6 mm)



PIN FUNCTIONS

No.	Name	Function
A1	SCK	SPI Clock Input
A2	VDD	+3 V ... +5.5 V I/O Ports Supply Voltage
A3	GND	I/O Ports Ground
A4	LED	LED Highside Current Source
A5	VDDA	+4 V ... +5.5 V Supply Voltage
A6	GND A	Ground
B1	CS	SPI Chip Select Input
B2	MISO	SPI Data Output
B3	MOSI	SPI Data Input
B4	PCOS	Analog Voltage Output PCOS
B5	NSIN	Analog Voltage Output NSIN
B6	PSIN	Analog Voltage Output PSIN

PIN FUNCTIONS

No.	Name	Function
C1	DIR	Code Inversion Input / Parallel Output Bit 13
C2	TNS	Test Input NSIN / Parallel Output Bit 14
C3	TNC	Test Input NCOS / Parallel Output Bit 15
C4	TPS	Test Input PSIN / Parallel Output Bit 1
C5	TPC	Test Input PCOS / Parallel Output Bit 0
C6	NCOS	Analog Voltage Output NCOS
D1	DOUT	Shift Register Data Output / Parallel Output Bit 10
D2	DIN	Shift Register Data Input / Parallel Output Bit 11
D3	NSL	Shift Register Load Input (low active) / Parallel Output Bit 12
D4	INCB	Incremental Output B / Parallel Output Bit 3
D5	INCA	Incremental Output A / Parallel Output Bit 2
D6	ERR	Error Message Output (high active)
E1	GB	Gray-code Output B (MSB-1) / Parallel Output Bit 7
E2	GA	Gray-code Output A (MSB) / Parallel Output Bit 8
E3	CLK	Shift Register Clock Input / Parallel Output Bit 9
E4	XJD	Adjustment Signal / Parallel Output Bit 6
E5	POK	Power Ok Indication / Parallel Output Bit 5
E6	INCZ	Incremental Output Z / Parallel Output Bit 4

Wiring unused input pins can be recommended, especially for pins DIR, TPS, TNS, TPC, TNC (e.g. via 10 kΩ to GNDA).

For dimensional specifications refer to the package datasheet iC-LNB oBGA LNB2C, available separately.

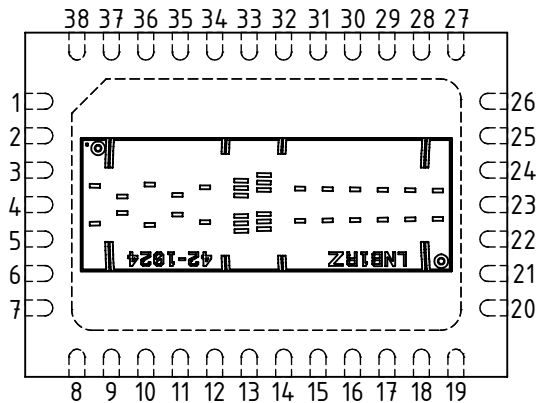
iC-LNB 18-BIT OPTO ENCODER WITH SPI AND SER/PAR INTERFACES



Rev A1, Page 5/35

PIN CONFIGURATION

oQFN38-7x5 (7.0 mm x 5.0 mm x 0.9 mm)
(in qualification)



PIN FUNCTIONS

No.	Name	Function
1	GNDA	Ground
2-6	n.c.	
7	GND	I/O Ports Ground
8	VDD	+3 V ... +5.5 V I/O Ports Supply Voltage
9	SCK	SPI Clock Input
10	MOSI	SPI Data Input
11	MISO	SPI Data Output
12	CS	SPI Chip Select Input
13	TNC	Test Input NCOS / Parallel Output Bit 15
14	TNS	Test Input NSIN / Parallel Output Bit 14
15	DIR	Code Inversion Input / Parallel Output Bit 13

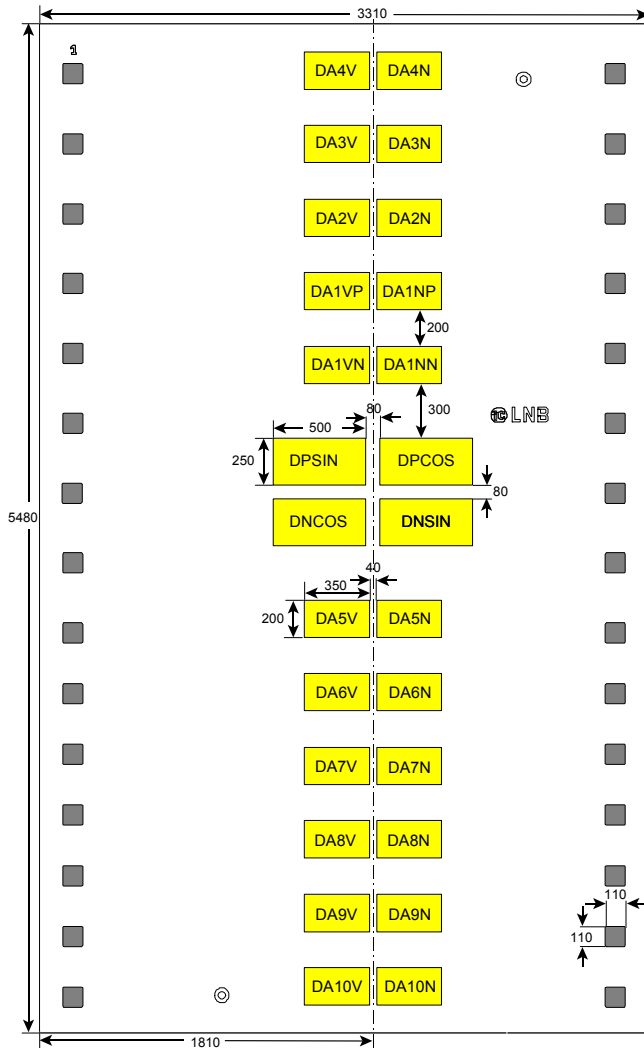
PIN FUNCTIONS

No.	Name	Function
16	NSL	Shift Register Load Input (low active) / Parallel Output Bit 12
17	DIN	Shift Register Data Input / Parallel Output Bit 11
18	DOUT	Shift Register Data Output / Parallel Output Bit 10
19	CLK	Shift Register Clock Input / Parallel Output Bit 9
20	GB	Gray-code Output B (MSB-1) / Parallel Output Bit 7
21	GA	Gray-code Output A (MSB) / Parallel Output Bit 8
22-24	n.c.	
25	POK	Power Ok Indication/ Parallel Output Bit 5
26	XJD	Adjustment Signal / Parallel Output Bit 6
27	INCZ	Incremental Output Z / Parallel Output Bit 4
28	INCB	Incremental Output B / Parallel Output Bit 3
29	INCA	Incremental Output A / Parallel Output Bit 2
30	ERR	Error Message Output (high active)
31	TPS	Test Input PSIN / Parallel Output Bit 1
32	TPC	Test Input PCOS / Parallel Output Bit 0
33	NCOS	Analog Voltage Output NCOS
34	PCOS	Analog Voltage Output PCOS
35	NSIN	Analog Voltage Output NSIN
36	PSIN	Analog Voltage Output PSIN
37	LED	LED Highside Current Source
38	VDDA	+4 V ... +5.5 V Supply Voltage
	n.c.	pin not connected

Wiring unused input pins can be recommended, especially for pins DIR, TPS, TNS, TPC, TNC (e.g. via 10 kΩ to GNDA).

The *thermal pad* of the optoQFN package (bottom side) should be joined to an extended copper area which must have GNDA potential.

PAD LAYOUT



PAD FUNCTIONS

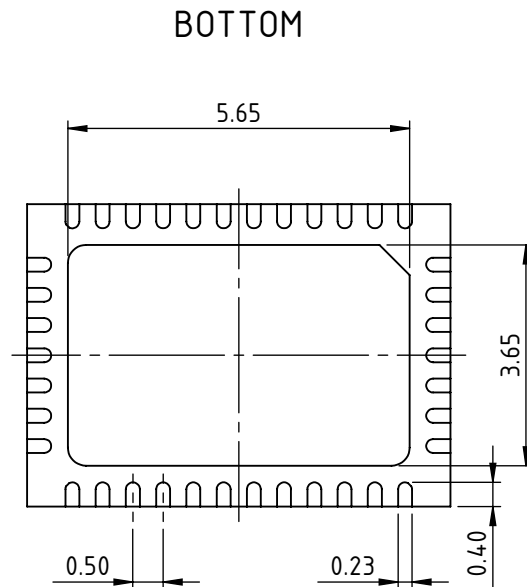
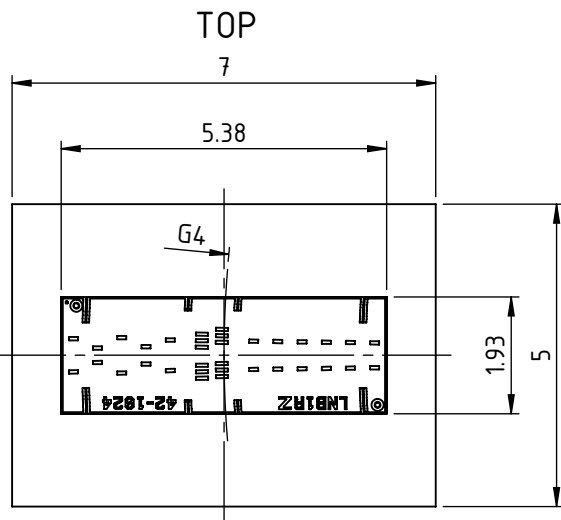
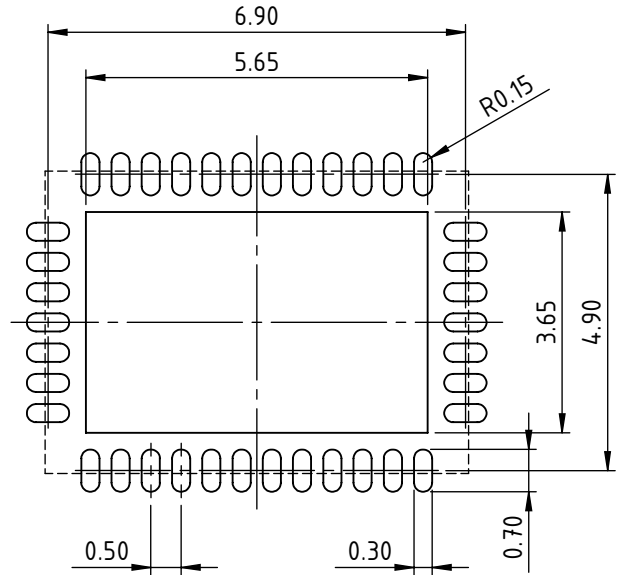
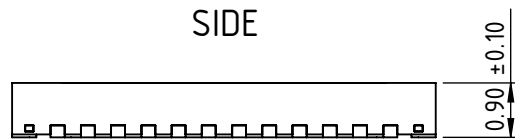
No. Name Function

No.	Name	Function
1	GND	I/O Ports Ground
2	VDD	+ 3 V ... +5.5 V I/O Ports Supply Voltage
3	SCK	SPI Clock Input
4	MOSI	SPI Data Input
5	MISO	SPI Data Output
6	CS	SPI Chip Select Input
7	TNC	Test Input NCOS / Parallel Output Bit 15
8	TNS	Test Input NSIN / Parallel Output Bit 14
9	DIR	Code Inversion Input / Parallel Output Bit 13
10	NSL	Shift Register Load Input (low active) / Parallel Output Bit 12
11	DIN	Shift Register Data Input / Parallel Output Bit 11
12	DOUT	Shift Register Data Output / Parallel Output Bit 10
13	CLK	Shift Register Clock Input / Parallel Output Bit 9
14	GA	Gray-code Output A (MSB) / Parallel Output Bit 8
15	GB	Gray-code Output B (MSB-1) / Parallel Output Bit 7
16	XJD	Adjustment Signal / Parallel Output Bit 6
17	POK	Power Ok Indication/ Parallel Output Bit 5
18	INCZ	Incremental Output Z / Parallel Output Bit 4
19	INCB	Incremental Output B / Parallel Output Bit 3
20	INCA	Incremental Output A / Parallel Output Bit 2
21	ERR	Error Message Output
22	TPS	Test Input PSIN / Parallel Output Bit 1
23	TPC	Test Input PCOS / Parallel Output Bit 0
24	NCOS	Analog Voltage Output NCOS
25	PCOS	Analog Voltage Output PCOS
26	NSIN	Analog Voltage Output NSIN
27	PSIN	Analog Voltage Output PSIN
28	LED	LED Highside Current Source
29	VDDA	+ 4 V ... +5.5 V Supply Voltage
30	GNDA	Ground

Wiring unused input pads can be recommended, especially for pins DIR, TPS, TNS, TPC, TNC (e.g. via 10 kΩ to GNDA).

PACKAGE DIMENSIONS oQFN38-7x5

RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
 Positional tolerance of reticle pattern: $\pm 90\mu\text{m}$ / $\pm 1.5^\circ$ (with respect to backside pad).
 G4: radius of chip center (refer to the relevant encoder disc and code description).
 Maximum molding excess $+20\mu\text{m}$ / $-75\mu\text{m}$ versus surface of glass/reticle.

iC-LNB 18-BIT OPTO ENCODER WITH SPI AND SER/PAR INTERFACES



Rev A1, Page 8/35

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply permissible operating conditions; functional operation is not guaranteed. Exceeding these ratings may damage the device.

Item No.	Symbol	Parameter	Conditions			Unit
				Min.	Max.	
G001	VDDA	Voltage at VDDA		-0.3	6	V
G002	VDD	Voltage at VDD		-0.3	VDDA+0.3	V
G003	V(GND)	Voltage at GND		-0.3	0.3	V
G004	V()	Voltage at LED, PCOS, NCOS, PSIN, NSIN, TPC, TNC, TPS, TNS		-0.3	VDDA+0.3	V
G005	V()	Voltage at INCA, INCB, INCZ, ERR, DIR, CLK, DOUT, DIN, NSL, NCS, MOSI, MISO, SCK, POK, XJD, GA, GB		-0.3	VDD+0.3	V
G006	I(VDDA)	Current in VDDA		-100	100	mA
G007	I(VDD)	Current in VDD		-50	50	mA
G008	I(GND)	Current in GND		-20	20	mA
G009	I(LED)	Current in LED		-100	20	mA
G010	I()	Current in INCA, INCB, INCZ, ERR, DIR, CLK, DOUT, DIN, NSL, NCS, MOSI, MISO, SCK, POK, XJD, GA, GB, TPC, TNC, TPS, TNS		-35	35	mA
G011	I()	Current in PCOS, NCOS, PSIN, NSIN		-35	35	mA
G012	Vd()	ESD Susceptibility at all pins	HBM 100pF discharged through 1.5 kΩ		2	kV
G013	Tj	Junction Temperature		-40	125	°C
G014	Ts	Chip Storage Temperature		-40	125	°C

THERMAL DATA

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
T01	Ta	Operating Ambient Temperature Range	packages oBGA LNB2C, oQFN38-7x5	-40		110	°C
T02	Ts	Permissible Storage Temperature Range	packages oBGA LNB2C, oQFN38-7x5	-40		110	°C
T03	Tpk	Soldering Peak Temperature	package oBGA LSH2C tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering TOL (time on label) 8 h; Please refer to customer information file No. 7 for details.			245 230	°C °C
T04	Tpk	Soldering Peak Temperature	package oQFN38-7x5 tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering MSL 5A (max. floor life 24 h at 30 °C and 60% RH); Please refer to customer information file No. 7 for details.			245 230	°C °C

All voltages are referenced to ground (GNDA) unless otherwise stated.

All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

iC-LNB 18-BIT OPTO ENCODER WITH SPI AND SER/PAR INTERFACES



Rev A1, Page 9/35

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Total Device							
001	VDDA	Permissible Supply Voltage		4	5	5.5	V
002	VDD	Permissible I/O Supply Voltage	$VDD \leq VDDA$	3	5	5.5	V
003	VDDA, VDD	Permissible Supply Voltage Ripple	at 150 kHz		10		mV
004	I(VDDA), I(VDD)	Supply Current in VDDA and VDD (sum)	without currents I(LED) and I(ERR), Tj = 27 °C		25	40	mA
005	Vcz()hi	Clamp Voltage hi at all Pins	I() = 4 mA			11	V
006	Vc()hi	Clamp Voltage hi at CLK, DIN, NSL, INCA, INCB, INCZ, ERR, DIR, MISO, DOUT, POK, XJD, GA, GB, TPS, TNS, TPC, TNC	$Vc()hi = V() - V(VDD)$, I() = 4 mA	0.3		1.2	V
007	Vc()hi	Clamp Voltage hi at CS, MOSI, SCK	$Vc()hi = V() - V(VDD)$, I() = 4 mA	1.2		2.2	V
008	Vc()lo	Clamp Voltage lo at all Pins	I() = -4 mA	-1.2		-0.3	V
Photodiodes							
101	Se(λ)	Spectral Application Range	$Se(\lambda) = 0.25 \times S(\lambda)_{max}$	400		950	nm
102	S(λ)max	Spectral Sensitivity	$\lambda = 690 \text{ nm}$ $\lambda = 850 \text{ nm}$		0.45 0.30		A/W A/W
103	Aph()	Radiant Sensitive Area DPSIN, DNSIN, DPCOS, DNCOS	0.5 mm x 0.25 mm		0.125		mm ²
104	Aph()	Radiant Sensitive Area Digital DA1VP, DA1VN, DA1NP, DA1NN, DA2V ... DA10V, DA2N ... DA10N	0.35 mm x 0.2 mm		0.07		mm ²
Photocurrent Amplifier							
201	Iph()	Permissible Photocurrent Operating Range		0		200	nA
202	Z()	Equivalent Transimpedance Gain	$Z() = Vout() / Iph()$	1.8	3.0	4.2	M Ω
203	$\Delta Z()$ pn	Transimpedance Gain Matching of an Amplifier Pair	P-channel versus corresponding N-channel	-0.2		0.2	%
204	fhc()	Upper Cut-off Frequency (-3 dB)	without LED current control	120	300	500	kHz
205	VR()	Ratio of Reference Voltage Digital Tracks (Vcomp) to Sum of Digital Track 1	$VR() = \frac{V_{comp}}{VA1VP + VA1VN + VA1NP + VA1NN}$		0.25		
206	Hys()	Hysteresis Digital Tracks		5	15	25	mV
207	GR()	Coarse Gain Range Analog Track	GR = 0x00 GR = 0x01 GR = 0x02 GR = 0x03		1 1.33 1.6 2		
208	Vref	Reference Voltage of Photocurrent Amplifiers		0.6	0.8	1	V
209	$\Delta Vd()$ sc	Analog Track Dark Signal Voltage versus Vref	$\Delta Vd()_{sc} = V() - Vref$	-20		20	mV
210	$\Delta Vd()$ dig	Digital Tracks Dark Signal Voltage versus Vref	$\Delta Vd()_{dig} = V() - Vref$	-35		35	mV
Signal Conditioning Sin/Cos							
301	Gmin	Adjustable Minimum Gain	GS, GC = 0x00		1		
302	Gmax	Adjustable Maximum Gain	GS, GC = 0x3F		2		
303	ΔG diff	Differential Gain Calibration Accuracy	calibration range 6 bit	-0.5		0.5	LSB
304	Omin	Offset Calibration Min	OSP, OSN, OCP, OCN = 0x00	43	45	47	%VDDA
305	Omax	Offset Calibration Max	OSP, OSN, OCP, OCN = 0x7F	53	55	57	%VDDA
306	ΔO diff	Differential Offset Calibration Accuracy	calibration range 7 bit	0.02	0.08	0.12	%VDDA

iC-LNB 18-BIT OPTO ENCODER WITH SPI AND SER/PAR INTERFACES



Rev A1, Page 10/35

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Output Voltage PSIN, NSIN, PCOS, NCOS							
401	Vdc()	DC-Voltage at all Outputs	Offset adjusted to VDDAH	47	50	53	%VDDA
402	Vpk()	Permissible Signal Amplitude	DC level = VDDA/2		0.5	0.6	V
403	I(mx)	Permissible Output Current		-1		1	mA
404	Ri()	Output Resistor	I() = -1 ... 1 mA		75	200	Ω
LED Power Control LED, Error Message ERR							
501	I(mx)	Permissible LED Current at LED		-100		0	mA
502	Iop()	LED Current Control Range	ERRS (internal) = 0, V(LED) > Vs(LED)	-50		-1	mA
503	Vs()	Saturation Voltage at LED	Vs() = VDDA - V(LED); I() = -50 mA			1	V
504	tr()	Rise Time LED Current	I(LED): 0% → 90%		0.8	1.5	ms
505	tset()	Settling Time of LED Control Loop	amplitude at PSIN, NSIN, PCOS and NCOS from 50 % to 100 % of setpoint		300		μs
506	Vs()hi	Saturation Voltage hi at ERR	Vs()hi = VDD - V(ERR); VDD = 3 ... 4 V, I() = 1.5 mA VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
507	Isc()hi	Short-Circuit Current hi at ERR		-100		-1.5	mA
508	Vs()lo	Saturation Voltage lo at ERR	VDD = 3 ... 4 V, I() = 1.5 mA VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
509	Isc()lo	Short-Circuit Current lo at ERR		1.5		100	mA
Interpolator							
701	AAabs	Absolute Angular Position Accuracy	referenced to a Sin/Cos signal period RESIPO = 10 (6 bit interpolation) RESIPO = 01 (7 bit interpolation) RESIPO = 00 (8 bit interpolation)		2.8 1.4 0.7		DEG DEG DEG
702	AArel	Relative Angular Error	referenced to output period T, see Figure 1 RESIPO = 10 (6 bit interpolation) RESIPO = 01 (7 bit interpolation) RESIPO = 00 (8 bit interpolation)		1 2 4		% % %
703	AAhys	Angular Hysteresis	referenced to output period T, see Figure 1 RESIPO = 10 (6 bit interpolation) RESIPO = 01 (7 bit interpolation) RESIPO = 00 (8 bit interpolation)		2.8 1.4 0.7		DEG DEG DEG
704	tw()hi	Duty Cycle	referenced to output period T, see Figure 1 RESIPO ≠ 11 (interpolation active)		50		%
705	t _{AB}	Phase Shift A versus B	referenced to output period T, see Figure 1 RESIPO ≠ 11 (interpolation active)		25		%
706	f _{max}	Maximum Permissible Sin/Cos Frequency	RESIPO = 10 (6 bit interpolation) RESIPO = 01 (7 bit interpolation) RESIPO = 00 (8 bit interpolation)		f _{oipo} /64 f _{oipo} /128 f _{oipo} /256		kHz kHz kHz
FlexCount							
801	AArel _{Flex}	Additional Relative Angular Error of FlexCount	referenced to output period T, see Figure 1 all resolutions all binary resolutions maximum resolution - 4 for RESIPO = 00 (8 bit interpolation): RESSUB = 0x01387 (resolution 5 000) RESSUB = 0x04E1F (resolution 20 000) RESSUB = 0x09C3F (resolution 40 000) RESSUB = 0x3FFFB (resolution 2 ¹⁸ - 4)	0		25 0 25 0.48 1.92 3.85 25	% % % % % % %
802	tp _{Flex} ()	Propagation Delay FlexCount			1/f _{oflex}		
803	f _{max}	Maximum Permissible Sin/Cos Frequency	RESIPO = 10 (6 bit interpolation) RESIPO = 01 (7 bit interpolation) RESIPO = 00 (8 bit interpolation)		f _{oflex} /64 f _{oflex} /128 f _{oflex} /256		kHz kHz kHz

iC-LNB 18-BIT OPTO ENCODER WITH SPI AND SER/PAR INTERFACES



Rev A1, Page 11/35

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Incremental Outputs INCA, INCB, INCZ							
901	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); VDD = 3 ... 4 V, I() = 1.5 mA VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
902	Isc()hi	Short-Circuit Current hi		-100		-1.5	mA
903	Vs()lo	Saturation Voltage lo	VDD = 3 ... 4 V, I() = 1.5 mA VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
904	Isc()lo	Short-Circuit Current lo		1.5		100	mA
905	tr()	Rise Time	CL = 30 pF, V(): 10% → 90% VDD			30	ns
906	tf()	Fall Time	CL = 30 pF, V(): 90% → 10% VDD			30	ns
SPI Interface SCK, CS, MISO, MOSI							
A01	Vs()hi	Saturation Voltage hi at MISO	Vs()hi = VDD - V(); VDD = 3 ... 4 V, I() = 1.5 mA VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
A02	Isc()hi	Short-Circuit Current hi at MISO		-100		-1.5	mA
A03	Vs()lo	Saturation Voltage lo at MISO	VDD = 3 ... 4 V, I() = 1.5 mA VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
A04	Isc()lo	Short-Circuit Current lo at MISO		1.5		100	mA
A05	fin()	Permissible Clock Frequency at SCK				10	MHz
A06	Vt()hi	Threshold Voltage hi at SCK, CS, MOSI				2	V
A07	Vt()lo	Threshold Voltage lo at SCK, CS, MOSI		0.8			V
A08	Vt()hys	Hysteresis at SCK, CS, MOSI	Vt()hys = Vt()hi - Vt()lo	40	100		mV
A09	Ipu()	Pull-Up Current at SCK, MOSI	V() = 0 ... VDD - 1 V; VDD = 3 ... 4 V VDD = 4 ... 5.5 V	-65 -120	-25 -60	-5 -10	μA μA
A10	Vpu()	Pull-Up Voltage at SCK, MOSI	Vpu() = VDD - V(); VDD = 3 ... 4 V, I() = -3 μA VDD = 4 ... 5.5 V, I() = -5 μA			400	mV
A11	Ipd()	Pull-Down Current at CS	V() = 1 V ... VDD; VDD = 3 ... 4 V VDD = 4 ... 5.5 V	5 8	25 60	80 150	μA μA
A12	Vpd()	Pull-Down Voltage at CS	VDD = 3 ... 4 V, I() = 3 μA VDD = 4 ... 5.5 V, I() = 5 μA			400	mV
A13	tp1()	Propagation Delay: MISO hi after Falling Edge CS	see Figure 2		30		ns
A14	tp2()	Propagation Delay: MISO Stable after Clock Edge SCK	see Figure 2		30		ns

iC-LNB 18-BIT OPTO ENCODER WITH SPI AND SER/PAR INTERFACES



Rev A1, Page 12/35

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Shift Register CLK, NSL, DOUT, DIN							
B01	Vs()hi	Saturation Voltage hi at DOUT	Vs()hi = VDD - V(); VDD = 3 ... 4 V, I() = 1.5 mA VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
B02	Isc()hi	Short-Circuit Current hi at DOUT		-100		-1.5	mA
B03	Vs()lo	Saturation Voltage lo at DOUT	VDD = 3 ... 4 V, I() = 1.5 mA VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
B04	Isc()lo	Short-Circuit Current lo at DOUT		1.5		100	mA
B05	fin()	Permissible Clock Frequency at CLK				16	MHz
B06	Vt()hi	Threshold Voltage hi at CLK, NSL, DIN				2	V
B07	Vt()lo	Threshold Voltage lo at CLK, NSL, DIN		0.8			V
B08	Vt()hys	Hysteresis at CLK, NSL, DIN	Vt()hys = Vt()hi - Vt()lo	40	100		mV
B09	Ipu()	Pull-Up Current at CLK, NSL	V() = 0 ... VDD - 1 V; VDD = 3 ... 4 V VDD = 4 ... 5.5 V	-65 -120	-25 -60	-5 -10	μA μA
B10	Vpu()	Pull-Up Voltage at CLK, NSL	Vpu() = VDD - V(); VDD = 3 ... 4 V, I() = -3 μA VDD = 4 ... 5.5 V, I() = -5 μA			400	mV
B11	Ipd()	Pull-Down Current at DIN	V() = 1 V ... VDD; VDD = 3 ... 4 V VDD = 4 ... 5.5 V	5 8	25 60	80 150	μA μA
B12	Vpd()	Pull-Down Voltage at DIN	VDD = 3 ... 4 V, I() = 3 μA VDD = 4 ... 5.5 V, I() = 5 μA			400	mV
B13	tp3()	Propagation Delay: DOUT Idle State after Falling Edge NSL	see Figure 3		20		ns
B14	tp4()	Propagation Delay: DOUT stable after Clock Edge CLK	see Figure 3		20		ns
Parallel Outputs Bit 0 ... 15 (parameter EPG = 0x1)							
Pins: TNC, TNS, DIR, NSL, DIN, DOUT, CLK, GA, GB, XJD, POK, INCZ, INCB, INCA, TPS, TPC							
C01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); VDD = 3 ... 4 V, I() = 1.5 mA, VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
C02	Isc()hi	Short-Circuit Current hi		-100		-1.5	mA
C03	Vs()lo	Saturation Voltage lo	VDD = 3 ... 4 V, I() = 1.5 mA, VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
C04	Isc()lo	Short-Circuit Current lo		1.5		100	mA
C05	tr()	Rise Time	CL = 30 pF, V(): 10% → 90% VDD			30	ns
C06	tf()	Fall Time	CL = 30 pF, V(): 90% → 10% VDD			30	ns
Power-On-Reset POK							
D01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); VDD = 3 ... 4 V, I() = 1.5 mA, VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
D02	Isc()hi	Short-Circuit Current hi		-100		-1.5	mA
D03	Vs()lo	Saturation Voltage lo	VDD = 3 ... 4 V, I() = 1.5 mA, VDD = 4 ... 5.5 V, I() = 2.5 mA			400	mV
D04	Isc()lo	Short-Circuit Current lo		1.5		100	mA
D05	VDDAon	Turn-on Threshold VDDA, Power-on-release	increasing voltage at VDDA; POK: lo → hi	3.6	3.8	4.0	V
D06	VDDAoff	Turn-off Threshold VDDA, Power-down-reset	decreasing voltage at VDDA; EPG = 0, POK: hi → lo	3.3	3.5	3.7	V
D07	VDDAhys	Hysteresis	VDDAhys = VDDAon - VDDAoff	0.2	0.3		V
Code Inversion Input DIR							
E01	Vt()hi	Threshold Voltage hi				2	V

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
E02	Vt()lo	Threshold Voltage lo		0.8			V
E03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	40	100		mV
E04	Ipd()	Pull-Down Current	V() = 1 V ... VDD; VDD = 3 ... 4 V VDD = 4 ... 5.5 V	5 8	25 60	80 150	μ A μ A
E05	Vpd()	Pull-Down Voltage	VDD = 3 ... 4 V, I() = 3 μ A VDD = 4 ... 5.5 V, I() = 5 μ A			400	mV
Oscillator							
F01	f _{oipo}	Interpolator Oscillator Frequency	OSZC = 0x00 OSZC = 0x01 OSZC = 0x10 OSZC = 0x11		12.8 13.8 14.4 14.6		MHz MHz MHz MHz
F02	f _{oflex}	FlexCount Oscillator Frequency	OSZC = 0x00 OSZC = 0x01 OSZC = 0x10 OSZC = 0x11		12.8 13.8 14.4 14.6		MHz MHz MHz MHz

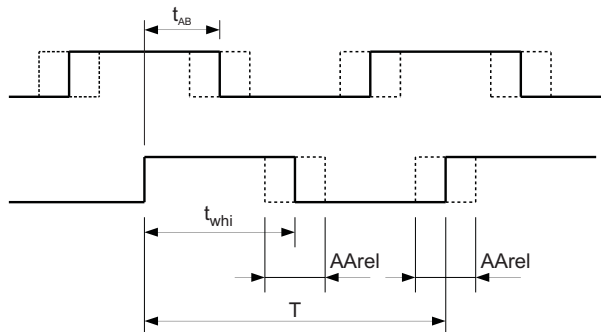


Figure 1: Definition of relative angle error

OPERATING CONDITIONS: SPI Interface

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min. Max.		Unit
				Min.	Max.	
I001	T_{SCK}	Permissible Clock Period	see Elec. Char. No.: A05	1/fin()		
I002	t_{CS}	Setup Time: CS hi before SCK hi \rightarrow lo		50		ns
I003	tp1	Propagation Delay: MISO hi after CS hi \rightarrow lo		Elec. Char. No.: A13		
I004	t_{IS}	Setup Time: MOSI stable before SCK lo \rightarrow hi		50		ns
I005	t_{SI}	Hold Time: MOSI stable after SCK lo \rightarrow hi		50		ns
I006	tp2	Propagation Delay: MISO stable after clock edge SCK		Elec. Char. No.: A14		
I007	t_{CC}	Wait Time: between CS hi \rightarrow lo and CS lo \rightarrow hi		500		ns

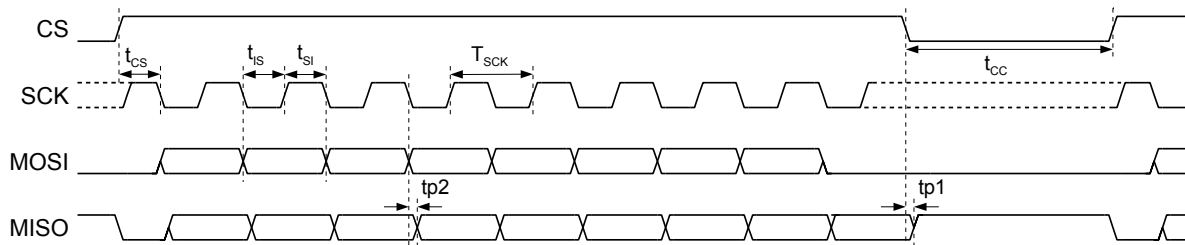


Figure 2: SPI timing

OPERATING CONDITIONS: Shift Register

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min. Max.		Unit
				Min.	Max.	
I101	T _{CLK}	Permissible Clock Period	see Elec. Char. No.: B05	1/fin()		
I102	t _{lo}	Hold Time Load Signal: NSL low before NSL edge lo → hi		30		ns
I103	tp3	Propagation Delay: DOUT (idle state) after NSL lo → hi		Elec. Char. No.: B13		
I104	tp4	Propagation Delay: DOUT stable after clock edge CLK		Elec. Char. No.: B14		
I105	t _{ic}	Setup Time: DIN stable before CLK lo → hi		30		ns
I106	t _{cl}	Hold Time: DIN stable after CLK lo → hi		30		ns
I107	t _{hi}	Preparation Time: NSL high before request of position data (CLK hi → lo)		30		ns

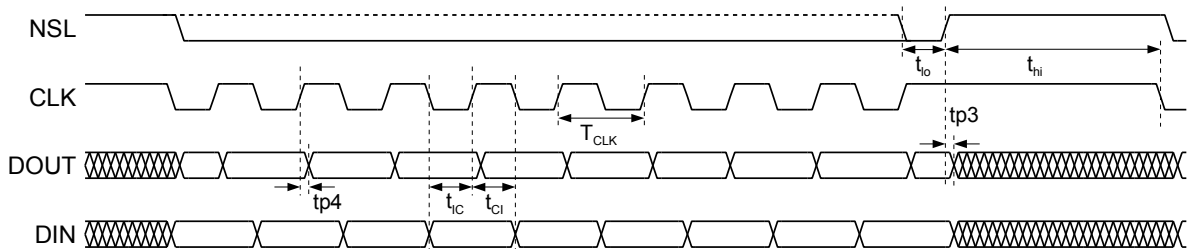


Figure 3: Shift register timing

CONFIGURATION PARAMETERS

Operating Modes	Page 19	FlexCount®	Page 28
EPG: Operating mode		NENFLEX: Enable/Disable	
SPI Interface	Page 20	SELABS: Absolute output options (SPI, SER, PAR)	
OPCODE: SPI instructions		RESSUB: Resolution - 1	
RACTIVE: Register communication activation		STOPFLEX: Stop/Reset FlexCount	
PACTIVE: Sensor data channel activation		POSOK: Position valid	
SVALID: Sensor data channel valid indication		NOUTLO: Setting FlexCount outputs to low	
STATUS: SPI status information		HYS: Hysteresis	
Signal Conditioning	Page 25	INVA: Output inversion INCA	
GR: Gain range		INVB: Output inversion INCB	
GS: SIN gain		INVZ: Output inversion INCZ	
OSP: PSIN offset		ZPOS: Position offset (binary)	
OSN: NSIN offset		Z90: Z pulse width	
GC: COS gain		Shift Register Output	Page 30
OCP: PCOS offset		NGRAY: Shift register output data format	
OCN: NCOS offset		RNF: Shift register idle output	
LED Power Control	Page 27	SRC: Shift register length	
LCMOD: LED Power control mode		DIR: Code inversion	
LCTYP: LED Power control type		Parallel Encoder Mode	Page 31
LCSET(5:0): LED Power control setpoint		EPG: Operating mode	
Interpolator	Page 27	Alarm Output	Page 32
RESIPO: Interpolator resolution		ERRS: LED range error (internal)	
ENIPO: Interpolator enable		ERRP: Parity error (internal)	
NENF: Interpolator filter		Oscillator	Page 32
Incremental output	Page 30	OSZC: Oscillator adjustment	
INC: Incremental output options		Test Functions	Page 33
TRIABZ: Incremental output tristate		TA: Test modes	
		TMUX: Test signal multiplexer	

PROGRAMMING iC-LNB

REGISTER MAP (RAM)								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Signal calibration								
0x00	P00	0	GS(5:0)					
0x01	P01	LCMOD	GC(5:0)					
0x02	P02	OSP(6:0)						
0x03	P03	OSN(6:0)						
0x04	P04	OCP(6:0)						
0x05	P05	OCN(6:0)						
LED power control								
0x06	P06	LCTYP	LCSET(5:0)					
Output configuration								
0x07	P07	NGRAY	DIR	EPG	OSZC(1:0)		GR(1:0)	
0x08	P08	INC(2:0)			RNF	SRC(2:0)		
Test functions								
0x09	P09	NENF	TA(1:0)		TMUX(3:0)			
FlexCount								
0x0A	P0A	HYS(6:0)						
0x0B	P0B	INVA	INVB	INVZ	TRIABZ	SELABS	NENFLEX	HYS(7)
0x0C	P0C	ZPOS(6:0)						
0x0D	P0D	ZPOS(13:7)						
0x0E	P0E	RESIPO(1:0)		Z90	ZPOS(17:14)			
0x0F	P0F	RESSUB(6:0)						
0x10	P10	RESSUB(13:7)						
0x11	P11	NOUTLO	STOPFLEX	ENIPO	RESSUB(17:14)			
Status (read only)								
0x12	0	0	0	0	0	ERRP	ERRS	POSOK

Table 6: Register layout

Address range

The addresses of iC-LNB available through the SPI interface range from addresses 0x00 to 0x12. As only the lower five bits of the address byte are evaluated, with addresses that are greater than 0x1F the device returns to address range 0x00-0x12.

RAM monitoring (parity check)

The configuration registers in the internal RAM are constantly monitored by a parity check. Bit 7 of each address is the parity bit (P00-P11) and is supplemented to an even number of ones. The unused bits are also monitored. A parity error (internal ERRP) is signaled at pin ERR (see the alarm output section).

Reset values

After power-on the registers are initialized as follows:

Address	Reset Value	Description
0x00-0x01	0xA0	Gain (GS, GC) = 1.408 LED control behavior (LCMOD) = 0
0x02-0x05	0xC0	Offset (OSP, OSN, OCP, OCN) = $0.5004 \cdot V_{DDA}$
0x06	0x60	LED control mode (LCTYP) = sum control, Set point (LCSET) = 0.23 V
0x07	0x09	Shift register output format (NGRAY) = GRAY, Direction (DIR) = CW, EPG = interface mode, Oscillator (OSZC) = 14.4MHz, Gain range (GR) = 1.33
0x08	0x18	Interpolator factor (INC) = x2, Idle state DOUT (RNF) = '1', Shift register (SRC) = 18 bit
0x09-0x0A	0x00	Test functions = 0, Hysteresis (HYS) = 0°
0x0B	0x8E	ABZ outputs (INVA/B/Z) = not inverted, ABZ outputs (TRIA/BZ) = tri-state, Shift register (SELABS) = max. resolution, FlexCount (NENFLEX) = disabled
0x0C-0x10	0x00	FlexCount parameters = 0
0x11	0xA0	FlexCount: Outputs (NOUTLO) = low, Reset (STOPFLEX) = stopped, Interpolator (ENIPO) = disabled

Table 7: Register reset values (RAM)

Programming sequence

Following iC-LNB's system reset (POK lo → hi) the internal RAM must be configured through the SPI interface. A microcontroller with an integrated EEPROM and SPI master is usually used for this purpose. Depending on the required function the parameters must be written in a certain order (Figure 4).

If iC-LNB is to be used without FlexCount, only the required interpolator resolution is set (RESIPO) and en-

abled (ENIPO). The drivers at the A/B/Z outputs are then switched from tristate to push-pull state.

If the device is to be operated with FlexCount, the user then decides whether to leave the A/B/Z outputs in low or switch these to tristate (TRIA/BZ). After configuring all parameters, FlexCount is enabled (STOPFLEX 1 → 0). After the current position has been found (POSOK), the A/B/Z outputs can be enabled (TRIA/BZ or NOUTLO).

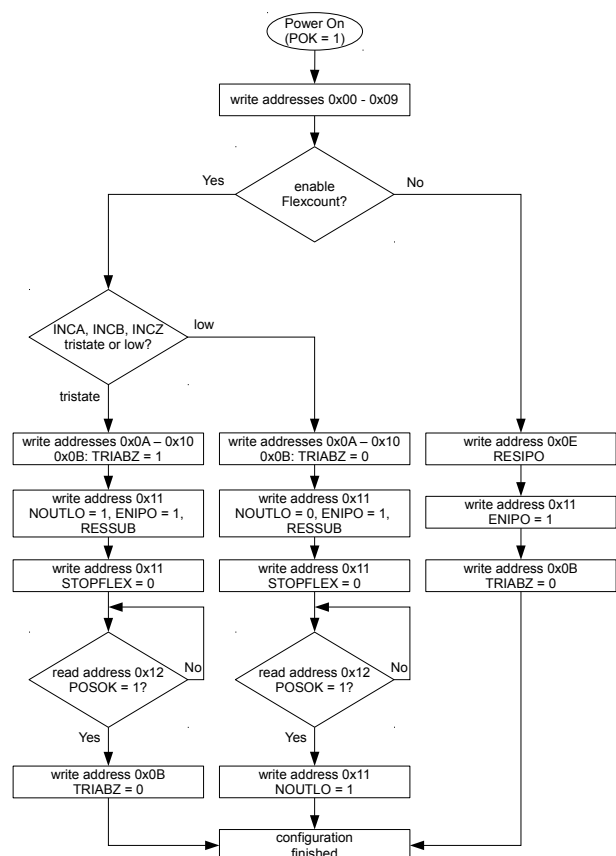


Figure 4: Example of a typical configuration sequence

OPERATING MODES

Device iC-LNB has two operating modes which are selected using register bit EPG.

EPG	Addr. 0x07; bit 4
Code	Description
0	Interface mode
1	Parallel mode

Table 8: Operating mode

In interface mode a shift register is provided for sensor data readout, with an incremental interface including an index signal (FlexCount active) for the output of encoder quadrature signals with a configurable resolution. A power-on signal at pin POK indicates that the system is enabled. Regardless of the FlexCount

resolution digital signals in Gray code are available at outputs GA and GB. These can be used for example to count the number of revolutions. A mechanical tilt angle of the scanner can be adjusted using output signal XJD.

In parallel encoder mode the sensor data is output as a 16-bit, parallel data word in Gray code. For this purpose all the relevant pins are reconfigured as outputs. Table 9 shows the pin functions for the respective operating mode (also see the parallel encoder mode section on page 31).

The SPI interface for device configuration can also be used for position data readout and is available in both operating modes.

PAD FUNCTIONS		
Pad	Interface mode	Parallel mode
GND	I/O Ports Ground	I/O Ports Ground
VDD	+ 3V to +5.5 V I/O Ports Supply Voltage	+ 3V to +5.5 V I/O Ports Supply Voltage
SCK	SPI Clock Input	SPI Clock Input
MOSI	SPI Data Input	SPI Data Input
MISO	SPI Data Output	SPI Data Output
CS	SPI Chip Select Input	SPI Chip Select Input
TNC	Test Input NCOS	Parallel Output Bit 15
TNS	Test Input NSIN	Parallel Output Bit 14
DIR	Code Inversion Input	Parallel Output Bit 13
NSL	Shift Register Load Input	Parallel Output Bit 12
DIN	Shift Register Data Input	Parallel Output Bit 11
DOUT	Shift Register Data Output	Parallel Output Bit 10
CLK	Shift Register Clock Input	Parallel Output Bit 9
GA	Graycode Output A (MSB)	Parallel Output Bit 8
GB	Graycode Output B (MSB-1)	Parallel Output Bit 7
XJD	Adjustment Signal	Parallel Output Bit 6
POK	Power OK Indication	Parallel Output Bit 5
INCZ	Incremental Output Z	Parallel Output Bit 4
INCB	Incremental Output B	Parallel Output Bit 3
INCA	Incremental Output A	Parallel Output Bit 2
ERR	Error Message Output	Error Message Output
TPS	Test Input PSIN	Parallel Output Bit 1
TPC	Test Input PCOS	Parallel Output Bit 0
NCOS	Analog Voltage Output NCOS	Analog Voltage Output NCOS
PCOS	Analog Voltage Output PCOS	Analog Voltage Output PCOS
NSIN	Analog Voltage Output NSIN	Analog Voltage Output NSIN
PSIN	Analog Voltage Output PSIN	Analog Voltage Output PSIN
LED	LED High Side Current Source	LED High Side Current Source
VDDA	+ 4V to +5.5V Supply Voltage	+ 4V to +5.5V Supply Voltage
GNDA	Ground	Ground

Table 9: Pad functions according to operating mode

SPI INTERFACE

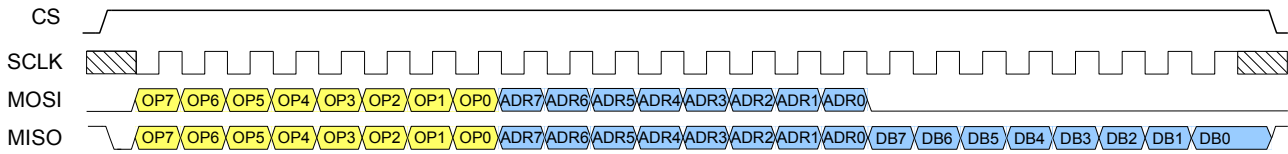


Figure 5: SPI transmission, taking the read OPCODE REGISTER as an example (continuous)

General protocol description

iC-LNB's SPI interface is implemented as an SPI slave and supports SPI modes 0 and 3, meaning the idle time at SCK can be 0 or 1. Data is always accepted on a rising edge at SCK. The idle state of the MISO line is 1; on a rising edge at CS the MOSI signal is switched through to the MISO signal. Data is sent byte by byte with the MSB (most significant bit) first. Each data transmission starts when a 1-byte OPCODE is sent by the SPI master (Table 10). This OPCODE selects whether the iC-LNB configuration data (REGISTER) or position data (SDAD) should be accessed, for instance.

OPCODE	
Code	Command
0xB0	ACTIVATE
0xA6	Sensor data (SDAD) transmission
0xF5	Sensor data (SDAD) status
0x8A	REGISTER read (continuous)
0xCF	REGISTER write (continuous)
0xAD	REGISTER status/data

Table 10: SPI Instructions / OPCODES

SPI data transmission takes place as follows: (Figure 5):

1. The master initializes a transmission on a rising edge at CS.
2. iC-LNB transfers the level from MOSI to MISO.
3. The master transmits the OPCODE and address ADR through MOSI; iC-LNB immediately outputs OPCODE and ADR through MISO.
4. iC-LNB transmits the data requested according to the address.
5. The master ends the command with a falling edge at CS.
6. iC-LNB switches its MISO output to 1.

OPCODE description

ACTIVATE

iC-LNB's register and sensor data channels can be switched on and off using the **ACTIVATE** command. The command causes all slaves to zero their RACTIVE and PACTIVE registers and to loop this register data into the data stream between the MOSI and MISO. The register and sensor or actuator data channels can be switched on and off using the following data bytes. After a power-on iC-LNB's sensor data channel is disabled (PACTIVE = 0) and register communication enabled (RACTIVE = 1).

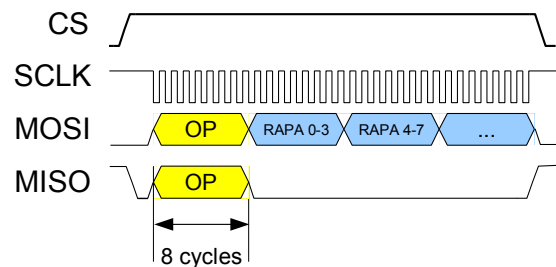


Figure 6: Setting ACTIVATE: RACTIVE/PACTIVE (several slaves)

Bytes FAIL, VALID, BUSY, and DISMISS in the STATUS byte are reset by the **ACTIVATE** command (Table 14).

RACTIVE	
Code	Description
0	Register communication deactivated
1	Register communication activated

Table 11: Register com. activation

If RACTIVE is not set, on commands **Read REGISTER (cont.)**, **Write to REGISTER (cont.)**, and **REGISTER status/data** the ERROR bit is set in the SPI interface STATUS byte (Table 14), indicating that the command has not been carried out. The slave immediately outputs the data at MISO which has been sent by the master through MOSI.

PACTIVE	
Code	Description
0	Sensor data channel deactivated
1	Sensor data channel activated

Table 12: Sensor data activation

If PACTIVE is not set, on commands **Sensor data status** or **Sensor data transmission** the ERROR bit is set in the STATUS byte (Table 14), indicating that the command has not been carried out. The slave immediately outputs the data at MISO which has been sent by the master through MOSI.

If only one slave is connected up with one register and one sensor data channel, it must be ensured that the RACTIVE and PACTIVE bits are last in the data byte (Figure 7).

NB: daisy chain

If the slaves are connected in a chain (full duplex chain), with this command the master can determine the number of connected register and sensor data channels. To this end it can send a 1 after the OP-CODE, which is repeated at MISO after the number of register and sensor data channels (see Figure 7).

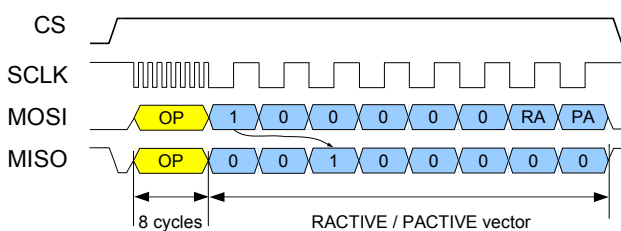


Figure 7: Setting ACTIVATE: RACTIVE/PACTIVE (one slave)

Sensor data transmission

iC-LNB latches its position data on the first rising edge at SCLK if CS is switched to 1 (REQ). The sensor data shift register is switched between signals MOSI and MISO for SPI communication and can then be clocked out. **The size of the sensor data shift register must be set to 18 bits** (see section on shift register output, page 30). The position data is output with the MSB first. Byte SD3 (Figure 8) is then filled with zeroes.

If invalid data is sampled in the shift register, the ERROR bit is set in the STATUS byte (Tab. 14) and zeroes are output as the data word.

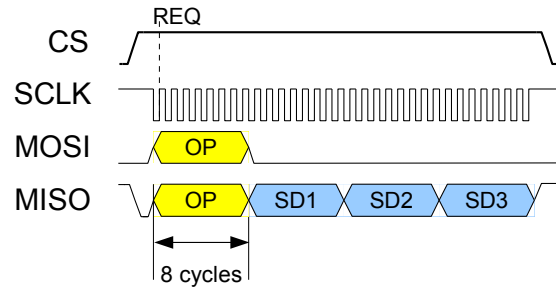


Figure 8: SDAD transmission: read SD

With command **Sensor data transmission** the master can not only read sensor data (SD) out from the slave; at the same time it can also transmit actuator data (AD) to the slave. iC-LNB ignores the transmitted actuator data.

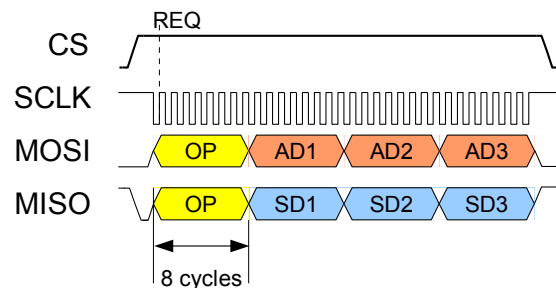


Figure 9: SDAD transmission: read SD, write AD

Sensor data status

Should the master not know the processing time, it can request sensor data using the command **Sensor data status**. iC-LNB does not need any processing time; therefore, SVALID is always valid.

The command causes

1. all slaves activated with PACTIVE to switch their SVALID register between MOSI and MISO.
2. The next request for sensor data, triggered on the first rising edge at SCLK when CS has again been set to 1, is ignored by the slave.

The end of conversion is signaled by SVALID (SV). With this command the master can poll to the end of conversion. The sensor data is readout on the command **SDAD transmission**.

SVALID	
Code	Description
0	Sensor data channel invalid
1	Sensor data channel valid

Table 13: Sensor data valid indication

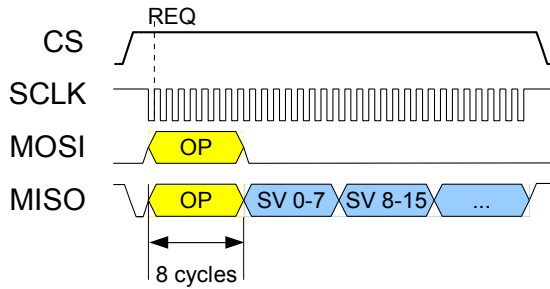


Figure 10: SDAD status

If only one slave is connected, the relevant SVALID bit is placed at bit position 7 in the SVALID byte (SV0, Figure 11).

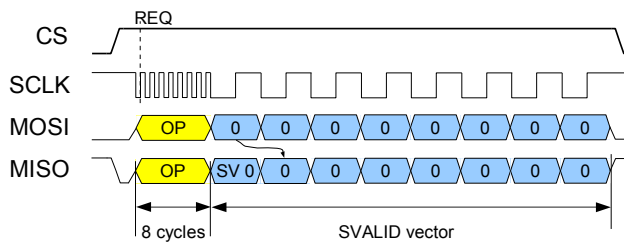


Figure 11: SDAD status (one slave)

REGISTER status/data

The status of the last REGISTER communication or the last data transmission can be queried using the **REGISTER status/data** command. The STATUS byte contains the information summarized in Table 14.

STATUS		
Bit	Name	Description of the status report
7	ERROR	OPCODE invalid. Sensor data was invalid on readout
6..4	-	Reserved
3	DISMISS	Address refused
2	FAIL	Data request has failed
1	BUSY	Slave is busy with a request
0	VALID	DATA is valid
NB	Display logic: 1 = true, 0 = false	

Table 14: SPI status information

All status bits are updated with each register access. The ERROR bit is the exception to the rule; this bit signals whether an error occurred during the last communication with the SPI interface or not.

The master transmits the OPCODE **REGISTER status/data**. iC-LNB immediately passes the OPCODE on to MISO. iC-LNB then transmits the STATUS byte

and a DATA byte. The DATA byte is not available in iC-LNB and is thus not defined.

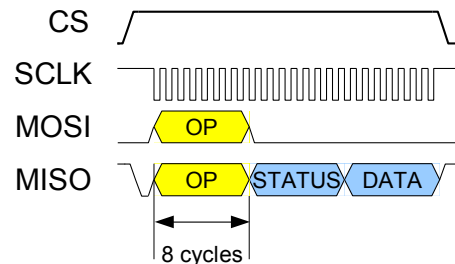


Figure 12: REGISTER status/data

Read REGISTER (continuous)

The master transmits the OPCODE **Read REGISTER (cont.)**. Start address ADR, from which point data is to be read, is transmitted in the 2nd byte. The slave immediately outputs the OPCODE and address and then transmits DATA1. The internal address counter is incremented after each data package.

If an error occurs during register readout in continuous mode, i.e. the address is invalid, the requested data was not valid on data byte clocking, etc., the internal address counter is incremented no further and the FAIL error bit is set in the status byte (Table 14).

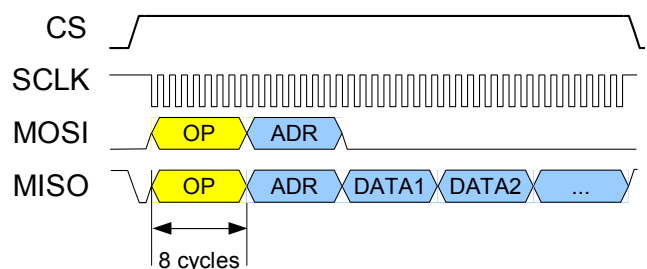


Figure 13: Read REGISTER (cont.)

Write to REGISTER (continuous)

The master transmits the OPCODE **Write to REGISTER (cont.)**. Start address ADR, from which point successive data DATA1-DATAN is to be written, is transmitted in the 2nd byte. The slave immediately outputs the OPCODE, address, and data at MISO. The slave increments its internal address counter after each DATAN data package.

If an error occurs during a write to register in continuous mode, i.e. the address is invalid, writing of the last address data has not finished, etc., the internal address counter is incremented no further and the FAIL error bit is set in the status byte (Table 14).

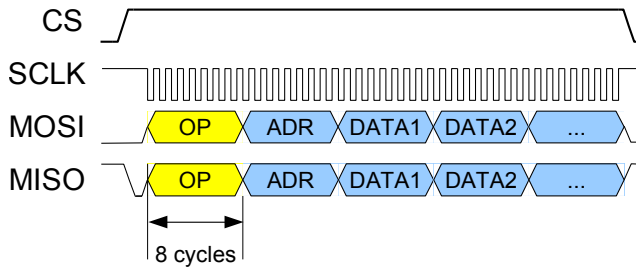


Figure 14: Write to REGISTER (cont.)

GRAY-CODE OUTPUTS

In interface mode the outputs GA, GB provide two 90° shifted digital signals with 1 PPR each (Figure 15). The signals are independent of the Flex-Count resolution (RESSUB) or the zero position (ZPOS), but pin DIR or register bit DIR can be applied to invert the signal GA (code inversion). Thereby GA and GB can be used for instance to trigger an external multiturn to count the revolutions.

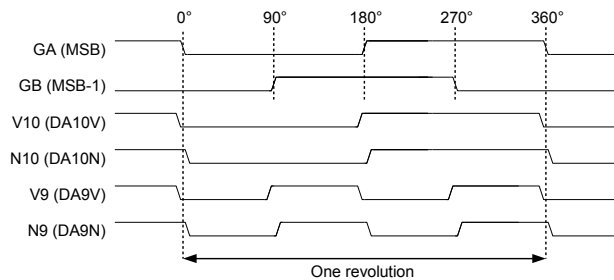


Figure 15: Phase of GA, GB without code inversion

ADJUSTMENT

iC-LNB is adjusted in relation to the code disc with the help of an electronic alignment aid.

Tilt angle

In interface mode (EPG = 0) an EXORed signal from tracks DA4V and DA10V (differential signal of the leading track 4 and track 10 diodes) is output at pin XJD. By tilting iC-LNB output signal XJD can be given a minimum spike length at 0° and 180°.

The falling or rising edge of signal GA (MSB bit in interface mode) marks the 0° and 180° positions.

The maximum tilt angle tolerated by the system is stipulated by the resolution and the diameter of the code disc. Table 15 shows the allocation of the maximum tilt to the relevant code disc.

Code disc	tilt angle max.
LNB1S 42-1024	1.8°
LNB4S 26-1024	1.0°

Table 15: Maximum tilt angle referenced to the chip's center

Example: LNB1S 42-1024

The scan ratio for the adjustment signal at XJD can be derived from the maximum tilt. At a tilt angle of 1.8° photodiode DA4V is approximately 74 μm from the ideal position; with an average radius of 19.89 mm for track DA4 there is an edge shift of 0.06%. The edge shift for photodiode DA10V is contradirectional and about the same size. A spike length of $t/T = 0.12\%$ is thus accrued for a maximum tilt angle of 1.8°. If we were to take half of the maximum tilt angle as a target alignment, i.e. 0.9°, the device must be aligned to a spike length of $(t/T) < 0.06\%$.

Spike length t can be computed dependent on the speed. Under optimum conditions the maximum spike length is $t = 0.0006 / \text{revs per second}$. Due to imperfect light levels, code disc tolerances, etc. a spike length of about half this maximum value should be aimed for (e.g. of less than 60 μs for a speed of 300 rpm).

The maximum spike length must be adhered to for both spikes (at 0° and 180°); ideally, both spikes should be the same length.

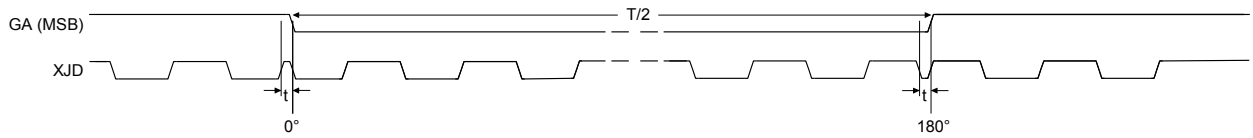


Figure 16: EXOR signal at XJD in interface mode

Radial adjustment to code disc

The digital tracks' distance determines the maximum tolerable offset from the radial ideal position. Starting from an offset of > 100 µm a crosstalk of the nearby digital track occurs. This can cause an incorrect absolute position.

A radial offset causes amongst others an alteration in the phase contact between sine/cosine signals. Thereby with minimizing the phase error the radial po-

sition can be adjusted in a range of about ±150 µm. Table 16 illustrates the phase error at a radial offset of 100 µm.

Code disc	Phase error
LNB1S 42-1024	0.65°
LNB4S 26-1024	1.6°

Table 16: Phase error at a radial offset of 100 µm

SIGNAL CONDITIONING

iC-LNB has various parameters for signal conditioning.

Gain

The gain of the analog sine/cosine track can be set using parameter GR. A gain factor of 1.33 (GR=0x01) can be used for most applications.

GR	Addr. 0x07; bit 1:0
Code	Gain factor
00	1.0
01	1.33
10	1.6
11	2.0

Table 17: Gain range for the sine/cosine track

The sine/cosine signals can be calibrated in amplitude and offset (Figure 17). To this end the LED power control must be programmed to sum control (LCTYP = 1) and the internal calibration signals switched to analog outputs PSIN, NSIN, PCOS, and NCOS (TA = 0x1, page 33).

The optical power of the LED can be adjusted to the approximate target amplitude (VPx/VNx) with parameter LCSET(5:0). The amplitude and offset parameters should be set to reasonable start values for this purpose (see register reset values in Table 7).

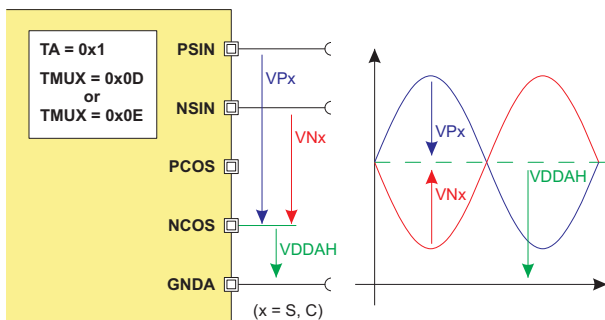


Figure 17: Sine/cosine signal calibration

Sine calibration

To calibrate the sine signals TMUX must be programmed to 0x0D (page 33). The amplitude of signals PSIN and NSIN can then be calibrated using parameter GS. The target amplitude (VPx/VNx) is 500 mVp.

GS	Addr. 0x00; bit 5:0
Code	Gain factor
0x00	1.0
0x01	1.01
...	$\frac{1+GS-0.0053}{1-GS-0.0053}$
0x3F	2.0

Table 18: PSIN and NSIN gain

The PSIN and NSIN offsets can be calibrated separately using parameters OSP and OSN. The offset of signal PSIN must be calibrated to reference signal VDDAH. This signal is available in test mode at pin NCOS. The offset of signal NSIN must then be calibrated to the calibrated offset of signal PSIN.

OSP	Addr. 0x02; bit 6:0
Code	Offset values
0x00	$0.45 \cdot VDDA$
0x01	$0.4508 \cdot VDDA$
...	$(0.45 + \frac{OSP-0.1}{127}) \cdot VDDA$
0x7F	$0.55 \cdot VDDA$

Table 19: PSIN offset

OSN	Addr. 0x03; bit 6:0
Code	Offset values
0x00	$0.45 \cdot VDDA$
0x01	$0.4508 \cdot VDDA$
...	$(0.45 + \frac{OSN-0.1}{127}) \cdot VDDA$
0x7F	$0.55 \cdot VDDA$

Table 20: NSIN offset

Cosine calibration

To calibrate the cosine signals TMUX must be programmed to 0x0E. The amplitude of signals PCOS and NCOS can then be calibrated to the same amplitude as that of the sine signals using parameter GS.

GC	Addr. 0x01; bit 5:0
Code	Gain factors
0x00	1.0
0x01	1.01
...	$\frac{1+GC-0.0053}{1-GC-0.0053}$
0x3F	2.0

Table 21: PCOS and NCOS gain

The PCOS and NCOS offsets can be calibrated separately using parameters OCP and OCN. The offset of signal PCOS must be calibrated to reference signal

VDDAH. This signal is available in test mode at pin NCOS. The offset of signal NCOS must then be calibrated to the calibrated offset of signal PCOS.

The signal path of the Sin/Cos tracks is shown in Figure 18 with the conditioning unit.

OCP		Addr. 0x04; bit 6:0
Code	Offset values	
0x00	$0.45 \cdot VDDA$	
0x01	$0.4508 \cdot VDDA$	
...	$(0.45 + \frac{OCP \cdot 0.1}{127}) \cdot VDDA$	
0x7F	$0.55 \cdot VDDA$	

Table 22: PCOS offset

OCN		Addr. 0x05; bit 6:0
Code	Offset values	
0x00	$0.45 \cdot VDDA$	
0x01	$0.4508 \cdot VDDA$	
...	$(0.45 + \frac{OCN \cdot 0.1}{127}) \cdot VDDA$	
0x7F	$0.55 \cdot VDDA$	

Table 23: NCOS offset

Square control

After all parameters (gain and offset) have been calibrated, it is recommended that the square control function in the LED power control be enabled (see the LED power control section on page 27) in order to keep the optical receive power of the sine/cosine sensors constant, regardless of temperature and LED ageing effects. To this end the device is switched to normal mode ($TA = 0x0$) and square control enabled ($LCTYP = 0$). The LED power control setpoint is adjusted to the set target amplitude with parameter LCSET(5:0).

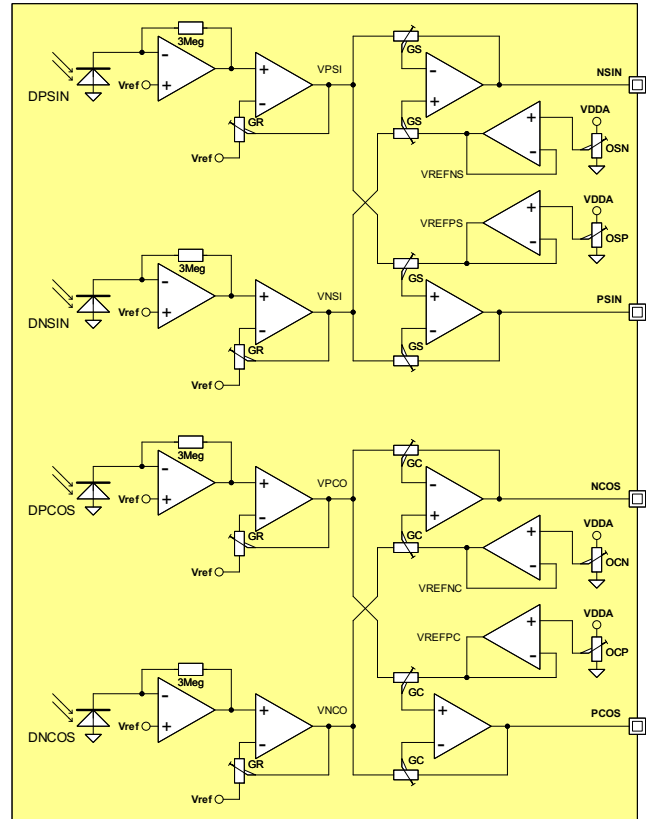


Figure 18: Sin/Cos signal path

LED POWER CONTROL

The optical receive power of the sine/cosine sensors is kept constant by an integrated LED control unit, regardless of the temperature and ageing effects of the LED. The mode of control can be selected using parameter LCTYP, the possible options being sum control or square control. So that the internal interpolator is always optimally controlled in all operating conditions, square control should be used. Sum control should be used for signal conditioning.

LCTYP Addr. 0x06; bit 6	
Code	Control type
0	square control ($\sin^2 + \cos^2$)
1	sum control (DC controlled prop. to VR())

Table 24: LED power control type

The setpoint for the control can be configured using parameter LCSET(5:0).

LCSET(5:0) Addr. 0x06; bit 5:0		
Code	Square control LCTYP = 0	Sum control LCTYP = 1
0x00	0.240 Vp	0.140 V
0x01	0.243 Vp	0.142 V
...	$\frac{0.24 \text{ Vp}}{1 - i \cdot 0.0125}$	$\frac{0.14 \text{ V}}{1 - i \cdot 0.0125}$
0x3F	1.1 Vp	0.640 V

Table 25: LED power control setpoint

LCMOD Adr 0x01, bit 6	
Code	Control mode (LCTYP = 0 or 1)
0	continuous control
1	deadband control (approx. 5% of setpoint)

Table 26: LED power control mode

Error monitoring

iC-LNB's LED power control is monitored. Should the LED current exceed its control range, internal error ERRS (status register) is set to 1. This error signal is linked to iC-LNB's ERRP alarm (parity check) and output at error output ERR (see the alarm output section).

INTERPOLATOR

Interpolator resolution

The resolution of the internal interpolator is set using RESIPO. The maximum permissible Sin/Cos signal frequency (RPM speed) is dependent on the selected resolution. Before changing the interpolator resolution, the interpolator must be disabled (ENIPO = 0). During the interpolator is disabled 0 is output as the interpolated position value. Once changes have been made, the interpolator can be re-enabled (ENIPO = 1).

RESIPO Addr. 0x0E; bit 6:5		
Code	Interpolator resolution	Max. sin/cos frequency
00	8 bit	50 kHz
01	7 bit	100 kHz
10	6 bit	200 kHz
11	Interpolator deactivated	-

Table 27: Interpolator resolution

ENIPO Addr. 0x11; bit 4	
Code	Description
0	Interpolator disabled
1	Interpolator enabled

Table 28: Interpolator enable

Interpolator filter

The interpolator input signals can be filtered by a low-pass filter. This filter can be enabled by NENF. The filter has been designed so that it can be applied across the entire speed range.

NENF Addr. 0x07; bit 6	
Code	Description
0	Filter enabled (recommended)
1	Filter disabled

Table 29: Interpolator filter

FLEXCOUNT®

When FlexCount is enabled in iC-LNB, the resolution can be freely programmed and is output through the incremental signals. Another option is to output the set resolution through the SPI interface and the shift register, or, in parallel encoder mode, to the parallel IO ports. FlexCount operates in real time and does not introduce any significant latency to the signal path.

Enable/disable

FlexCount can be enabled using register bit NENFLEX. SELABS determines whether the FlexCount resolution or iC-LNB's maximum internal resolution (dependent on RESIPO) is output for the absolute data output (parallel encoder mode, shift register or SPI).

NENFLEX		Addr. 0x0B; bit 1
Code	Description	
0	FlexCount enabled	
1	FlexCount disabled	

Table 30: FlexCount disable

SELABS		Addr. 0x0B; bit 2
Code	SER/PAR/SPI interface	
0	FlexCount resolution	
1	Maximum resolution*	
*16 bit, 17 bit, 18 bit dependent on RESIPO		

Table 31: SPI, SER, PAR absolute output options

Resolution

Parameter RESSUB defines the FlexCount resolution. The binary value in RESSUB is equivalent to the required resolution minus 1; for instance, RESSUB must be programmed to 0x0FFFF (binary value for 65,535) for a resolution of 65,536 steps (a 16-bit resolution).

The required resolution must be divisible by four and the maximum resolution is limited by the set interpolator resolution. At an interpolation of 6 bits FlexCount may have a maximum resolution of 65,536 (RESSUB = 0x0FFFF); at 7-bit interpolation this maximum rises to 131,072 (RESSUB = 0x1FFFF), and at 8 bits to a full resolution of 262,144 (RESSUB = 0x3FFFF). FlexCount is always output in Gray code for all settable resolutions. With non-binary resolutions the Gray code is capped symmetrically to 0. This retains the required single-step transitions of the Gray code.

RESSUB		Addr. 0x0F; 0x10; 0x11 bit 3:0
Code	Resolution (edges per revolution)	
0x3	4	
0x7	8	
...	RESSUB + 1	
0x0FFFF	65536	
...	... (only with 7/8 bit interpolation)	
0x1FFFF	131072 (only with 7/8 bit interpolation)	
...	... (only with 8 bit interpolation)	
0x3FFFF	262144 (only with 8 bit interpolation)	
NB: RESSUB = resolution - 1		

Table 32: FlexCount resolution

Reset

FlexCount must be stopped before the resolution or direction of rotation are reprogrammed (pin DIR or register bit DIR). This is done using register bit STOPFLEX. This freezes the FlexCount outputs and FlexCount goes into its reset state. After STOPFLEX has been reset the outputs are enabled and FlexCount moves to the current position.

STOPFLEX		Addr. 0x11; bit 5
Code	Description	
0	Normal operation	
1	FlexCount stopped	
FlexCount reset: STOPFLEX 1 → 0		

Table 33: FlexCount reset

Following a reset (STOPFLEX 1 → 0) FlexCount searches for the current position. During this position signals/data are not valid. Attainment of the current position and thus valid output signals are indicated in the status register with POSOK.

POSOK		Addr. 0x12; bit 0
Code	Description	
0	Position invalid	
1	Position valid	

Table 34: Position valid

The FlexCount output signals can be set to low using register bit NOUTLO; FlexCount itself continues to run. This function should be used after FlexCount has been reset to prevent the device 'running' to the current position in the output signals.

NOUTLO Addr. 0x11; bit 6	
Code	Internal FlexCount outputs
0	low
1	Normal operation

Table 35: Setting FlexCount outputs to low

INVZ Addr. 0x0B; bit 4	
Code	Incremental output INCZ
0	not inverted
1	inverted

Table 39: Output inversion INCZ

Hysteresis

A hysteresis can be programmed for FlexCount. The size of the hysteresis can be set as a multiple of the interpolator LSB step size using parameter HYS. This means that the resolution of the interpolator influences the selectable hysteresis.

HYS Addr. 0x0B, bit 0; Addr. 0x0A, bit 6:0			
Code	RESIPO = 0x0 8-bit interp.	RESIPO = 0x1 7-bit interp.	RESIPO = 0x2 6-bit interp.
0x0	No hysteresis	No hysteresis	No hysteresis
0x1	±1 LSB	No hysteresis	No hysteresis
0x2	±2 LSB	±1 LSB	No hysteresis
0x3	±3 LSB	±1 LSB	No hysteresis
0x4	±4 LSB	±2 LSB	±1 LSB
...			
0xFC	±252 LSB	±126 LSB	±63 LSB

Table 36: FlexCount hysteresis

Incremental outputs

When FlexCount is enabled, incremental outputs A/B/Z can be inverted as required using register bits INVA, INVB, and INVZ. If the A/B/Z outputs are not generated by FlexCount ($INC \neq 0x07$), inversion will not function.

INVA Addr. 0x0B; bit 6	
Code	Incremental output INCA
0	not inverted
1	inverted

Table 37: Output inversion INCA

INVB ADR 0x0B, bit 5	
Code	Incremental output INCB
0	not inverted
1	inverted

Table 38: Output inversion INCB

Position offset

iC-LNB's FlexCount permits a programmable position offset. This offset can be set as a binary value of the maximum internal resolution (which is dependent on interpolator resolution RESIPO) using parameter ZPOS (not in the selected FlexCount resolution). All values from 0 to 262,143 can be selected at 8 bits; at 7 bits the LSB must remain fixed at 0, and at 6 bits the last two LSBs must be 0. If no position offset is set ($ZPOS = 0x0$), the zero position is symmetrical with the falling edge of the MSB (in interface operation: signal at pin GA, Figure 19).

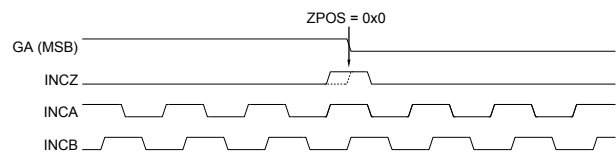


Figure 19: Zero position for ZPOS = 0x0

ZPOS Addr. 0x0C; 0x0D; 0x0E bit 3:0	
Code	Positions offset (binary)
0x0	0
0x1	1 (only with 8 bit interpolation)
0x2	2 (only with 7/8 bit interpolation)
...	ZPOS
0x7FFF	32767 (only with 8 bit interpolation)
...	ZPOS
0x10000	65536
...	ZPOS
0x3FFFF	262143 (only with 8 bit interpolation)

Table 40: Position offset

The length of the Z pulse can be selected using parameter Z90. It can be set to a width of 90° or 180°.

Z90 Addr. 0x0E; bit 4		
Code	Index width	Index gating
0	180°	A
1	90°	A & B

Table 41: Z pulse width

INCREMENTAL OUTPUT

Selecting the output

At pins INCA and INCB incremental signals are output with either various interpolation factors or FlexCount resolutions. Selection is made using parameter INC.

INC		Addr. 0x08; bit 6:4
Code	Function	
0x00	Interpolation factor x1	
0x01	Interpolation factor x2	
0x02	Interpolation factor x4	
0x03	Interpolation factor x8	
0x04	Interpolation factor x16	
0x05	iC-Haus digital test	
0x06	iC-Haus test	
0x07	FlexCount	

Table 42: Incremental output options

A valid Z pulse is only output at pin INCZ when FlexCount is enabled (INC = 0x07).

Output in digital test and iC-Haus test modes is described in the section on test functions on page 33.

Tristate

The incremental signal pins (INCA/INCB/INCZ) can be switched to tristate using register bit TRIABZ. After a power-on TRIABZ is initialized with a 1.

TRIABZ		Addr. 0x0B; bit 3
Code	Pin function of INCA, INCB, INCZ	
0	Push-pull (incremental signals)	
1	Tristate	

Table 43: Incremental output tristate

SHIFT REGISTER OUTPUT

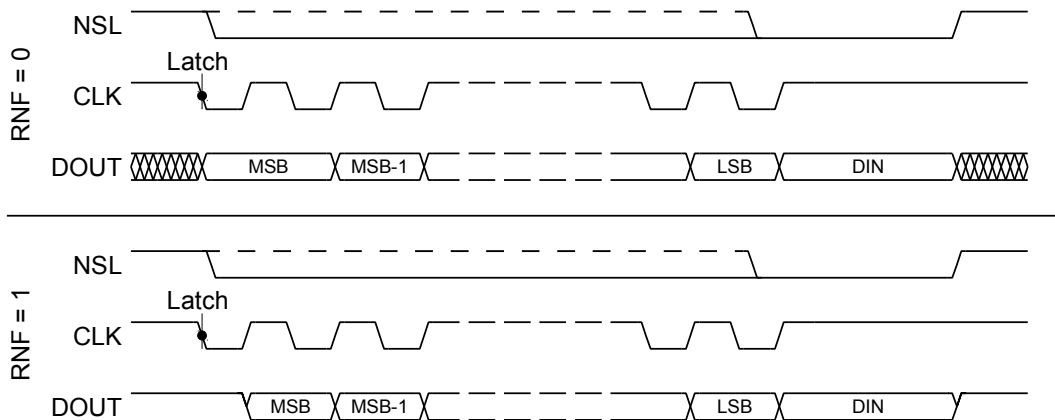


Figure 20: Shift register output

iC-LNB has a shift register for position data readout. In order to enable this shift register the sensor data channel for the SPI interface must be disabled by command **ACTIVATE** (table 12). After power-on the shift register in iC-LNB is active and the sensor data channel of the SPI interface is deactivated.

The position data is output in Gray code or binary code (depending on parameter NGRAY), with the MSB first. If pin NSL = 1, the position data is loaded into the shift register on the first falling edge at pin CLK. Following this, the data is clocked out on each rising edge at pin CLK, regardless of the level at pin NSL.

The shift register returns to its idle state on a rising edge at NSL. This means that the falling edge at NSL

can occur during data transmission and is not time critical.

RNF is used to select an output level at pin DOUT for idle state - either idle 1 (high) or the MSB bit in real time. External data can be read into iC-LNB through shift register input pin DIN. This is output after the position data. The position data readout process is shown in Figure 20.

The length of the shift register and the number of data bits used can be selected using parameter SRC.

NGRAY		Addr. 0x07; bit 6
Code	Data format	
0	Gray	
1	binary	

Table 44: Shift register output data format

If binary output is enabled (NGRAY = 1), DIN must be switched to 0, i.e. no external data can be read into the shift register (as in ring operation, for example).

RNF		Addr. 0x08; bit 3
Code	Output pin DOUT	
0	MSB bit	
1	High	

Table 45: Shift register idle output

SRC			Addr. 0x08; bit 2:0
Code	Shift register length	Number of used bits	
000	18-bit	18	
001	17-bit	17	
010	16-bit	16	
011	16-bit	15	
100	16-bit	14	
101	16-bit	13	
110	14-bit	13	
111	14-bit	12	

Table 46: Shift register length

PARALLEL ENCODER MODE

Depending on SELABS, in parallel encoder mode 16 bits of position data (10 bits from the digital tracks and 6 bits from the interpolator) are output in parallel, or FlexCount outputs the top 16 bits in parallel with the set RESSUB resolution.

Parallel encoder mode is enabled by parameter EPG = 1.

The interpolator resolution can be set to 6 bits (RE-SIPO = 0b10) to permit the maximum input frequency.

The MSB of the position data can be inverted by parameter DIR or pin DIR (code inversion). Parameter DIR and pin DIR are exor gated; for instance, no code inversion occurs if the level at pin DIR is high and parameter DIR = 1.

NB:

If FlexCount is enabled, after changing the direction of rotation FlexCount must be reset (Table 33).

DIR		Addr. 0x07; bit 5
Code	Description	
0	CW (no inversion)	
1	CCW (inversion)	

Table 47: Code inversion

Programming the interpolator resolution to 7 and 8 bits allows an extra 17 or 18 bits of position data to be read in through the SPI interface.

EPG		Addr. 0x07; bit 4
Code	Description	
0	Interface mode	
1	Parallel mode	

Table 48: Selecting the operating mode

ALARM OUTPUT

iC-LNB has an alarm or error output to indicate existing errors. If an error occurs, pin ERR is set to 1.

iC-LNB's LED power control range is monitored. Should the LED power control exceed its control range, internal error ERRS (status register, table 6) is set to 1.

If the parity check signals an error in the RAM area, internal error ERRP (status register, table 6) is set to 1.

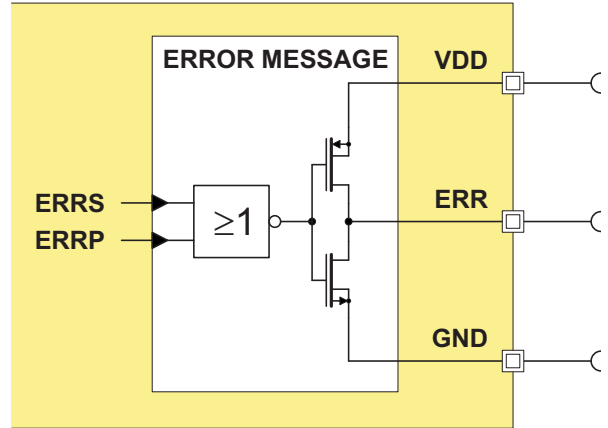


Figure 21: Alarm output

OSCILLATOR

iC-LNB has two internal oscillators for the interpolator and FlexCount. The frequency of these oscillators can be finely adjusted using register OSZC; this frequency limits iC-LNB's permissible Sin/Cos frequency.

In Table 49 f_b is a basic frequency of typically 12.8 MHz.

OSZC		
Addr. 0x07; bit 3:2		
Code	Description	Oscillator frequency (typ.)
00	$1.000 \cdot f_b$	12.8 MHz
01	$1.078 \cdot f_b$	13.8 MHz
10	$1.125 \cdot f_b$	14.4 MHz
11	$1.140 \cdot f_b$	14.6 MHz

Table 49: Oscillator adjustment

TEST FUNCTIONS

TA	Addr. 0x09; bit 5:4
Code	Output at PSIN, NSIN, PCOS, NCOS
00	Normal operation
01	Test signals (s. Tab. 51)
10	iC-Haus test
11	iC-Haus test

Table 50: Test modes

TMUX	Addr. 0x09; bit 3:0			
Code	Pin PSIN	Pin NSIN	Pin PCOS	Pin NCOS
0x00	VPSI	VNSI	VPCI	VNCI
0x01	AVP1	VTH	AVN1	VREF
0x02	ANP1	VTH	ANN1	VREF
0x03	AN2	VTH	AV2	VREF
0x04	AN3	VTH	AV3	VREF
0x05	AN4	VTH	AV4	VREF
0x06	AN5	VTH	AV5	VREF
0x07	AN6	VTH	AV6	VREF
0x08	AN7	VTH	AV7	VREF
0x09	AN8	VTH	AV8	VREF
0x0A	AN9	VTH	AV9	VREF
0x0B	AN10	VTH	AV10	VREF
0x0C	VREFPS	VREFNS	VREFPC	VREFNC
0x0D	PSIN	NSIN	PCOS	VDDAH
0x0E	PCOS	NCOS	PSIN	VDDAH
0x0F, NENF = 1	IPQT	–	–	–
0x0F, NENF = 0	PSF	NSF	PCF	NCF

Table 51: Test signal multiplexer for analog signals
(TA = 0x01)

TMUX	Addr. 0x09; bit 3:0		
Code	Pin INCA	Pin INCB	Pin INCZ
0x00	NENOS	NLOCK	I7
0x01	V1	N1	I7
0x02	V1	N1	I7
0x03	V2	N2	I7
0x04	V3	N3	I7
0x05	V4	N4	I7
0x06	V5	N5	I7
0x07	V6	N6	I7
0x08	V7	N7	I7
0x09	V8	N8	I7
0x0A	V9	N9	I7
0x0B	V10	N10	I7
0x0C	I6	I5	I7
0x0D	I4	I3	I7
0x0E	IPO_A	IPO_B	I7
0x0F	I2	I1	I7

Table 52: Test signal multiplexer for digital signals
(iC-Haus test, INC = 0x05)

DESIGN REVIEW: Notes On Chip Functions

iC-LNB X		
No.	Function, Parameter/Code	Description and Application Notes
1	FlexCount outputs low: NOUTLO = 1	Due to potential malfunction this parameter must not be used.
2	Permissible interpolator resolutions: RESIPO = 0x0 (8 bit) or RESIPO = 0x3 (deactivated)	Interpolator resolution 6/7 bit: If the rotation alters its direction, incremental and parallel outputs may switch wrong.
3	Default value of address 0x11 is 0x50	For configuration of iC-LNB first program address 0x11 to 0xA0, then follow sequence in figure 4.
4	LCMOD not available	standard control active
5	LCTYP (address 0x06): reset value is 0x30	For configuration of iC-LNB first program address 0x06 to 0x60, then follow sequence in Figure 4.

Table 53: Notes on chip functions regarding iC-LNB chip release X

iC-LNB X1		
No.	Function, Parameter/Code	Description and Application Notes
1	Interpolation without angle hysteresis (Elec. Char. No. 703)	Use FlexCount (NENFLEX=0) with hysteresis of at least 1 LSB configured by HYS.
2	LCMOD not available	standard control active
3	LCTYP (address 0x06): reset value is 0x30	For configuration of iC-LNB first program address 0x06 to 0x60, then follow sequence in Figure 4.

Table 54: Notes on chip functions regarding iC-LNB chip release X1

iC-LNB W1		
No.	Function, Parameter/Code	Description and Application Notes
1	LCTYP (address 0x06): reset value is 0x30	For configuration of iC-LNB first program address 0x06 to 0x60, then follow sequence in Figure 4.

Table 55: Notes on chip functions regarding iC-LNB chip release W1

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iC-LNB 18-BIT OPTO ENCODER WITH SPI AND SER/PAR INTERFACES



Rev A1, Page 35/35

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-LNB	30-pin optoBGA	standard reticle LNB1R standard reticle LNB4R customer specific reticle	iC-LNB oBGA LNB2C-1R iC-LNB oBGA LNB2C-4R iC-LNB oBGA LNB2C-xR
	38-pin optoQFN	standard reticle LNB1R customer specific reticle	iC-LNB oQFN38-7x5-1R iC-LNB oQFN38-7x5-xR
Standard Code Discs		Sin/Cos 1024 PPR, 10 bit digital OD/ID \varnothing 42/18 mm, glass	LNB1S 42-1024
		Sin/Cos 1024 PPR, 10 bit digital OD/ID \varnothing 26/9.6 mm, glass	LNB4S 26-1024

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