6 Output High Performance LVPECL Fanout Buffer

Features

- 6 LVPECL outputs
- Up to 1.5GHz output frequency
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Single differential input
- Low delay from input to output (Tpd typ. < 700ps)
- 2.5V / 3.3V power supply
- Industrial temperature support
- TSSOP-20 package

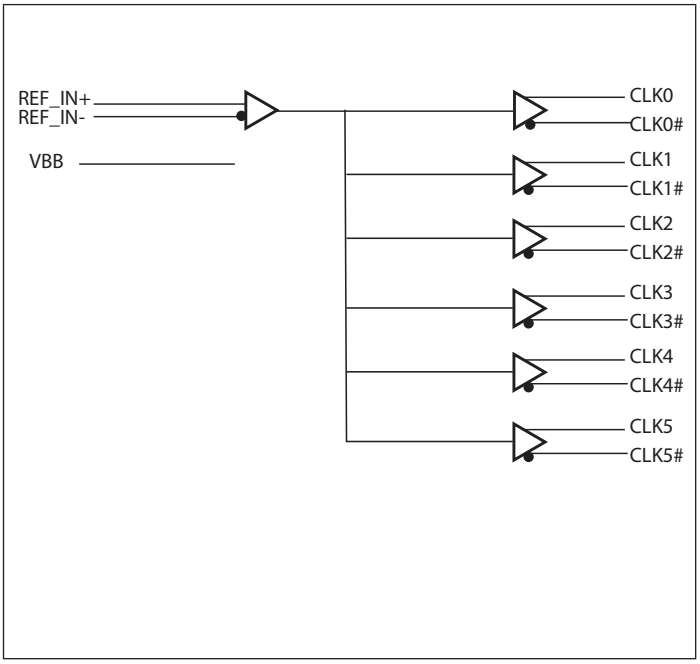
Description

The PI6C4911506 is a high performance fanout buffer device-which supports up to 1.5GHz frequency. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

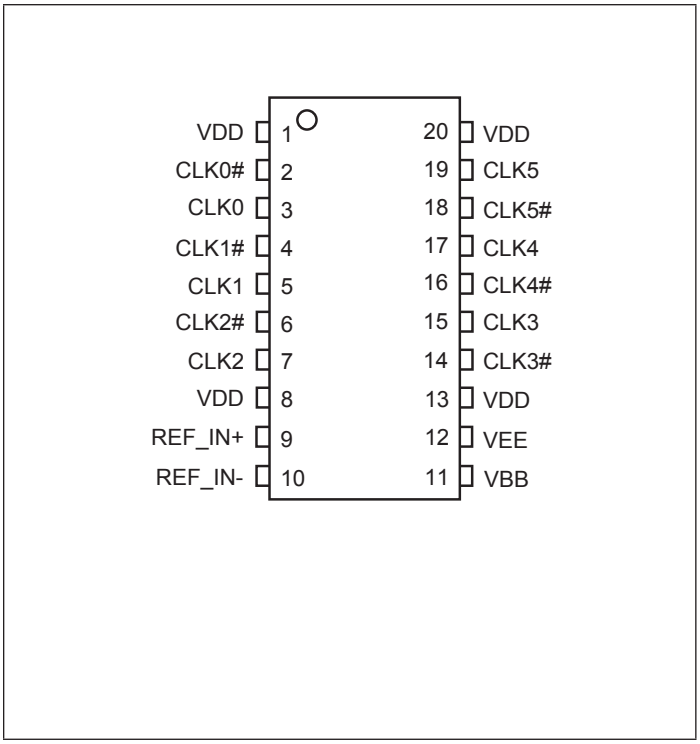
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (20-Pin TSSOP)



Pinout Table

Pin #	Pin Name	Type		Description
1, 8, 13, 20	V_{DD}	Power		Power supply
2, 3	CLK0#, CLK0	Output		Differential LVPECL output
4, 5	CLK1#, CLK1	Output		Differential LVPECL output
6, 7	CLK2#, CLK2	Output		Differential LVPECL output
9	REF_IN+	Input	Pulldown	Differential LVPECL input
10	REF_IN-	Input	Pull up/ Pull-down	Differential LVPECL input
11	V_{BB}	Output		Bias Voltage
12	V_{EE}	Power		Negative supply pin
14, 15	CLK3#, CLK3	Output		LVPECL output clock
16, 27	CLK4#, CLK4	Output		LVPECL output clock
18, 19	CLK5#, CLK5	Output		LVPECL output clock

Pin Characteristics

Symbol	Parameter	Min	Typ	Max	Units
R_{PULLUP}	Input Pullup Resistor		50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor		75		kΩ

Maximum Ratings (Over operating free-air temperature range)

Supply Voltage	4.6V
Storage Temperature	-65°C to+155°C
Ambient Temperature with Power Applied	-40°C to+85°C
3.3V Analog Supply Voltage	-0.5 to +3.7V
ESD Protection (HBM)	2000V
Junction Temperature	125°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Power Supply DC Characterisitcs, (T_A = -40°C to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	
I_{EE}	Power Supply Current	Outputs Unloaded		71	95	mA
I_{DD}	Power Supply Current	Outputs Unloaded		72	95	mA

LVPECL DC Characteristics, (T_A = -40°C to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3 V	2.0		2.36	V
		V_{DD} = 2.5 V	1.275		1.56	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3 V	1.43		1.765	V
		V_{DD} = 2.5 V	0.63		0.965	V
I_{IH}	Input High Current	REF_IN+, REF_IN-			150	µA
I_{IL}	Input Low Current	REF_IN+	-10			µA
		REF_IN-	-150			
V_{PP}	Input Peak to Peak Voltage		150		1200	mV
V_{OH}	Output High Voltage	V_{DD} = 3.3 V	2.06		2.54	V
		V_{DD} = 2.5 V	1.43		1.75	V
V_{OL}	Output Low Voltage	V_{DD} = 3.3 V	1.32		1.7	V
		V_{DD} = 2.5 V	0.82		1.02	V
V_{SWING}	Peak to Peak Output Voltage		625		870	mV
V_{BB}	Output Voltage Reference	V_{DD} = 3.3 V	1.76		1.98	V
V_{CMR}	Input Common Voltage Range		1.2		V_{DD}	V

ECL DC Characterisitcs, (T_A = -40°C to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		-1.225		-0.94	V
V_{IL}	Input Low Voltage		-1.87		-1.535	V
I_{IH}	Input High Current	REF_IN+, REF_IN-			150	µA
I_{IL}	Input Low Current	REF_IN+	-10			µA
		REF_IN-	-150			
V_{PP}	Input Peak to Peak Voltage		150		1200	mV
V_{OH}	Output High Voltage		-1.12		-0.89	V
V_{OL}	Output Low Voltage		-1.895		-1.65	V
V_{SWING}	Peak to Peak Output Voltage		625		870	mV
V_{BB}	Output Voltage Reference		-1.54		-1.32	V
V_{CMR}	Input Common Voltage Range		V_{EE}+ 1.2		0	V

Note:

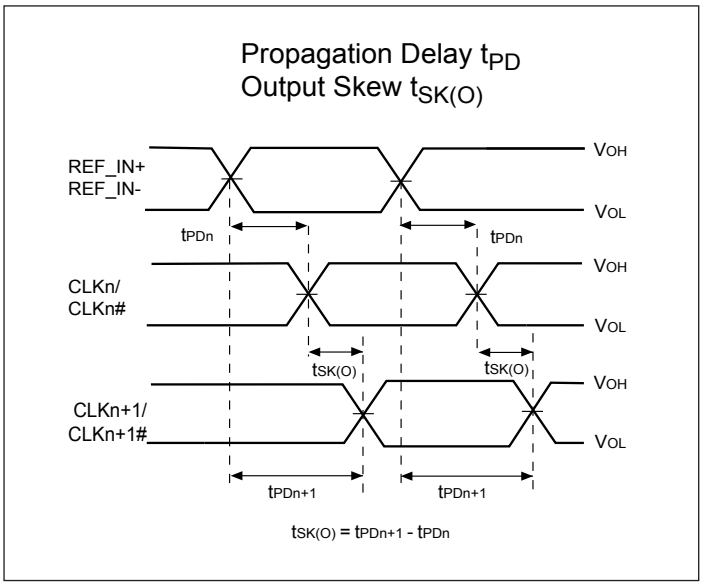
Note1: Single ended input limited to $V_{EE} \leq$ -3V in LVPECL

AC Electrical Characteristics

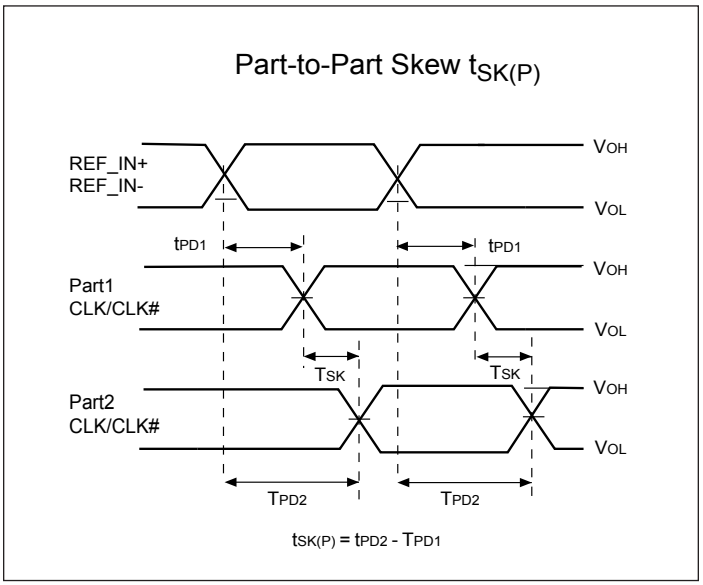
AC Characteristics, (T_A = -40°C to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{OUT}	Output Frequency				1.5	GHz
T_{PD}	Propagation Delay	V_{DD} = 3.3 V	400	520	650	ps
		V_{DD} = 2.5 V	450	560	700	
$T_{SK(0)}$	Output Skew				50	ps
$T_{SK(P)}$	Part to Part Skew				230	ps
T_{JITTER}	Additive Jitter			0.03		ps
T_R/T_F	Output Rise/ Fall Time	20% to 80%, Freq= 156.25MHz	100	180	250	ps
		10% to 90%, Freq = 156.25MHz	340	500	800	ps

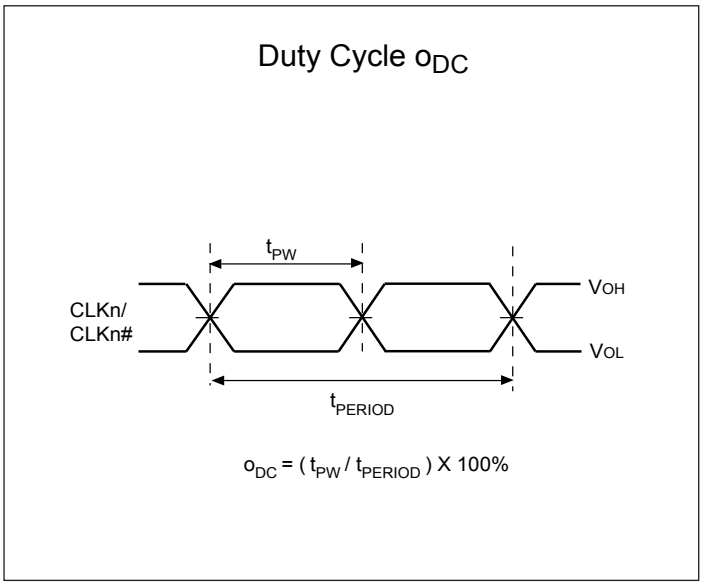
Propagation Delay and Output Skew



Part to Part Skew



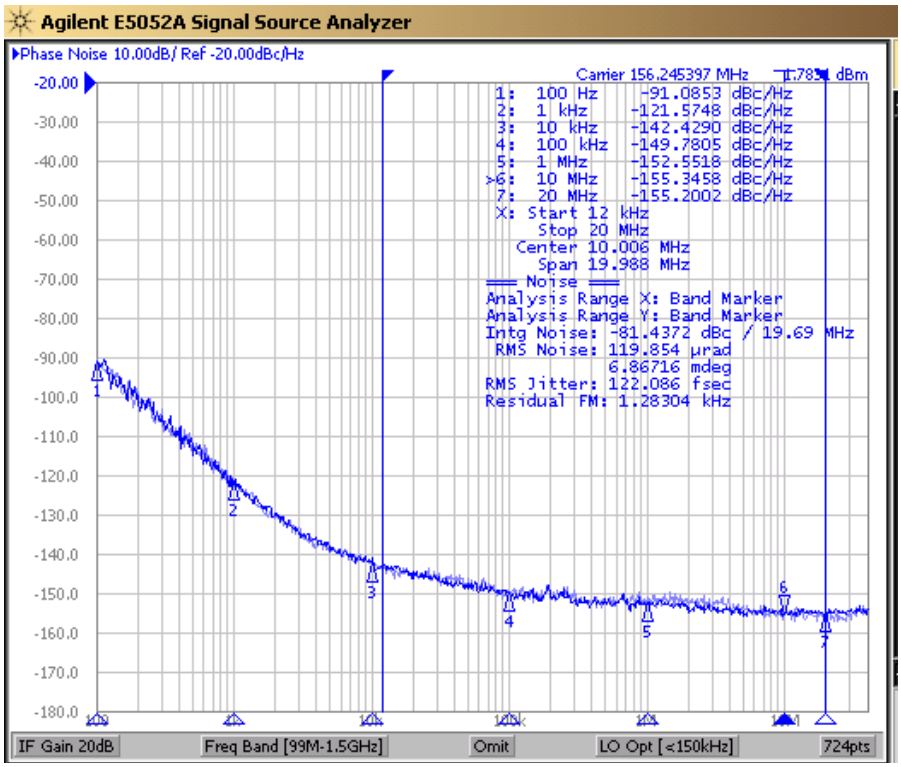
Output Duty Cycle



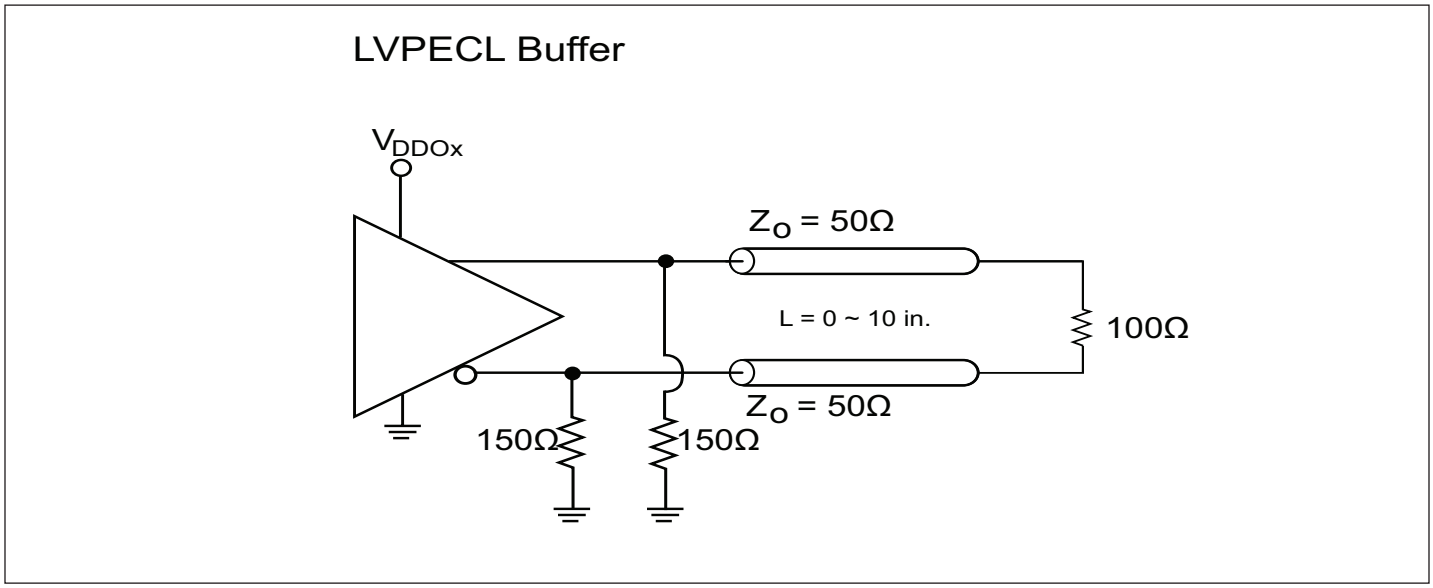
Phase Noise Plots

f_{OUT} = 156.25MHz

Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



LVPECL Test Circuit



Application information

Suggest for Unused Inputs and Outputs

Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power supply power.

Power Decoupling & Routing

VDD Pin Decoupling

As general design rule, each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as shown in Fig. 1.

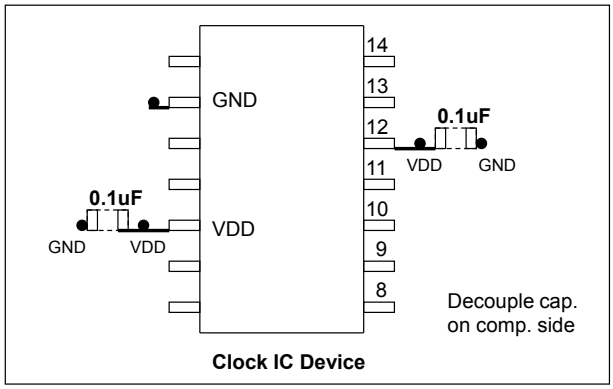


Fig 1: Placement of Decoupling caps

Differential Clock Trace Routing

Always route differential signals symmetrically, make sure there is enough keep-out space to the adjacent trace (>20mil.). In 156.25MHz XO drives IC example, it is better routing differential trace on component side as the following Fig. 2.

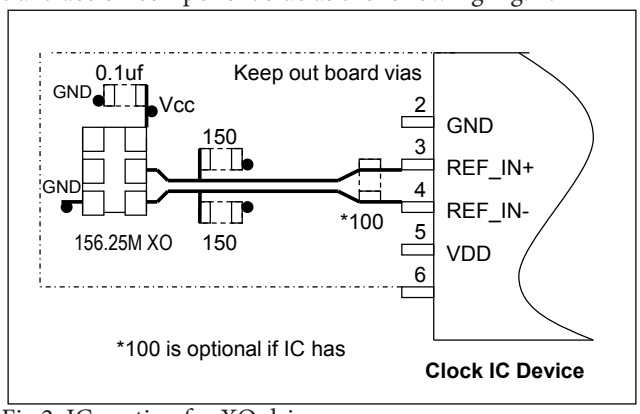


Fig 2: IC routing for XO drive

Clock timing is the most important component in PCB design, so its trace routing must be planned and routed as a first priority in manual routing. Some good practices are to use minimum vias (total trace vias count <4), use independent layers with good reference plane and keep other signal traces away from clock traces (>20mil.) etc.

LVPECL and LVDS Input Interface

LVPECL and LVDS DC/ AC Input

LVPECL and LVDS clock input to this IC is connected as shown in the Fig. 3.

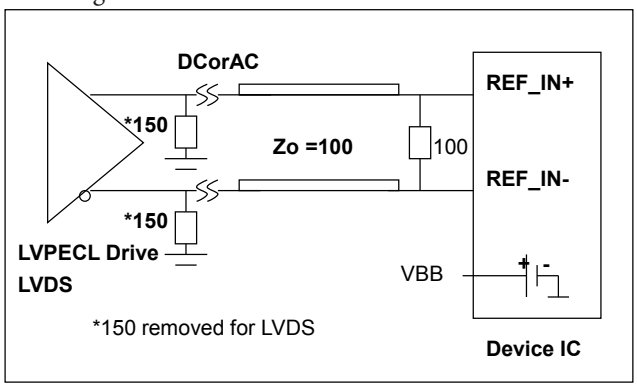


Fig 3: LVPECL/ LVDS Input

Use VBB LVPECL/LVDS AC Input

LVPECL and LVDS AC drive to this clock IC requires the use of VBB output to recover the DC bias for the IC input as shown in Fig. 4.

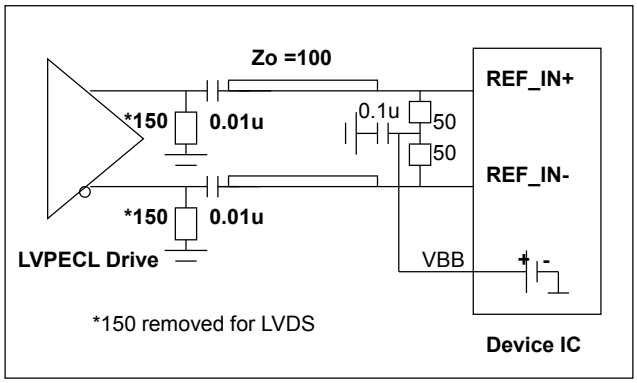


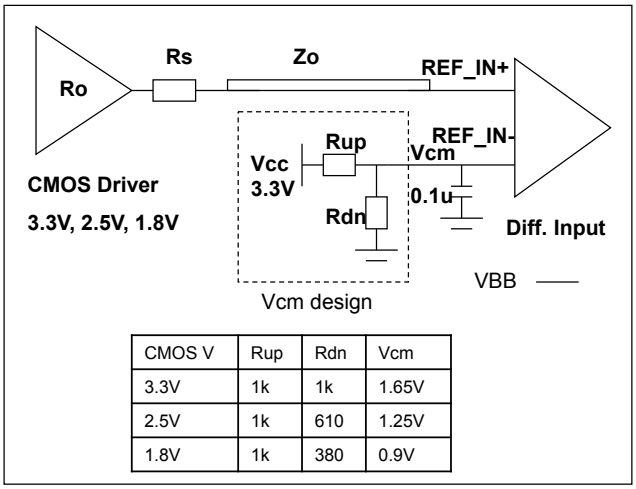
Fig 4: LVPECL/ LVDS AC Coupled Input

CML AC-Coupled Input

CML AC-coupled drive requires a connection to VBB. The CML DC drive is not recommended as different vendors have different CML DC voltage level. CML is mostly used in AC coupled drive configuration for data and clock signals.

CMOS Clock DC Drive Input

LVCMOS clock has voltage Voh levels such as 3.3V, 2.5V, 1.8V. CMOS drive requires a Vcm design at the input: Vcm= ½ (CMOS V) as shown in Fig. 7. Rs =22 ~33ohm typically.



CMOS V	Rup	Rdn	Vcm
3.3V	1k	1k	1.65V
2.5V	1k	610	1.25V
1.8V	1k	380	0.9V

Fig 5: CMOS DC Input Vcm Design

Device LVPECL Output Terminations

LVPECL Output Popular Termination

The most popular LVPECL termination is 150ohm pull-down bias and 100ohm across at RX side. Please consult ASIC datasheet if it already has 100ohm or equivalent internal termination. If so, do not connect external 100ohm across as shown in Fig. 6. This popular termination's advantage is that it does not allow any bias through from Vcc. This prevents Vcc system noise coupling onto clock trace.

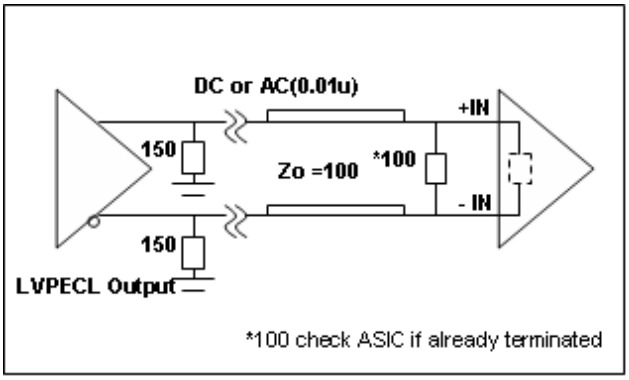


Fig. 6 LVPECL Output Popular Termination

LVPECL Output Thevenin Termination

Fig. 7 shows LVPECL output Thevenin termination which is used for shorter trace drive (<5in.), but it takes Vcc bias current and Vcc noise can get onto clock trace. It also requires more component count. So it is seldom used today.

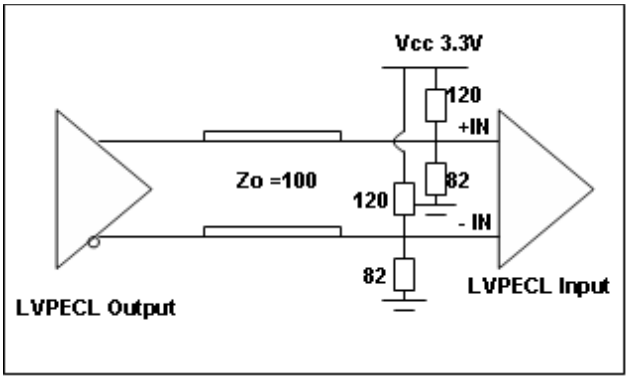


Fig. 7 LVPECL Thevenin Output Termination

LVPECL Output AC Thevenin Termination

LVPECL AC Thevenin terminations require a 150ohm pull-down before the AC coupling capacitor at the source as shown in Fig. 8. Note that pull-up/down resistor value is swapped compared to Fig. 7. This circuit is good for short trace (<5in.) application only.

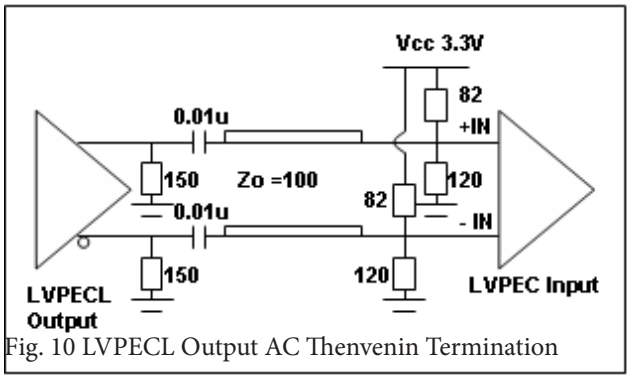


Fig. 10 LVPECL Output AC Thenvenin Termination

LVPECL Output Drive HCSL Input

Using the LVPECL output to drive a HCSL input can be done using a typical LVPECL AC Thenvenin termination scheme. Use pull-up/down 450/60ohm to generate Vcm=0.4V for the HCSL input clock. This termination is equivalent to 50Ohm load as shown in Fig. 9.

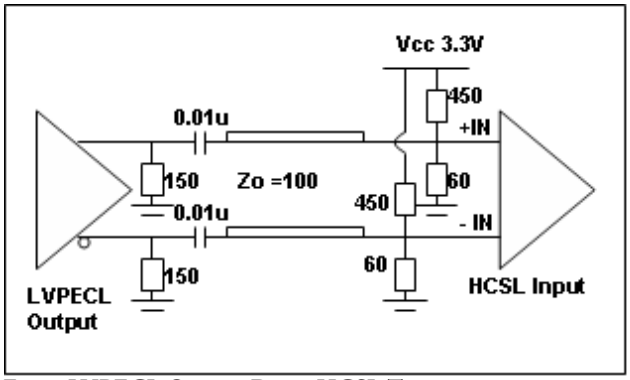


Fig. 9 LVPECL Output Drive HCSL Termination

LVPECL Output V_swing Adjustment

It is suggested to add another cross 100ohm at TX side to tune the LVPECL output V_swing without changing the optimal 150ohm pull-down bias in Fig. 10. This form of double termination can reduce the V_swing in ½ of the original at the RX side. By fine tuning the 100ohm resistor at the TX side with larger values like 150 to 200ohm, one can increase the V_swing by > 1/2 ratio.

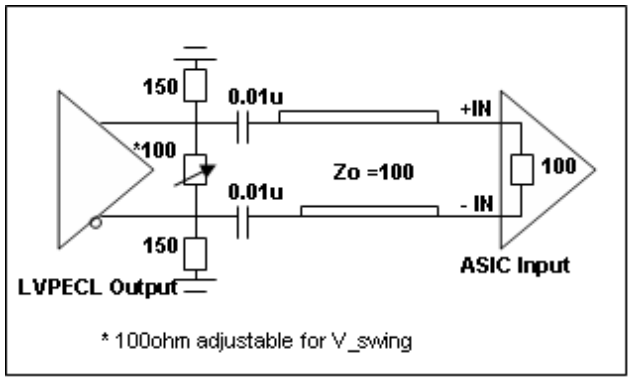


Fig. 10 LVPECL Output V_swing Adjustment

Clock Jitter Definitions

Total jitter= RJ + DJ

Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter: , where is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

Phase Jitter

Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz@10kHz which is phase noise power in 1-Hz normalized bandwidth vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter <=1ps at 12k to 20MHz offset band as SONET standard specification.

PCIe Ref_CLK Jitter

PCIe reference clock jitter specification requires testing via the PCI-SIG jitter tool, which is regulated by US PCI-SIG organization. The jitter tool has PCIe Serdes embedded filter to calculate the equivalent jitter that relates to data link eye closure. Direct peak-peak jitter or phase jitter test data, normally is higher than jitter measure using PCI-SIG jitter tool. It has high-frequency jitter and low-frequency jitter spec. limit. For more information, please refer to the PCI-SIG website: http://www.pcisig.com/specifications/pciexpress/

Device Thermal Calculation

Fig. 11 shows the JEDEC thermal model in a 4-layer PCB.

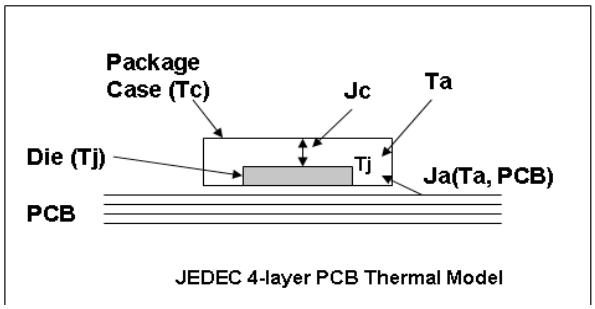


Fig. 11 JEDEC IC Thermal Model

Important factors to influence device operating temperature are:

1) The power dissipation from the chip (P_chip) is after subtracting power dissipation from external loads. Generally it can be the no-load device Idd

2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker has better heat dissipation

3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature Tj

The individual device thermal calculation formula:

Tj =Ta + Pchip x Ja

Tc = Tj - Pchip x Jc

Ja ___ Package thermal resistance from die to the ambient air in C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce Ja (still air) by 20~30%

Jc ___ Package thermal resistance from die to the package case in C/W unit

Tj ___ Die junction temperature in C (industry limit <125C max.)

Ta ___ Ambiant air température in C

Tc ___ Package case temperature in C

Pchip___ IC actually consumes power through Iee/GND current

Thermal calculation example
To calculate Tj and Tc of PI6CV304 in an SOIC-8 package:
Step 1: Go to Pericom web to find Ja=157 C/W, Jc=42 C/W
http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Step 2: Go to device datasheet to find Idd=40mA max.

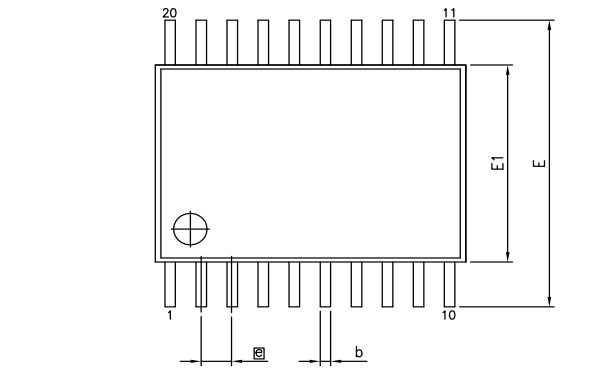
I_{DD}	Supply Current	C_L = 33pF/33MHz		20		mA
		C_L = 33pF/66MHz		40		
		C_L = 22pF/80MHz		35		
		C_L = 15pF/100MHz		32		
		C_L = 10pF/125MHz		28		
		C_L = 10pF/155MHz		41		

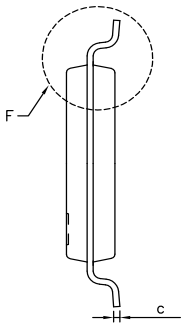
Step 3: P_total= 3.3Vx40mA=0.132W
Step 4: If Ta=85C
Tj= 85 + Ja xP_total= 85+25.9 = 105.7C
Tc= Tj + Jc xP_total= 105.7- 5.54 = 100.1C
Note:
The above calculation is directly using Idd current without subtracting the load power, so it is a conservative estimation. For more precise thermal calculation, use P_unload or P_chip from device Iee or GND current to calculate Tj, especially for LVPECL buffer ICs that have a 150ohm pull-down and equivalent 100ohm differential RX load.

Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	84.0 ^{O}C/W
Θ_{JC}	Junction-to-case thermal resistance		17.0 ^{O}C/W

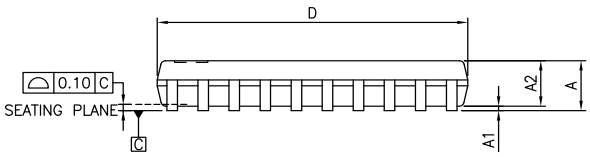
Packaging Mechanical: 20-Contact TSSOP (L)

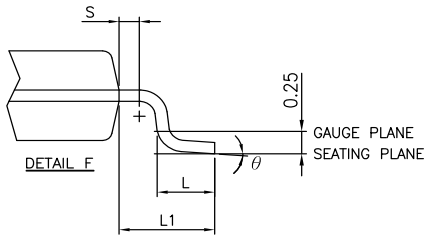




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





Notes:
1. Refer JEDEC MO-153F/AC
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 20-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1311 **REVISION: F**

12-0373

Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6C4911506LIE	L	Pb-free & Green, 20-pin TSSOP	Industrial

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging