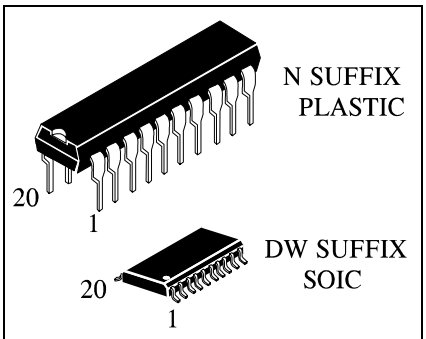
# KK74HCT373A

# Octal 3-State Noninverting Transparent Latch




**ORDERING INFORMATION**
KK74HCT373AN Plastic
KK74HCT373ADW SOIC
$T_A$ = -55° to 125° C for all packages

The KK74HCT373A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

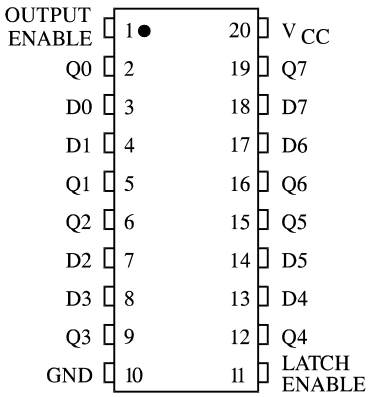
The KK74HCT373A is identical in pinout to the LS/ALS373.

The eight latches of the KK74HCT373A are transparent D-type latches. While the Latch Enable is high the Q outputs follow the Data Inputs. When Latch Enable is taken low, data meeting the setup and hold times becomes latched.

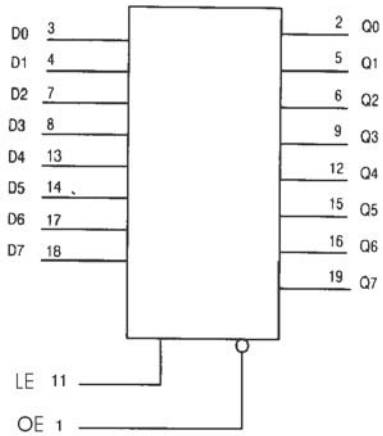
The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA

## PIN ASSIGNMENT




## LOGIC DIAGRAM




PIN 20=$V_{CC}$
PIN 10 = GND

## FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| Output Enable | Latch Enable | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | No Change |
| H | X | X | Z |

X = Don't Care
Z = High Impedance

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | -1.5 to $V_{CC}$ +1.5 | V |
| $V_{OUT}$ | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC}$ +0.5 | V |
| $I_{IN}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | ±35 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±75 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP**<br>SOIC Package** | 750<br>500 | mW |
| Tstg | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | -55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND≤($V_{IN}$ or $V_{OUT}$)≤$V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 25 °C to -55°C | ≤85 °C | ≤125 °C | |
| $V_{IH}$ | Minimum High-Level Input Voltage | $V_{OUT}$=0.1 V or $V_{CC}$-0.1 V<br>$\|I_{OUT}\| \leq 20$ μA | 4.5<br>5.5 | 2.0<br>2.0 | 2.0<br>2.0 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low - Level Input Voltage | $V_{OUT}$=0.1 V or $V_{CC}$-0.1 V<br>$\|I_{OUT}\| \leq 20$ μA | 4.5<br>5.5 | 0.8<br>0.8 | 0.8<br>0.8 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \leq 20$ μA | 4.5<br>5.5 | 4.4<br>5.4 | 4.4<br>5.4 | 4.4<br>5.4 | V |
| | | $V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \leq 6.0$ mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| $V_{OL}$ | Maximum Low-Level Output Voltage | $V_{IN}$= $V_{IL}$ or $V_{IH}$<br>$\|I_{OUT}\| \leq 20$ μA | 4.5<br>5.5 | 0.1<br>0.1 | 0.1<br>0.1 | 0.1<br>0.1 | V |
| | | $V_{IN}$= $V_{IL}$ or $V_{IH}$<br>$\|I_{OUT}\| \leq 6.0$ mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| $I_{IN}$ | Maximum Input Leakage Current | $V_{IN}$=$V_{CC}$ or GND | 5.5 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{OZ}$ | Maximum Three-State Leakage Current | Output in High-Impedance State<br>$V_{IN}$= $V_{IL}$ or $V_{IH}$<br>$V_{OUT}$=$V_{CC}$ or GND | 5.5 | ±0.5 | ±5.0 | ±10 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{IN}$=$V_{CC}$ or GND<br>$I_{OUT}$=0μA | 5.5 | 4.0 | 40 | 160 | μA |
| $\Delta I_{CC}$ | Additional Quiescent Supply Current | $V_{IN}$=2.4 V, Any One Input<br>$V_{IN}$=$V_{CC}$ or GND,<br>Other Inputs | | ≥-55°C | | 25°C to 125°C | mA |
| | | $I_{OUT}$=0μA | 5.5 | 2.9 | | 2.4 | |

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ =5.0 V ± 10%, $C_L$=50pF, $t_r$=$t_f$=6.0 ns)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|
| | | 25 °C to -55°C | ≤85°C | ≤125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input D to Q (Figures 1 and 5) | 28 | 35 | 42 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay , Latch Enable to Q (Figures 2 and 5) | 32 | 40 | 48 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay ,Output Enable to Q (Figures 3 and 6) | 30 | 38 | 45 | ns |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay , Output Enable to Q (Figures 3 and 6) | 35 | 44 | 53 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 5) | 12 | 15 | 18 | ns |
| $C_{IN}$ | Maximum Input Capacitance | 10 | 10 | 10 | pF |
| $C_{OUT}$ | Maximum Three-State Output Capacitance (Output in High-Impedance State) | 15 | 15 | 15 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Per Latch)<br>Used to determine the no-load dynamic power consumption:<br>$P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$ | $T_A$=25°C,$V_{CC}$=5.0 V<br>65 | | | pF |
| $t_{SU}$ | Minimum Setup Time, Input D to Latch Enable (Figure 4) | 10 | 13 | 15 | ns |
| $t_h$ | Minimum Hold Time,Latch Enable to Input D (Figure 4) | 10 | 13 | 15 | ns |
| $t_w$ | Minimum Pulse Width, Latch Enable (Figure 2) | 12 | 15 | 18 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times (Figure 1) | 500 | 500 | 500 | ns |

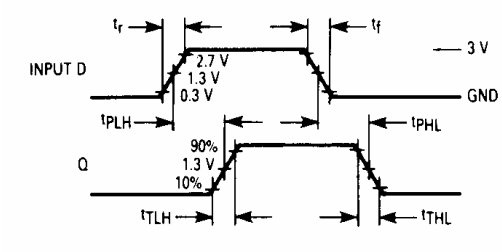



**Figure 1. Switching Waveforms**

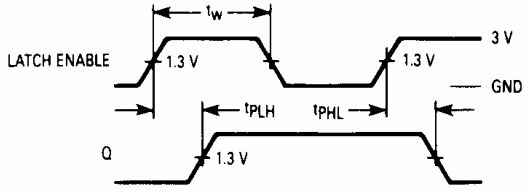



**Figure 2. Switching Waveforms**

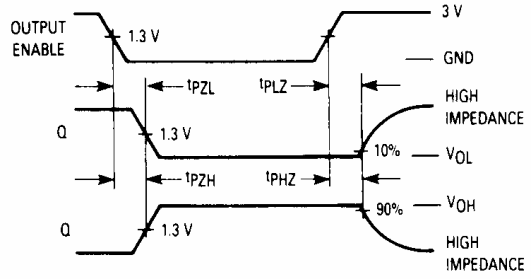



**Figure 3. Switching Waveforms**

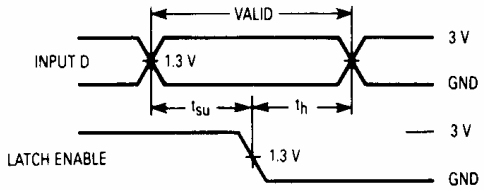



**Figure 4. Switching Waveforms**

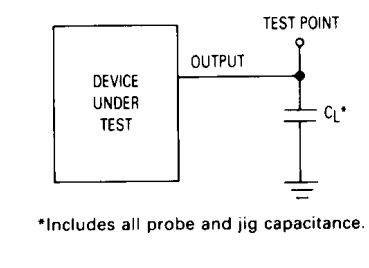



**Figure 5. Test Circuit**

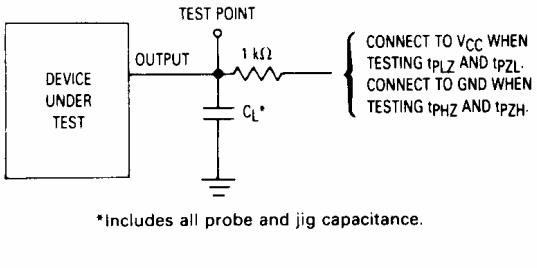
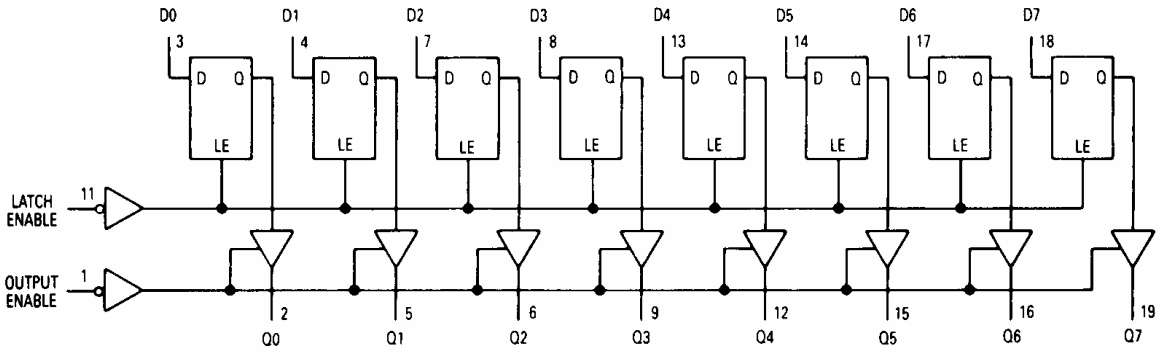
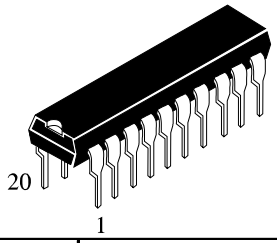


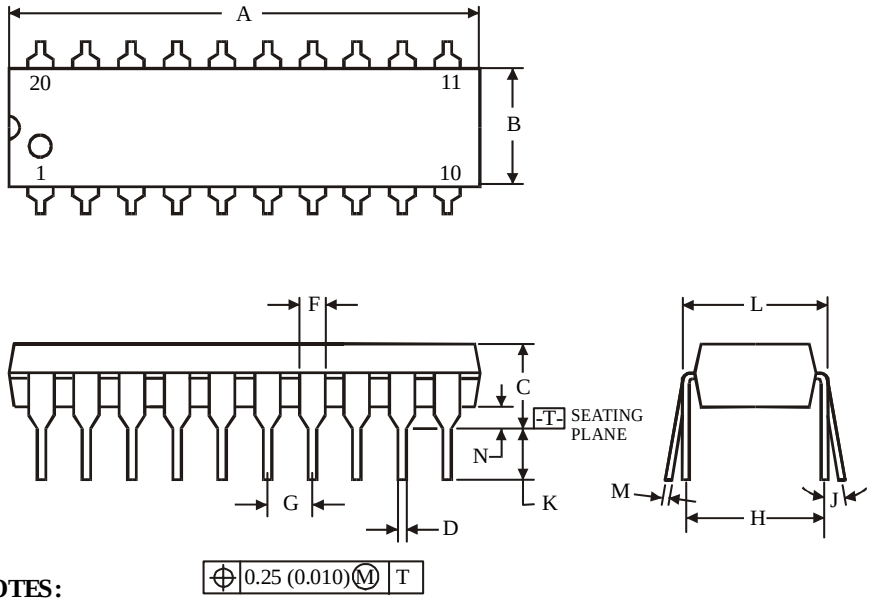

**Figure 6. Test Circuit**

## EXPANDED LOGIC DIAGRAM



## N SUFFIX PLASTIC DIP
## (MS - 001AD)




| | Dimension, mm | |
|---|---|---|
| Symbol | MIN | MAX |
| A | 24.89 | 26.92 |
| B | 6.1 | 7.11 |
| C | | 5.33 |
| D | 0.36 | 0.56 |
| F | 1.14 | 1.78 |
| G | 2.54 | |
| H | 7.62 | |
| J | 0° | 10° |
| K | 2.92 | 3.81 |
| L | 7.62 | 8.26 |
| M | 0.2 | 0.36 |
| N | 0.38 | |

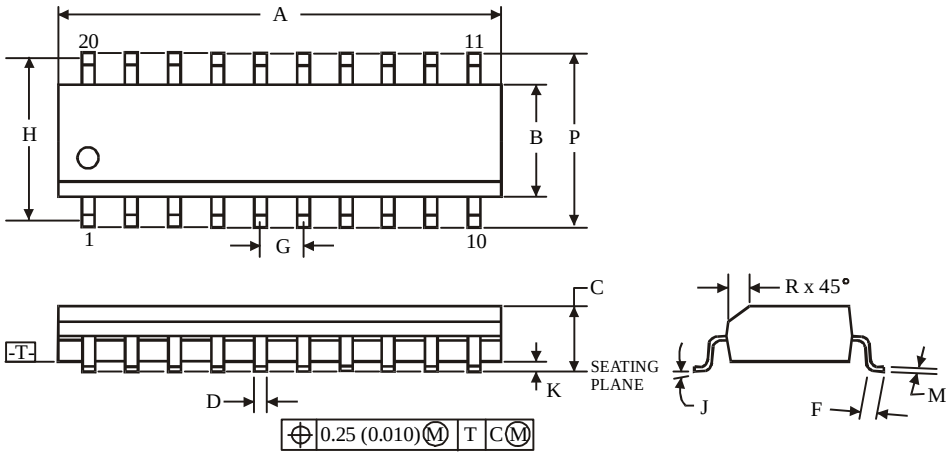
**NOTES:**

1. Dimensions “A”, “B” do not include mold flash or protrusions.

   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

## D SUFFIX SOIC
## (MS - 013AC)




| | Dimension, mm | |
|---|---|---|
| Symbol | MIN | MAX |
| A | 12.6 | 13 |
| B | 7.4 | 7.6 |
| C | 2.35 | 2.65 |
| D | 0.33 | 0.51 |
| F | 0.4 | 1.27 |
| G | 1.27 | |
| H | 9.53 | |
| J | 0° | 8° |
| K | 0.1 | 0.3 |
| M | 0.23 | 0.32 |
| P | 10 | 10.65 |
| R | 0.25 | 0.75 |

**NOTES:**

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B – 0.25 mm (0.010) per side.