

74AC843 • 74ACT843 9-Bit Transparent Latch

General Description

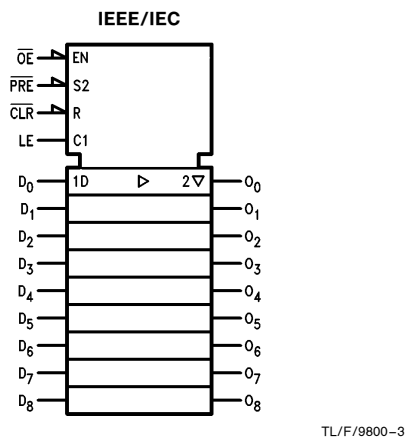
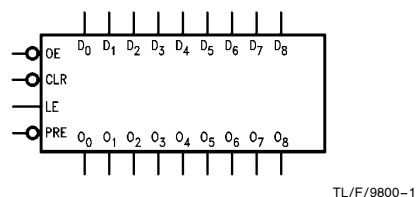
The 'AC/'ACT843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths.

The 'AC/'ACT843 is functionally and pin compatible with AMD's Am29843.

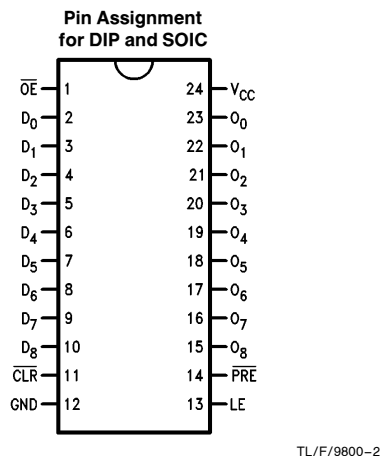
Features

- 'ACT843 has TTL-compatible inputs
- TRI-STATE® outputs for bus interfacing

Logic Symbols



Connection Diagram



Pin Names	Description
D ₀ -D ₈	Data Inputs
O ₀ -O ₈	Data Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable
$\overline{CLR}$	Clear
PRE	Preset

TRI-STATE® is a registered trademark of National Semiconductor Corporation
FACT™ is a trademark of National Semiconductor Corporation

Functional Description

The 'AC/'ACT843 consists of nine D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. In

addition to the LE and $\overline{OE}$ pins, the 'AC/'ACT843 has a Clear ($\overline{CLR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

Function Tables

Inputs					Internal	Outputs	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O	
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Clear/High Z
H	L	H	L	X	H	Z	Preset/High Z

H = HIGH Voltage Level

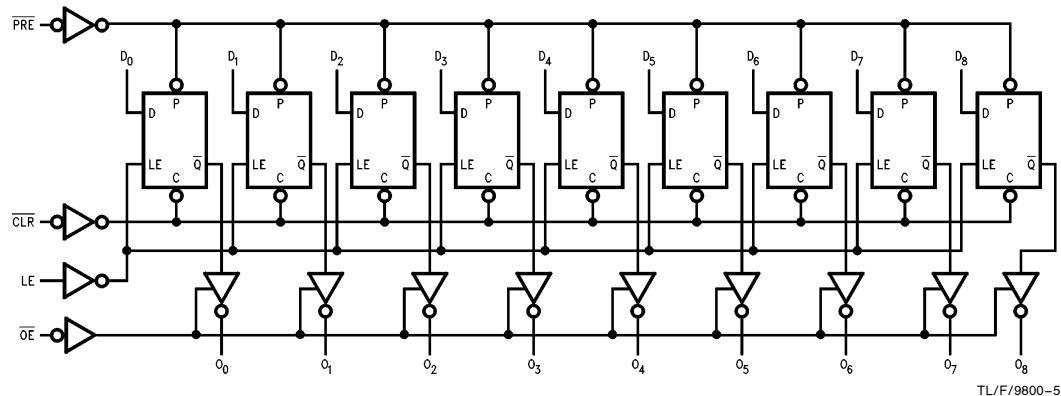
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

NC = No Change

Logic Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'AC Family Devices

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND

*All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
I _{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±5.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−75		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0		μA	V _{IN} = V _{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA	
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±5.0	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND	
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units
			T _A = + 25°C C _L = 50 pF			T _A = − 40°C to + 85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0	3.5 2.0	6.5 4.5	12.0 8.5	2.5 1.5	13.0 9.0	ns
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0	4.0 2.5	7.0 5.0	12.0 8.5	3.0 1.5	13.0 9.0	ns
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0	3.5 2.0	6.5 4.5	12.0 8.5	13.0 1.5	2.5 9.0	ns
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0	4.0 2.5	7.0 5.0	12.0 8.5	3.0 1.5	13.0 9.0	ns
t _{PLH}	Propagation Delay PRE to O _n	3.3 5.0	5.5 3.5	8.5 6.0	19.0 13.0	4.5 2.5	21.5 14.5	ns
t _{PHL}	Propagation Delay CLR to O _n	3.3 5.0	7.5 5.0	11.0 7.5	21.5 15.0	6.0 4.0	24.0 17.0	ns
t _{PZH}	Output Enable Time OE to O _n	3.3 5.0	3.5 2.0	6.0 4.5	11.0 8.0	3.0 1.5	12.0 9.0	ns
t _{PZL}	Output Enable Time OE to O _n	3.3 5.0	4.0 2.0	6.5 5.0	11.0 8.0	2.5 1.5	12.0 9.0	ns
t _{PHZ}	Output Disable Time OE to O _n	3.3 5.0	4.0 3.0	6.5 5.0	10.5 8.0	3.5 2.5	11.0 8.5	ns
t _{PLZ}	Output Disable Time OE to O _n	3.3 5.0	3.0 2.0	6.0 4.5	10.5 8.0	2.5 1.5	11.0 8.5	ns
t _{PHL}	Propagation Delay PRE to O _n	3.3 5.0	4.5 3.0	7.0 5.0	12.5 9.0	3.5 2.0	13.5 9.5	ns
t _{PLH}	Propagation Delay CLR to O _n	3.3 5.0	4.5 3.0	7.0 5.0	12.5 9.0	3.5 2.0	13.5 9.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Units
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW D _n to LE	3.3	0	3.0	3.5	ns
		5.0	−0.5	1.5	2.0	
t _h	Hold Time, HIGH or LOW D _n to LE	3.3		2.0	2.0	ns
		5.0	−0.5	2.5	2.5	
t _w	LE Pulse Width, HIGH	3.3	1.5	3.0	3.0	ns
		5.0	1.5	3.0	3.0	
t _w	$\overline{\text{PRE}}$ Pulse Width, LOW	3.3	5.0	12.0	14.5	ns
		5.0	3.0	8.5	10.0	
t _w	$\overline{\text{CLR}}$ Pulse Width, LOW	3.3	5.5	14.0	16.5	ns
		5.0	4.0	10.0	12.0	
t _{rec}	$\overline{\text{PRE}}$ Recovery Time	3.3	1.0	3.0	3.0	ns
		5.0	0	1.5	1.5	
t _{rec}	$\overline{\text{CLR}}$ Recovery Time	3.3	0	1.5	1.5	ns
		5.0	−0.5	0.5	0.5	

*Voltage Range 3.3 is 3.3V ±0.3V

*Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} [*] (V)	74ACT			74ACT		Units
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay D _n to O _n	5.0	2.5	5.5	9.5	2.0	10.0	ns
t _{PHL}	Propagation Delay D _n to O _n	5.0	2.5	5.5	9.5	2.0	10.0	ns
t _{PLH}	Propagation Delay LE to O _n	5.0	2.5	5.5	9.0	2.0	10.0	ns
t _{PHL}	Propagation Delay LE to O _n	5.0	2.5	5.5	9.0	2.0	10.0	ns
t _{PLH}	Propagation Delay PRE to O _n	5.0	2.5	6.5	14.0	2.0	16.0	ns
t _{PHL}	Propagation Delay CLR to O _n	5.0	2.5	7.5	15.5	2.0	17.5	ns
t _{PZH}	Output Enable Time OE to O _n	5.0	2.5	5.5	9.5	2.0	10.5	ns
t _{PZL}	Output Enable Time OE to O _n	5.0	2.5	5.5	9.5	2.0	10.5	ns
t _{PHZ}	Output Disable Time OE to O _n	5.0	2.5	6.0	10.5	2.0	11.0	ns
t _{PLZ}	Output Disable Time OE to O _n	5.0	2.5	6.0	10.5	2.0	11.0	ns
t _{PHL}	Propagation Delay PRE to O _n	5.0	2.5	6.0	10.5	2.0	11.0	ns
t _{PLH}	Propagation Delay CLR to O _n	5.0	2.5	5.5	9.5	2.0	10.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Units
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW D _n to LE	5.0	−0.5	0.5	1.0	ns
t _h	Hold Time, HIGH or LOW D _n to LE	5.0	0.5	2.0	2.0	ns
t _w	LE Pulse Width, HIGH	5.0	2.0	3.5	3.5	ns
t _w	$\overline{\text{PRE}}$ Pulse Width, LOW	5.0	5.0	8.5	10.0	ns
t _w	$\overline{\text{CLR}}$ Pulse Width, LOW	5.0	5.5	9.5	11.0	ns
t _{rec}	$\overline{\text{PRE}}$ Recovery Time	5.0	0.5	2.0	2.0	ns
t _{rec}	$\overline{\text{CLR}}$ Recovery Time	5.0	−0.5	1.0	1.0	ns

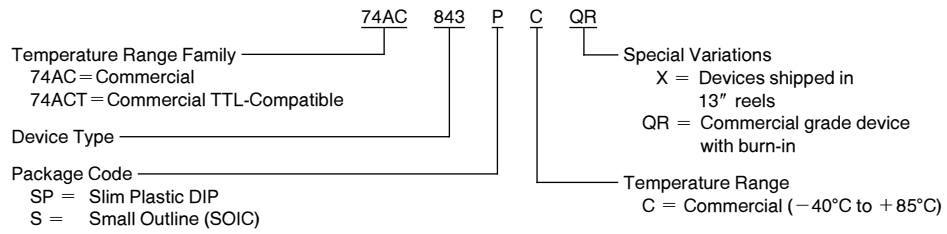
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = OPEN$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

Ordering Information

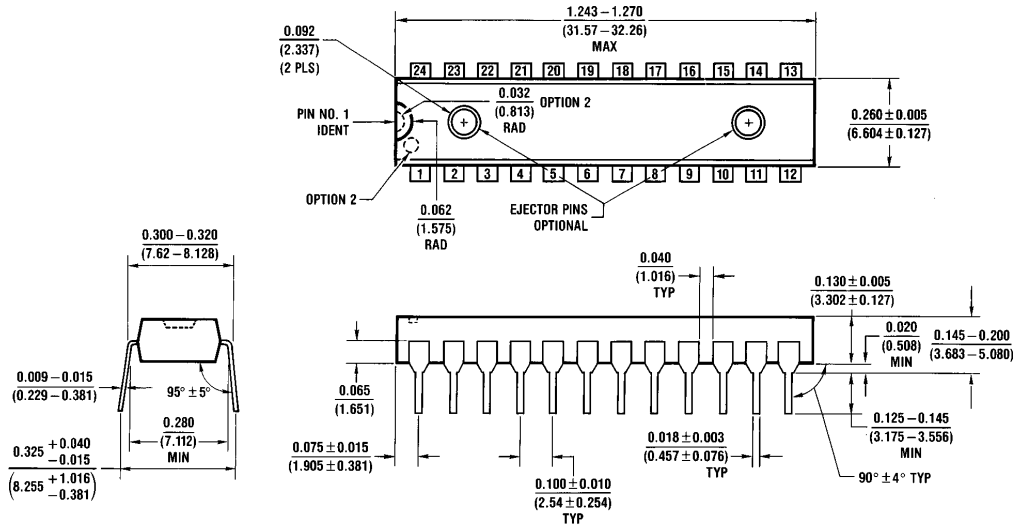
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



[illegible]

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114638



N24C (REV F)

24-Lead Slim (0.300" Wide) Plastic Dual-In-Line Package (SP)
NS Package Number N24C

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
 2900 Semiconductor Drive
 P.O. Box 58090
 Santa Clara, CA 95052-8090
 Tel: (408) 272-9959
 TWX: (910) 339-9240

National Semiconductor GmbH
 Livvy-Gargan-Str. 10
 D-82256 Fürstentfeldbruck
 Germany
 Tel: (81-41) 35-0
 Telex: 527849
 Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
 Sumitomo Chemical
 Engineering Center
 Bldg. 7F
 1-7-1, Nakase, Mihamu-ku
 Chiba-City,
 Chiba Prefecture 261
 Tel: (043) 299-2300
 Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
 13th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
 Rue Deputado Lacorda Franco
 120-3A
 Sao Paulo-SP
 Brazil 05418-000
 Tel: (55-11) 212-5066
 Telex: 391-1131931 NSBR BR
 Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty. Ltd.
 Building 16
 Business Park Drive
 Monash Business Park
 Nottingham, Melbourne
 Victoria 3168 Australia
 Tel: (3) 558-9999
 Fax: (3) 558-9998

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.