AN4382
Application note

100 W LED street lighting application using STLUX385A

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Introduction

The STEVAL385LEDPSR demonstration board is a complete and configurable solution that manages a single high brightness LED string using the STLUX385A digital controller and two stages of power conversion. The application consists of a PFC regulator followed by a zero voltage switching (ZVS) LC resonant stage. The LED current is adjusted using a primary side regulation (PSR) control technique. The LED brightness can be dimmed by controlling the LED current down to a very low level. Communication interfaces like DALI and UART are present, as well as an insulated 0 - 10 control input. This application note describes the use of the STEVAL385LEDPSR demonstration board, the hardware design and the firmware implementation. A real measurement is also described. For complete information on the STLUX385A digital controller, please refer to STLUX385A datasheet.

Danger: **High voltage is present on the PSR-ZVS demonstration board.**

Caution: This board shall be used by qualified and knowledgeable people due to internal high voltage. The user shall take great care when handling the demonstration board, even when no power is supplied.

Contents

1 **Board features 6**

Block diagram 6

2 **Getting started with STEVAL385LEDPSR demonstration board 7**

First power-on procedure 9

3 **PFC stage 11**

3.1 Constant T_{ON} working principles 11

3.2 Protections 12

3.3 Implementation on STLUX385A 13

3.4 PFC stage customization 14

3.4.1 Inductor 14

3.4.2 Output capacitor 14

3.4.3 Zero current detection circuit 15

4 **ZVS LC resonant stage description 16**

4.1 LC stage customization 17

4.1.1 Resonant Cell ZVS design 17

4.1.2 LC stage characteristic selection 19

4.1.3 Half bridge operating parameters 20

4.1.4 Transformer output voltage 21

4.2 Protections 22

4.3 ZVS LC resonant stage implementation on STLUX385A 22

5 **STLUX - pinout 24**

6 **Schematic diagrams 26**

7 **Bill of material 33**

8 **Board connector pinout 40**

9 **User interface 42**

9.1 Status LEDs 42

9.2 List of supported DALI commands 42
9.3 Serial command 46
9.3.1 ll - configure LED output current 47
9.3.2 st - status 49
9.3.3 gp - get PFC status 51
9.3.4 gh - get half bridge status 52
9.3.5 ad - get last ADC samples 53
9.3.6 ti - time since power-on 53
9.3.7 co - clear error 54
9.3.8 in - enabled/disable features 54
9.3.9 hf - configure half bridge deadtime 55
9.3.10 hb - configure half bridge frequency and status 56
9.3.11 pf - configure PFC voltage and status 56
9.3.12 dt -delay time compensation 57
9.4 Error codes 58
9.5 0 - 10 V interface 59

10 Measurements 60
10.1 Output current precision 61
10.2 Output current regulation 62
10.3 Efficiency 63
10.4 IDLE and minimum power 64
10.5 Demonstration board power factor and THD 65
10.6 PFC startup phases 66

11 Firmware download procedure 67

12 Revision history 69

List of tables

Table 1. List of STLUX385A pins used by the PFC stage . . . 13
Table 2. Current values . . . 19
Table 3. List of STLUX385A pins used by the ZVS LC stage . . . 22
Table 4. STLUX385A pinout . . . 24
Table 5. Bill of material . . . 33
Table 6. Connector J8 pinout - AC-DC input . . . 40
Table 7. Connector J4 pinout - DC output . . . 40
Table 8. Connector J3 pinout - DALI interfaces . . . 40
Table 9. Connector J9 pinout - 0 - 10 V . . . 40
Table 10. Connector J2 pinout - serial interfaces . . . 40
Table 11. Connector J1 pinout - SWIM interfaces . . . 41
Table 12. List of supported DALI commands . . . 42
Table 13. IEC62386 part 207 - command extension . . . 45
Table 14. “Il” <-> output current relation . . . 48
Table 15. Status information . . . 49
Table 16. PFC status information . . . 51
Table 17. Half bridge status information . . . 52
Table 18. ADC samples . . . 53
Table 19. Startup configuration . . . 54
Table 20. Error code . . . 58
Table 21. 0 - 10 V voltage to output current . . . 59
Table 22. Output current precision . . . 61
Table 23. Board standby and minimum power . . . 64
Table 24. Document revision history . . . 69

List of figures

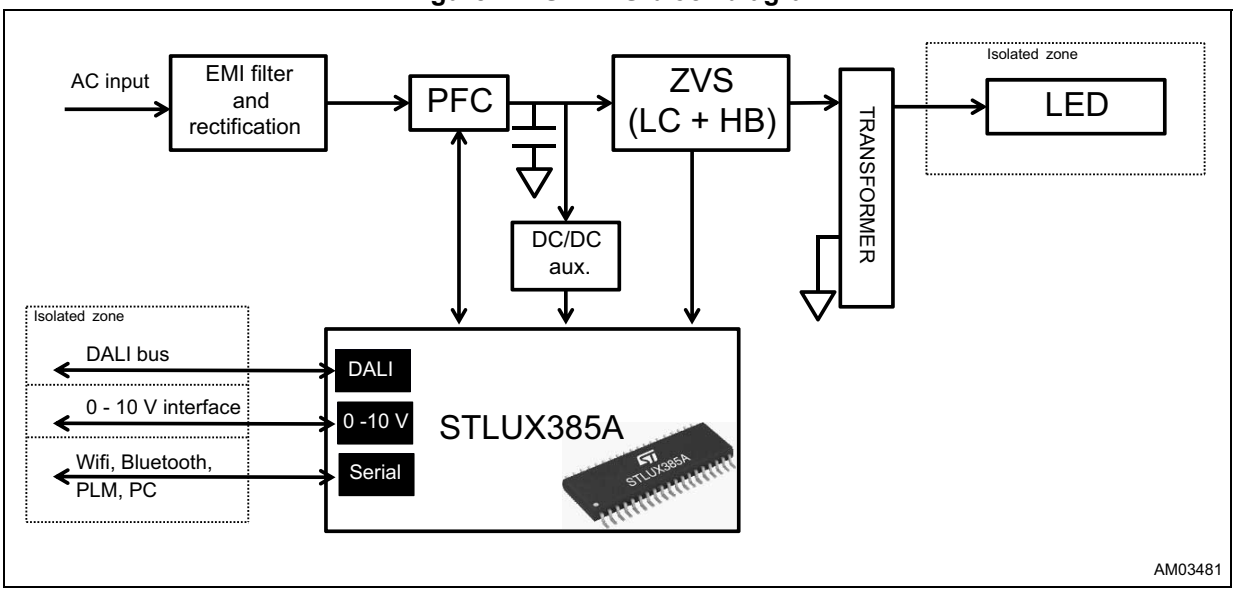
Figure 1. PSR-ZVS block diagram . . . 6
Figure 2. STLUX385A PSR-ZVS demonstration board . . . 7
Figure 3. STLUX385A PSR-ZVS board connections . . . 7
Figure 4. PFC concept . . . 11
Figure 5. PFC input current . . . 12
Figure 6. PFC logical implementation . . . 13
Figure 7. PFC - ZCD sensing . . . 15
Figure 8. ZVS concept . . . 16
Figure 9. ZVS - Λ vs. frequency . . . 18
Figure 10. ZVS output circuits . . . 21
Figure 11. Half bridge logical implementation . . . 23
Figure 12. PSR-ZVS demonstration board schematic - STLUX385A - top . . . 26
Figure 13. PSR-ZVS demonstration board schematic - PFC and DC/DC zone . . . 27
Figure 14. PSR-ZVS demonstration board schematic - PSR-ZVS stage . . . 28
Figure 15. PSR-ZVS demonstration board schematic - digital dimming stage . . . 29
Figure 16. PSR-ZVS demonstration board schematic - THD optimizer . . . 30
Figure 17. PSR-ZVS demonstration board schematic - DALI and 0 - 10 interfaces . . . 31
Figure 18. PSR-ZVS demonstration board schematic - serial interfaces . . . 32
Figure 19. Power-up message . . . 46
Figure 20. Command list . . . 47
Figure 21. Output current precision . . . 61
Figure 22. Output current ramp-up and down . . . 62
Figure 23. Demonstration board efficiency . . . 63
Figure 24. Standby power vs AC input voltage . . . 64
Figure 25. Demonstration board power factor . . . 65
Figure 26. Demonstration board current distorsion . . . 65
Figure 27. PFC startup at 110 Vac . . . 66
Figure 28. PFC startup at 220 Vac . . . 66
Figure 29. Program.bat screenshot . . . 67
Figure 30. Power-up message after a firmware update . . . 68
Figure 31. Power-up message of a fully enabled board . . . 68

1 Board features

- Wide input voltage range: 90 V to 265 V AC (50 or 60 Hz) compliant with IEC61000-3-2
- Single isolated output suitable for LED connection.
- Output voltage range (hardware configurable):
  - Standard version: 30 V to 100 V
  - High voltage version: 60 V to 200 V
- Output current and dimmability range:
  - Standard version: from 10 mA to 1000 mA
  - High voltage range: from 5 mA to 500 mA
- Output resolution: 11-bit equivalent.
- Maximum output power: 100 W
- Primary side control for higher efficiency (92% at full load)
- Faults detection and protection: short- or open circuit.
- IDLE mode power consumption: < 200 mW
- Remote control:
  - DALI command (IEC62386 - 201)
  - Isolated serial line
  - Isolated 0 - 10 V (alternative to DALI)
- Two status LEDs: green = ready-run-CPU load; red = fault
- Primary to secondary and interfaces isolation: 3750 V

Block diagram

Figure 1. PSR-ZVS block diagram



2 Getting started with STEVAL385LEDPSR demonstration board

This section is intended to provide directions to correctly connect, power up and control the demonstration board.

Danger: **Very high voltages are present on the board: suitable IPD ("Individual Protection Devices") and specific skills are required to operate on the board.**

Figure 2. STLUX385A PSR-ZVS demonstration board

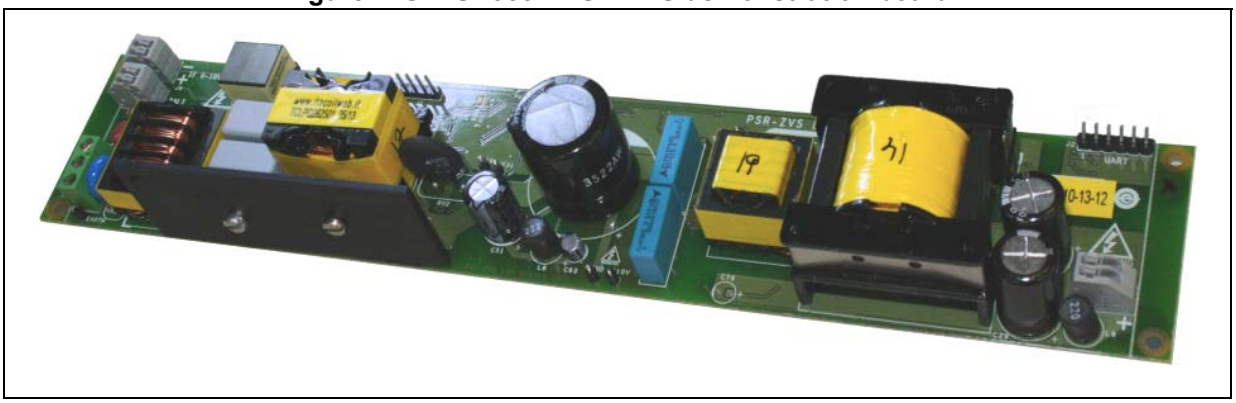
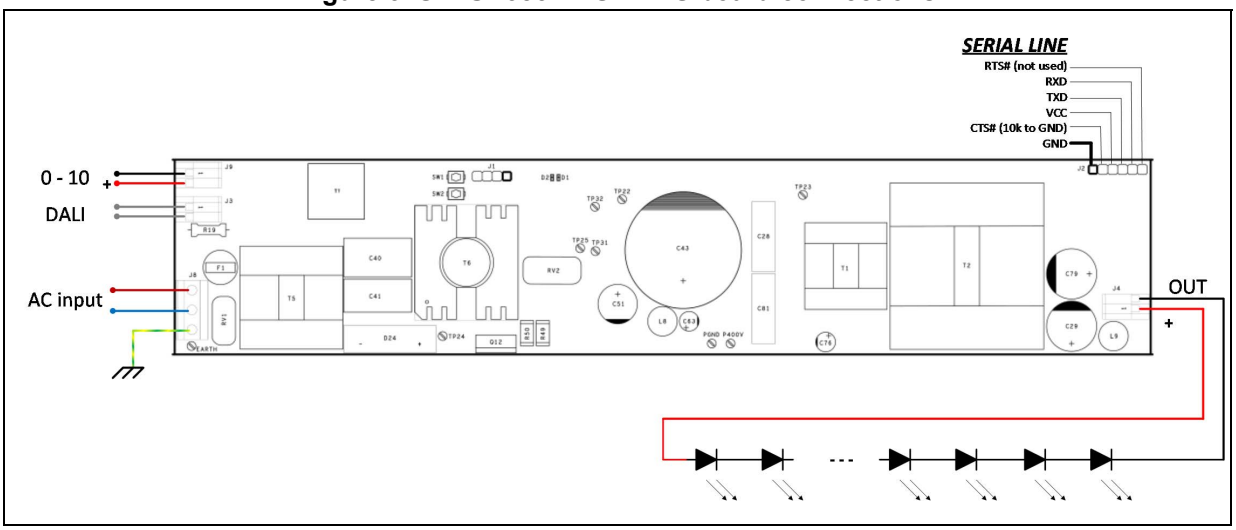


Figure 3. STLUX385A PSR-ZVS board connections



The LED string is not provided with the board and the user shall provide a suitable LED string with a total forward voltage and a maximum current rate that match the current board configuration (100 V at 1 A, 200 V at 0.5 A). The LED string is connected to the board output connector J4. The output power is isolated from the main AC input.

Caution: The user shall observe the correct string polarity as reported on the PCB.
An incorrect LED connection may damage the LED due to the high inverse voltage

The board supports a wide range AC input (J8 connector) and operates within the range 90 VAC - 265 VAC. This makes the board suitable to be connected directly into mains. The board also supports, on the same connector J8, a DC voltage comprised between 170 V and 350 V. The AC or DC connection to J8 is shown in *Figure 3*.

The STEVAL385LEDPSR demonstration board offers 3 different communication channels: DALI, 0 - 10 V and a serial interface. The DALI and 0 - 10 V interface share the same STLUX385A pins and are therefore mutually exclusive. The active line is selected via serial line commands.

The DALI interface can be controlled by any DALI master compliant with the IEC62386-201 standard. When the DALI protocol is used, the DALI bus must be connected before starting the application. An absence of the DALI line (OPEN DALI) for more than 500 mS from power-up causes the DALI interface to be disabled. When using the DALI interface, it is recommended that the DALI master is already “up and running” before connecting the board. The DALI connector is J3, it has no polarity and it is also isolated from the power stage. The DALI command set implemented on this board is described in *Chapter 9.2 on page 42*.

An isolated 0 - 10 V interface can be activated alternatively to the DALI bus when the DALI protocol is not required or is unavailable. The 0 - 10 V interface connector is J9 and is polarized.
A voltage below 1 V powers off the output LED strings. A voltage starting from 1 V to 10 V drives the output current from 10% to 100% of the maximum rated value, in a linear fashion. A voltage between 0 V and 1 V switches off the LED.

The serial line is accessible via the J2 connector and is isolated from the power stage.
A dedicated USB cable (e.g. TTL-232R-3V3 from FTDI) can be used to connect a personal computer with the serial interface and control the board using a terminal emulator software such as hyperterminal. The 2.54 mm connector of the USB cable shall be linked to the board so that the black wire is connected to the J2, pin1.

The serial input allows the user to interact with the board in parallel with the DALI bus. When the 0 - 10 V interface is selected, the output current is regulated only via the 0 - 10 V interface and no changes are allowed via the serial line. The serial line command set is described in *Chapter 9.3 on page 46*.

The STEVAL385LEDPSR can be set in a very low-power state, named IDLE, when the LEDs are switched off via DALI commands. During this state all operations are halted until a new DALI command is received or the DALI_RDY button is pushed. The serial line also stops to be active during the low-power mode.

First power-on procedure

The following section describes a step-by-step procedure which guarantees a correct power-on during the first configuration of the board.

This guide assumes that the STEVAL385LEDPSR demonstration board is tested using the following elements:

- A DALI master or a 0 - 10 V master line or the serial line.
- A USB TTL serial cable shipped with the board
- An AC Power supply or a DC power supply
- A computer running Microsoft® Windows®, Linux® or Apple® Mac OS® operating system and HyperTerminal or an equivalent terminal program.
- LED strings

Before first power-on the user shall connect the serial line as per the following instructions:

1. Connect the USB TTL serial cable to the USB port of the computer. Windows recognizes the cable as a new COM port and launches the driver installation.
2. Install the appropriate USB TTL serial cable drivers. The drivers are the “virtual COM port (VCP)” and they are provided by FTDI (http://www.ftdichip.com). If you need any help to install the drivers, please refer to your IT administrator. Once the drivers are installed, the Windows device manager panel shows a new USB serial port (COMx) device and the COM number associated.
3. Run Hyperterminal or an equivalent program from the computer connected to the COM port associated to the USB TTL serial cable. The serial connection configuration is:

- Baud rate 115200
- Data bits: 8
- Stop bits: 1
- Parity: no
- Flow control: no handshake

At any power-on of the board, the users shall verify the correct configuration of the board. The following instructions show a correct initialization of the board:

- The board input connector is J8 and the input voltage range goes from 96 VAC to 265 VAC (50 Hz or 60 Hz) or 170 VDC to 350 VDC. The user can supply the input from:
  - AC or DC power supply: configure the power supply output to one of the allowed input values; make sure that the power supply output is OFF and connect the power supply to J8.
  - Mains: make sure that the mains output is within the allowed range. Connect the power cable to J8 but do NOT plug the cable into a main socket.
- Connect the LEDs string to the connector J4. Verify the polarity: the LED string anode must be connected to “+” pole while the cathode follows the “-” pole. The LED string forward voltage and current must be within the current board configuration: 100 V (refer to *Section 4.1.4: Transformer output voltage on page 21*).
- Optionally connect the DALI or 0 - 10 V interface.
  - Connect the DALI line to the J3 connector (polarization is not important). Check with the serial line if this interface is enabling (default when the board is skipped).
  - Connect the 0 - 10 V line to the J9 connector (the interfaces is polarized). Check with the serial line if this interface is enabling (disabled when the board is skipped).
- Connect the serial cable to J2 using the USB TTL serial cable.
- Turn on the input power and verify that:
  - The RUN-FAULT LED goes on for few seconds before switching off. Should the RUN-FAULT LED stays ON than an error happened or that a protection is active. Switch off the board and investigate the problem.
  - The output current starts flowing in the LED string after less than 1 second. At power on the output current is low (~1% of total output power). The current level may vary depending on the external interfaces available:
- If the DALI bus is enabled and active, the output current is set to the “DALI power on level”.
- If the 0 - 10 V is enabled the output current defined by the voltage applied on J9.
- Verify the correct operation by changing the output current using alternatively DALI commands, 0 - 10 V or the serial command “ll”. Note that the serial “ll” command works only when the DALI and 0 - 10 are not active.

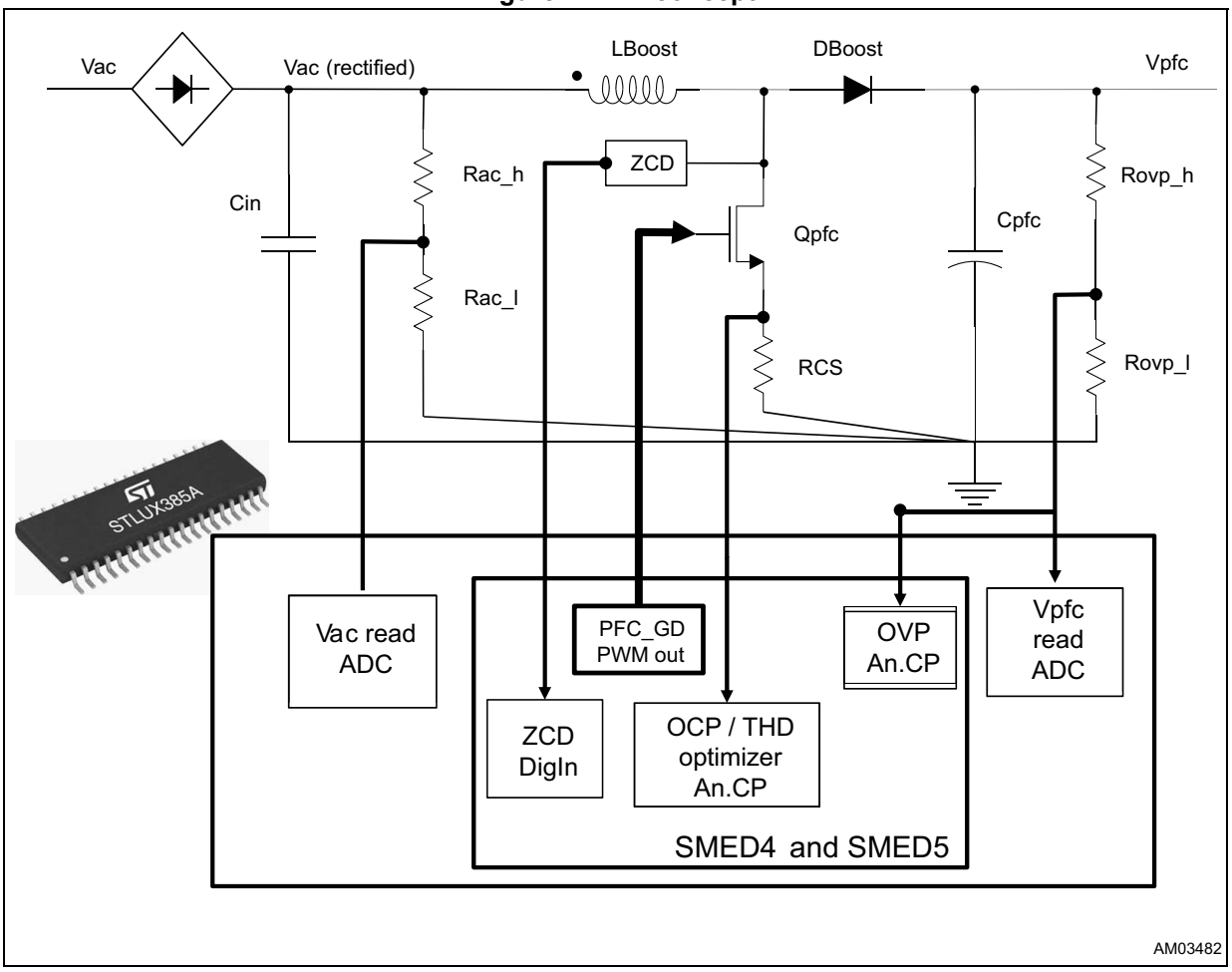
Should an error be detected (for example, no load condition) the PFC and ZVS stage are immediately switched off. See *Section 9.3.2: st - status on page 49* to debug the error code retrieved via the “st” command.

3 PFC stage

The STEVAL385LEDPSR demonstration board is based on two power conversion stages where a first PFC stage generates the DC voltage to apply to the LC resonant stage. The LC resonant stage controls the output current.

3.1 Constant T_{ON} working principles

Figure 4. PFC concept



The PFC stage is based on a boost converter operating in a transitional mode (also referred as critical conduction or a boundary mode) using the constant on-time method.

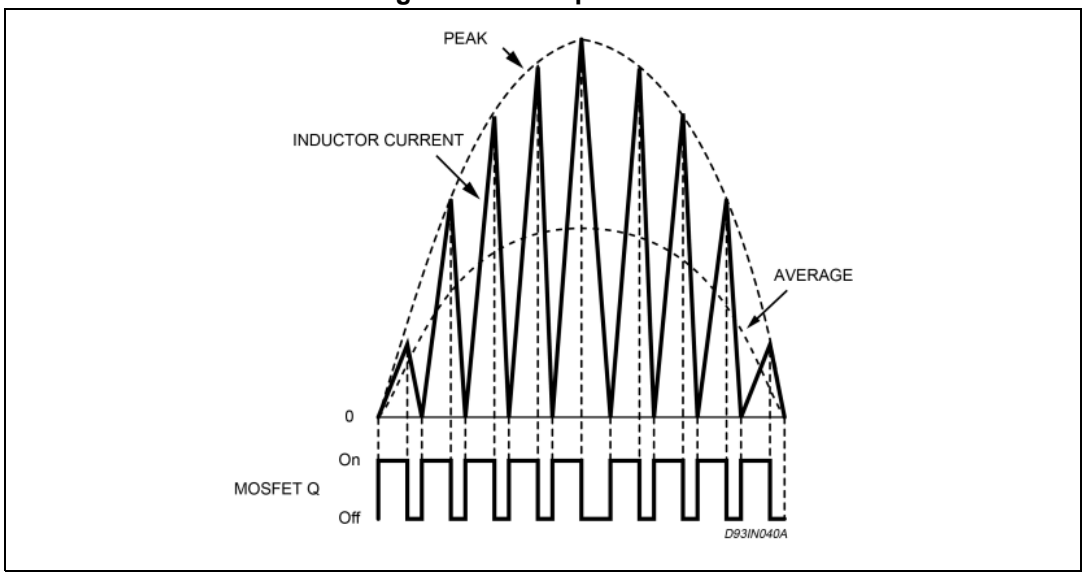
In boost topology the variation of the inductor current during the conduction time of the main switch (T_{ON}) depends on the input voltage as shown by *Equation 1*:

Equation 1

$$\Delta I_{Lboost} = Ton\frac{\sqrt{2}\cdot V_{ac}(\sin 2\pi \cdot f_{mains} \cdot t)}{L_{Boost}}$$

The conduction time (Ton) is the time the MOSFET remains on. Ton is updated every 100 µs and based on the PFC output voltage during the previous 200 ms. The PFC bandwidth is ~5 Hz. The boost MOSFET is turned on when the boost inductor current falls down to zero. The result of this algorithm is that the inductor current is shaped like a series of adjacent triangles whose peak's envelope is a half-wave sinusoid in phase with the AC input line voltage. For geometrical reason, the average current absorbed from the input line is also sinusoidal.

Figure 5. PFC input current



During light load conditions, a valley skipping mechanism is adopted, allowing a lower output voltage ripple and lower operating frequencies.

3.2 Protections

The STLUX385A device implements several protections that prevent the component degradation due to electrical overstresses or overheating. The protections implemented in the PFC stage are:

1. Overvoltage protection (OVP): stops the switching activity when the output capacitor voltage reaches a threshold. The PFC is turned on as soon as the capacitor voltage returns below the threshold.
2. Overcurrent protection (OCP): is activated when the inductor peak current reaches very high values during Ton (e.g. due to input overvoltage or output overloading). The current is read by the RCS shunt resistor and compared with a threshold. The threshold is dynamic and adjusted depending on the input voltage.
3. Brownout: When the input voltage is lower than a threshold the PFC stage is disabled. When the input voltage returns to acceptable levels, the PFC is turned on again. This prevents overstressing the PFC power components due to operations at very low input voltages.
4. Controlled soft start: the protection limits the charging current of the Cpfc capacitor. This method has two big advantages: a limited inrush current related with the PFC activation and better control of the output voltage that does not experience overshooting (and the audible noise associated).

3.3 Implementation on STLUX385A

The PFC stage is implemented exploiting the SMED technology used in the STLUX385A. In particular, two SMEDs, used in a coupled mode, are used to drive a single PWM output connected to the PFC MOSFET.

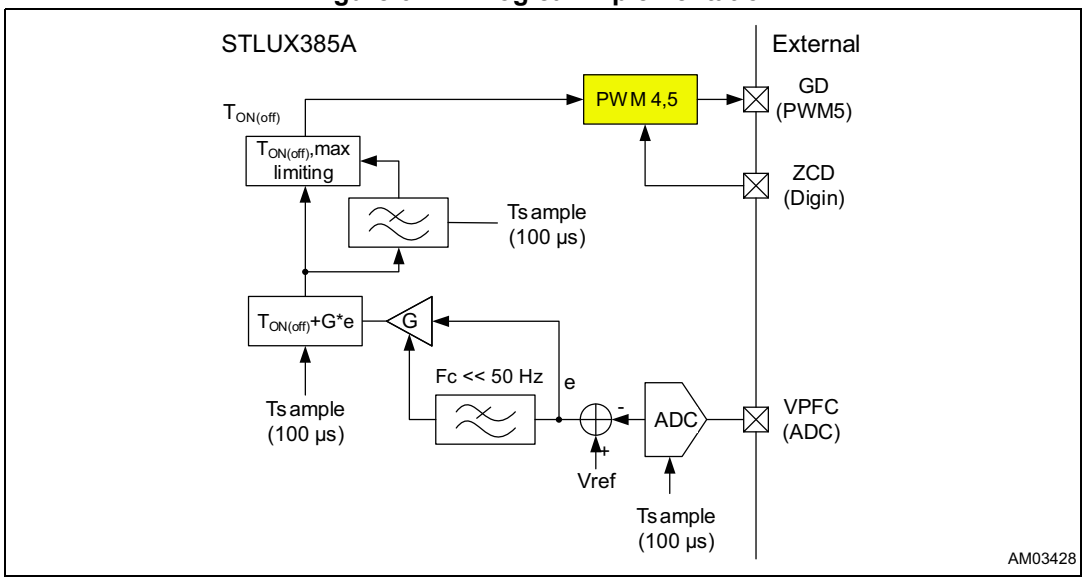
In *Table 1* is the list of the STLUX385A inputs and outputs used for the PFC stage:

Table 1. List of STLUX385A pins used by the PFC stage

Pin	Description
PWM5	Used as a PWM for the PFC MOSFET. It is internally driven by the SMED4 and SMED5
CPP0	Input for OVP protection
CPP2	Senses the current during Ton time
ADC0	PFC output voltage measurement
ADC3	Input voltage, phase and frequency measurement
DGIN3	“Zero Current Detection” input
DGIN2	Input THD optimizer

Figure 6 offers a system view on STLUX385A PFC implementation:

Figure 6. PFC logical implementation



The STLUX385A embeds the algorithms used to control the PFC behavior by regulating the PWM switching frequency. The correct switching parameters (Ton, Toff) are calculated starting from the PFC output voltage.

The system calculates the difference between the actual (ADC0) and the target (Vref) PFC output voltage. The error is firstly filtered by a 5 Hz low-pass filter obtaining a dynamic gain factor ranging from 1 x to 6 x. Every 100 µs, the new working parameters (Ton or Toff, depending on the load condition) are calculated by adding the error, amplified by the gain, to the current parameters. The output voltage is filtered by a 200 ms moving average window

technique. The algorithm also adapts the bandwidth to quickly react to fast variation of the input voltage or output load. The resulting bandwidth is then approximately equal to 5 Hz.

The CPP0 input is used to detect an overvoltage and switches off the PWM once the PFC voltage is greater than an internally configured safety threshold. The threshold is adjusted depending on the AC input voltage. Once the PFC output voltage reaches the safety threshold, the PWM is disabled within ~50 ns.

The PFC is activated 30 mS after power-on or activation. This time is used to sense the input AC voltage and enable the PFC with the optimal parameters for the given AC voltage.

The STLU385A also implements a THD optimizer approach (US2013194842 and US2013194845) via the DIGIN2 pin.

3.4 PFC stage customization

3.4.1 Inductor

The operating frequency of the PFC stage varies along every half cycle of the rectified AC input voltage and at different load conditions. The inductor value can be selected in order to obtain an operating frequency greater than a minimum value, normally ranging between 35 kHz and 60 kHz. *Equation 2* can be used to select the minimum operating frequency, using either minimum or maximum VAC value, whichever gives the lower value for L.

Equation 2

$$L_{Boost} = \frac{V_{ac}^2 \cdot (V_{pfc} - \sqrt{2}V_{ac})}{2\, f_{sw_min} \cdot P_{in} \cdot V_{pfc}}$$

The saturation current can be selected slightly higher than the maximum peak current occurring in correspondence of the peak of the input sine wave at full output power and low input voltage.

Equation 3

$$I_{Lsat} = 2 \cdot \sqrt{2} \frac{P_{in}}{V_{ac,min}}$$

Once obtained these two values, the inductor physical design can be done using one of the approaches described in some relevant application notes (see AN966 on www.st.com).

3.4.2 Output capacitor

The output capacitor is responsible for reducing the frequency ripple and maximizing the hold-up time. The operating frequency of the secondary LC stage is strongly dependent on its input voltage: it is therefore necessary to minimize the PFC output voltage ripple to avoid very wide frequency variation during the LC half bridge operations. The capacitor can be chosen according to *Equation 4*.

Equation 4

$$C_{pfc} \geq \frac{P_{out}}{4\pi \cdot f_{mains} \cdot V_{pfc} \cdot \Delta V_{pfc}}$$

The input filtering capacitor (Cin) and the offline EMI filtering are required to prevent that the high frequency noise, generated by both PFC and LC switching activity, is injected back to the input supply.

The STLUX385A device samples the PFC output voltage via a resistive voltage divider (see *Section 6: Schematic diagrams on page 26*: R46, R52, R55, R58, C49, C66). The voltage divider shall be set so that the PFC output voltage reference is divided down to 1.114 V input to the STLUX385A.

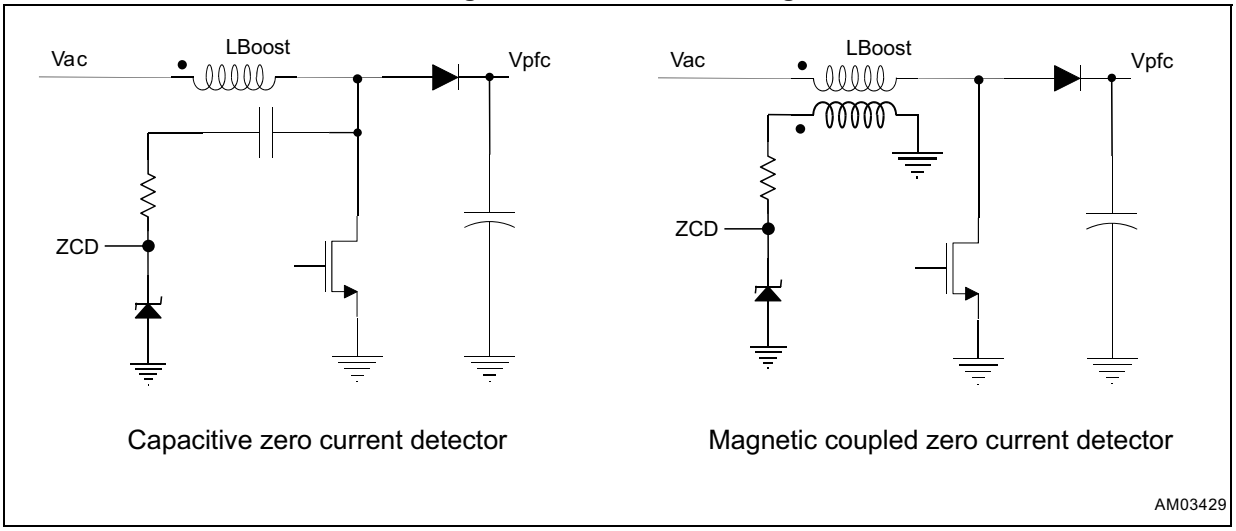
It is suggested to configure the PFC output voltage at least 25 V over the maximum voltage expected from the rectifying bridge. The STEVAL385LEDPSR demonstration board supports a PFC maximum input voltage equal to 375 V, therefore the PFC output voltage can be set to any value between 390 V and 415 V. The default value is 410 V.

3.4.3 Zero current detection circuit

The STLUX385A detects that the inductor current has fallen to zero via a “Zero Current Detection” circuit.

The STEVAL385LEDPSR demonstration board supports two different zero current detection mechanisms: one uses a capacitor between the MOSFET drain while the other connects an auxiliary winding across Lboost and detection input pin. In both cases suitable clamping devices (e.g. Zener diodes or current limiting resistors) are required. The board is currently configured to use the “Capacitive Zero Current” detection circuit.

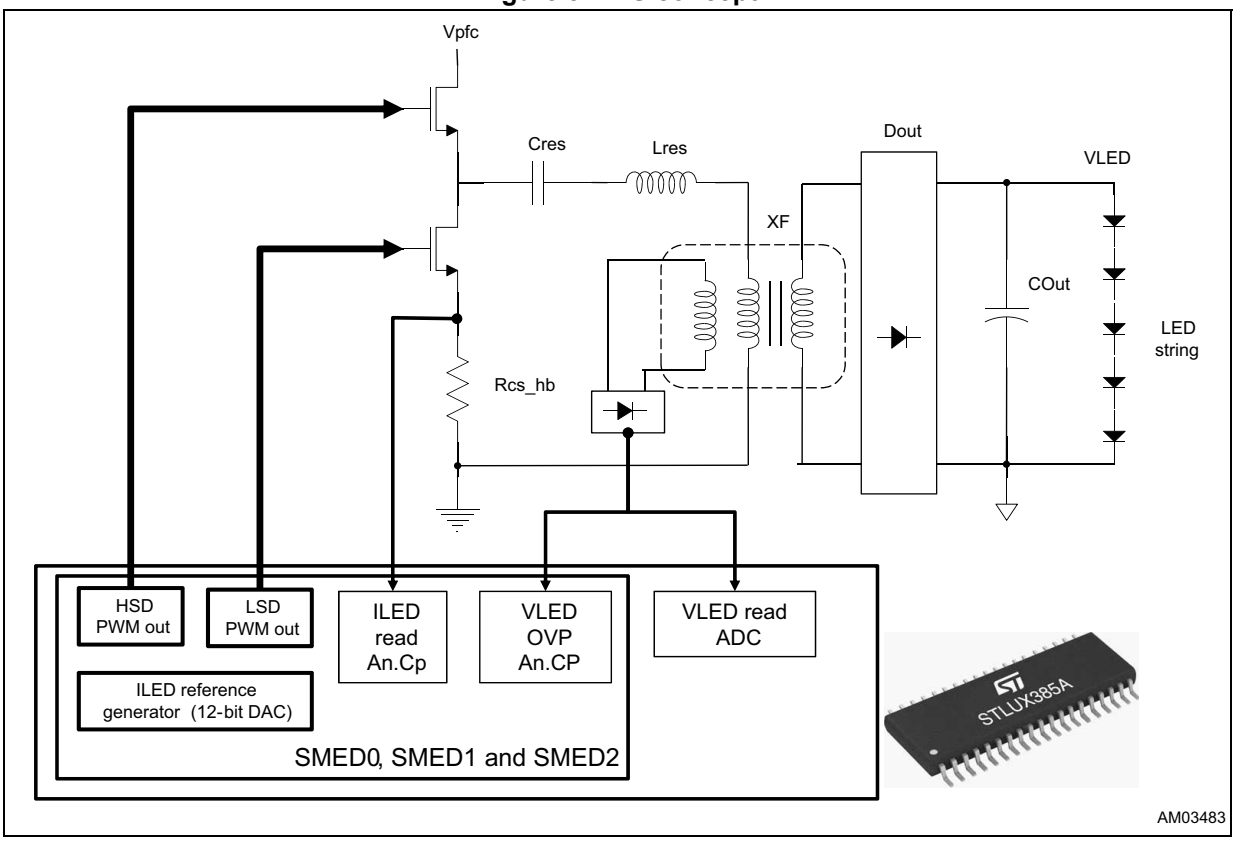
Figure 7. PFC - ZCD sensing



4 ZVS LC resonant stage description

The resonant stage is an LC topology consisting of a half bridge operating in “Zero Voltage Switching” condition supplying the resonant cell. The half bridge is connected to the PFC output. The LC stage (Cres, Lres) is separated from the transformer. The transformer XF is responsible for the energy transfer to the secondary side, where a rectifier circuit (Dout) and a filtering capacitor transform the AC current into a ripple free DC current required by the LEDs.

Figure 8. ZVS concept



The transformer XF is built in a way that maximize the winding coupling and operates similarly to an ideal transformer where the secondary side current is proportional to the primary side current and depends only on the transformer turn ratio (n = NPRI / NSEC). This proportionality is the key to control the secondary side current from the primary side.

The selection of Lres and Cres is made in order to operate above resonance in any condition therefore guaranteeing a soft switching behavior. The primary current has a triangular shape so that it can be stated that the average value of the LED current is equal to half of the peak of the resonant secondary current. Regulating the peak current during the low side conduction period and operating a 50% duty cycle then the primary side control of the output current is possible.

The transformer is coupled with an auxiliary winding which is used to measure at the primary side the reflected voltage and detect abnormal conditions such as short-circuit or no load.

4.1 LC stage customization

4.1.1 Resonant Cell ZVS design

In order to maintain the zero voltage switching condition *Equation 5* needs to be met.

Equation 5

$$n \cdot (VLED + Vdout) < \frac{1}{2} \cdot Vpfc$$

When the half bridge switching frequency (f_S) is close to the resonance frequency (f_R) then the shape of the resonant tank current is piecewise sinusoidal. Otherwise, when $f_S >> f_R$ then the shape of the resonant tank current is piecewise linear.

For the purpose of the analysis both the magnetizing current and the AC voltage across the tank capacitor Cres are negligible.

Considering that the square wave voltage applied to the resonant tank has 50% duty cycle, it is possible to state:

Equation 6

$$V(Cres) \approx \frac{1}{2} \cdot Vpfc$$

Furthermore the output current is given by the superposition of the currents through the secondary rectifier (Dout) and is a series of contiguous triangles. The DC output current is equal to half of the resonant current peak value multiplied by transfer ratio (n = NPRI / NSEC).

Equation 7

$$ILED \approx \frac{n}{2} \cdot Ires,pk$$

It can be demonstrated that the switching frequency of the converter is represented by *Equation 8*:

Equation 8

$$f_{hb} = \frac{n}{16 \cdot ILED \cdot Lres} \cdot \frac{Vpfc^2 - [2n \cdot (VLED + Vdout)]^2}{Vpfc}$$

The half bridge frequency depends directly on the input voltage and inversely on the LED current and depends on the difference between the square of the input voltage and the reflected value of the output voltage.

It should be noted that the half bridge frequency has a hyperbolical behavior depending on the output power (ILED, VLED). This behavior is the main difference when compared to an LLC or LCC resonant converter (see AN2644 and AN2450 on www.st.com).

The LC minimum operating frequency is obtained at the maximum output current, maximum output voltage and minimum PFC output voltage. The maximum frequency is, instead, obtained at the minimum output current (ILED, min), minimum output voltage (consider short-circuit if required) and maximum input voltage.

It is useful, for further consideration to arrange *Equation 5* as:

Equation 9

$$n = \lambda \cdot \frac{Vpfc,min}{2(VLED + Vdout)} \quad \text{with } \lambda \in (0,1)$$

Then the ratio between minimum and maximum frequency can be expressed as:

Equation 10

$$\frac{f_{hb,max}}{f_{hb,min}} = \frac{ILED,min}{ILED,max} \cdot \frac{1}{Vpfc,min} \cdot \frac{Vpfc,max^2 - Vpfc,min^2 \cdot \left(\frac{\lambda \cdot Vdout}{VLED + Vdout}\right)^2}{Vpfc,min \cdot (1-\lambda^2)}$$

Equation 10 can be simplified as follows:

Equation 11

$$\frac{f_{hb,max}}{f_{hb,min}} = Idim \frac{\Gamma}{(1-\lambda^2)} \quad \text{with} \quad \Gamma = \frac{Vpfc,max}{Vpfc,min} \quad \text{and} \quad Idim = \frac{ILED,min}{ILED,max}$$

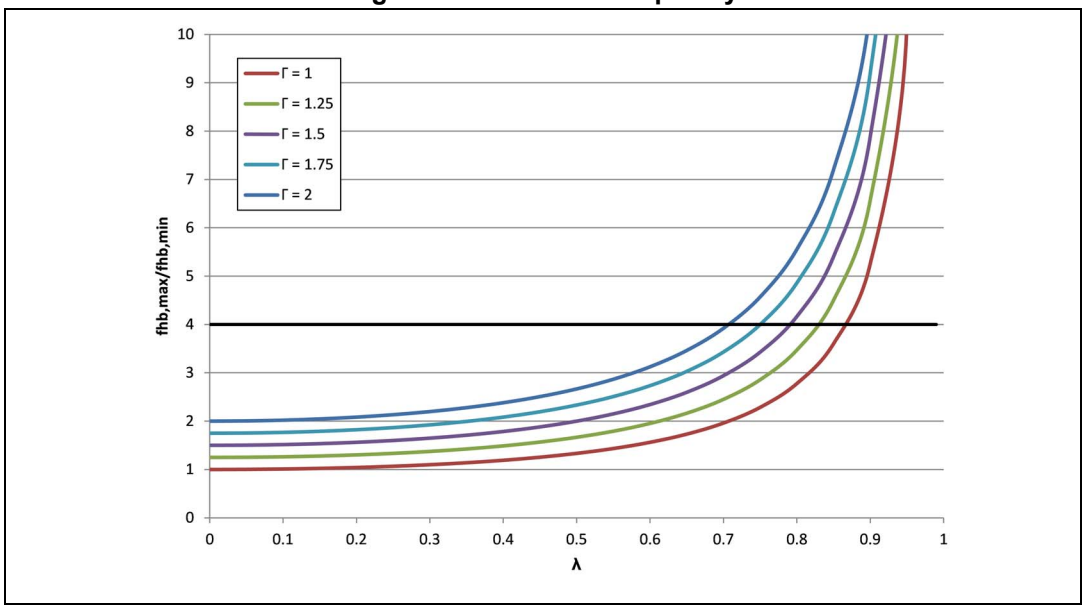
Keeping into consideration transient effects and current variations, it is a good empiric design practice to have:

Equation 12

$$\frac{f_{hb,max}}{f_{hb,min}} \leq 4$$

The parameter Γ is directly related with the ripple superimposed to the PFC output voltage. An indication about the required transformer ratio is obtained combining *Equation 11* and *Equation 9*. A representation of the frequency range at a fixed current versus Λ at different values of the parameter Γ is shown in *Figure 9*.

Figure 9. ZVS - Λ vs. frequency



4.1.2 LC stage characteristic selection

The following procedure can be used to determine the main component values.

Step1: Determine the primary-to-secondary turn ratio *n* of the transformer.

From *Equation 11* we derive:

Equation 13

$$\lambda = \sqrt{1 - \frac{Vpfc,max}{Vpfc,min} \cdot \frac{f_{hb,max}}{f_{hb,min}}}$$

Use *Equation 14* to calculate Λ for maximum LED current.

Note: $f_{hb,max}$ and $f_{hb,max}$ shall be selected so that Λ < 0.9 in order to account for rounding errors, mismatch and tolerances in the transformers.

Equation 15 can now be used to calculate the transformer transfer ratio *n* as:

Equation 14

$$n = \frac{NPRI}{NSEC} = \lambda \cdot \frac{Vpfc,min}{2(VLED + Vdout)}$$

Vdout is the forward voltage of the output rectified (0.5 V for a Schottky rectifiers, 0.8 V for p-n rectifiers or Shottky based Wien bridge rectifiers).

Step 2: Use *Table 2* to calculate the current in different point of the circuit.

Table 2. Current values

Parameter	Primary side	Secondary side
Peak current	$Ippk = \frac{2}{n} ILED$	$Ispk = 2 \cdot ILED$
Total current swing	$\Delta Ip = 2 \cdot Ippk = \frac{4}{n} ILED$	$\Delta Is = Ispk = 2 \cdot ILED$
DC current	$Ipdc = 0$ $Ipav = \frac{1}{n} ILED$ $Iin = \frac{ILED \cdot (VLED + Vdout)}{Vpfc}$	$Isdc = ILED$
Total RMS current	$Iprms = \frac{2}{n\sqrt{3}} ILED$	$Isrms = \frac{2}{\sqrt{3}} ILED$
AC RMS current	$Ipac = \frac{2}{n\sqrt{3}} ILED$	$Isac = \frac{1}{\sqrt{3}} ILED$

Step 3: Calculate the inductance value of the Lres, which is given by *Equation 8* and *Equation 13*:

Equation 15

$$Lres = \frac{\lambda(1-\lambda^2)}{32 \cdot ILED \cdot f_{hb,min}} \cdot \frac{Vpfc,min^2}{(VLED + Vdout)}$$

Step 4: determine the capacitance value of the resonant capacitor Cres so that the peak amplitude of the AC ripple voltage is much lower (e.g always 10%) than the DC offset. Indicatively:

Equation 16

$$Cres \geq 5 \frac{ILED}{n \cdot Vpfc,min \cdot f_{hb,min}}$$

Step 5: select the output capacitors Co so that they are rated for the maximum output voltage VLED, they meet the output voltage ripple specification (if any) and have an adequate AC current ripple rating.

The output current ripple specification must be met. To do so, at first we need to find the value of the overall RLED for the LED string by considering the tangent to the forward characteristic in the specified operating point. Then *Equation 17* can be used to find the suitable value for Co and its ESR.

Equation 17

$$\frac{\Delta ILED}{ILED} \cdot RLED \geq \sqrt{\left(\frac{1}{4 \cdot Co \cdot f_{hb,min}}\right)^2 + 4 \cdot ESR^2}$$

The maximum allowed ripple current for Co must be:

Equation 18

$$\Delta ICo \geq \frac{ILED}{\sqrt{3}}$$

4.1.3 Half bridge operating parameters

In order to generate a proper oscillation into the LC resonant tank, the half bridge must generate a square wave having a 50% of duty cycle. Any unbalancing of this duty cycle may cause the loss of zero voltage switching condition and, as a consequence, increases the risk of components overstress.

The adoption of the same conduction time (Ton) for both the halfbridge MOSFETs ensures this condition. When one MOSFET is turned off then the middle point of the half bridge, thanks to resonance, moves to the opposite side of the half bridge, in a time that depends on the overall capacitance (real or parasitic) connected to this node.

In order to avoid undesired switching losses, a deadtime (see "*hf*" command), longer than this transition time , shall be applied between the time one side of the half-bridge switches off and the time the opposite side turns on.

In order to correctly regulate the LED current, it is important to accurately detect the instant of the peak of the resonant current. The peak is detected by the STLUX385A via a shunt resistor placed between the source of the low side MOSFET and ground. The sampling time

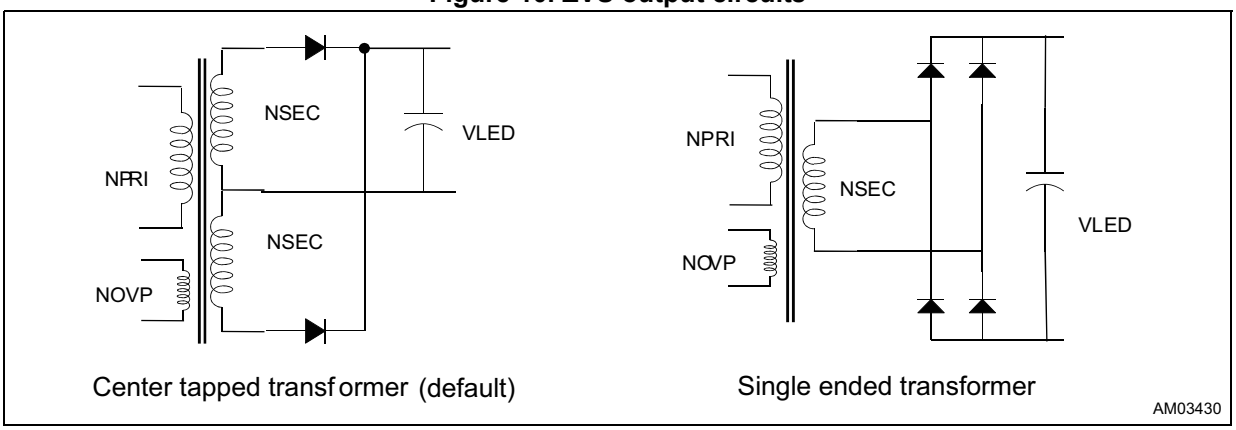
of the peak is therefore dependent on the propagation delay (~200 ns) generated by the driver and the MOSFET gate capacitance. An internal fixed STLUX385A delay shall be also considered (< 50 ns).

Given that the propagation time depends from the final board construction, the use shall measure the final propagation time and use the "*dt*" command to program the application specific propagation time.

4.1.4 Transformer output voltage

Transformer XF can be realized using a center tapped secondary side winding or a single ended secondary side. The structure of this component and the relevant rectifiers are shown in *Figure 10*.

Figure 10. ZVS output circuits



The transformer used in the STEVAL385LEDPSR demonstration board is configured as center tapped.

In order to change the output from the default 100 V (max 1 A) to 200 (max 0.5 A), the user shall perform the following steps:

- Mount the D42 and D43 with the 2 x STTH3R06S (SMC package)
- Remove the R102.

Note: The STTH3R06S component are not included in the STEVAL385LEDPSR demonstration board.

4.2 Protections

The STLUX385A offers several levels of protections:

1. Output undervoltage protection (UVP): prevents the LC resonant stage from operating when it's input voltage, i.e. the PFC output capacitor voltage, is at very low voltage. When an UVP condition arises, the STLUX385A stops the switching activity on the LC stage until the PFC voltage returns above an acceptable range.
2. No load: prevents the LC stage to operate while there is no LED string connected. This protection preserves the resonant output capacitors from being damaged due to overcharge. When the output capacitors voltage reaches a threshold, the STLUX385A disables the resonant activity within 50 ns.
3. Brownout protection: When the AC input voltage drops under 90 V the resonant stage is disabled at the same time as the PFC.
4. Short-circuit protection: the STEVAL385LEDPSR demonstration board architecture ensures that the output current in a short-circuit condition is always limited to the actual current level configured by the serial, DALI or 0 - 10 interface.

4.3 ZVS LC resonant stage implementation on STLUX385A

Similarly to the PFC stage, the LC resonant stage is driven by the SMED technology implemented by the STLUX385A. In particular, one SMED is used to control the half bridge high-side while another SMED controls the low-side. Using two SMEDs gives the STLUX385A full control over the half bridge conduction and deadtimes.

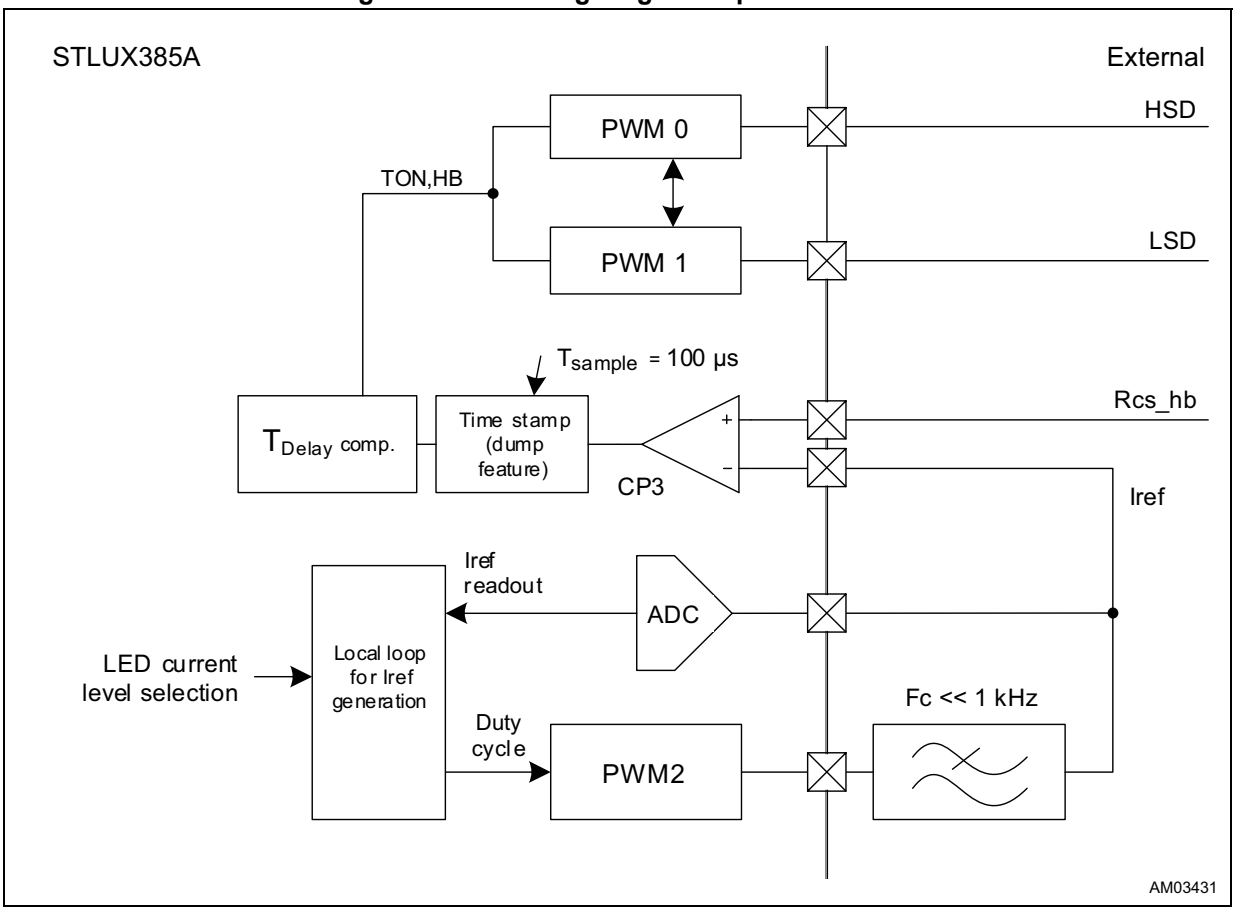
An additional PWM (SMED2) is used to feed a low-pass filter and generate a high precision signal with 12-bit resolution. The signal is monitored via ADC1 and continuously adjusted to compensate for the external circuit tolerance.

Table 3 shows the STLUX385A inputs and outputs used to control the resonant stage.

Table 3. List of STLUX385A pins used by the ZVS LC stage

Pin	Description
PWM0	PWM driving the half bridge low side MOSFET. The output is generated by SMED0.
PWM1	PWM driving the half bridge high side MOSFET. The output is generated by SMED1.
PWM2	Used to generate a high precision reference with 12 bit resolution. PWM2 is the input to an external low-pass filter which generates the reference.
PWM3	Used for synchronization.
DIGIN5	Used for synchronization.
CPP3	Monitors the current on half bridge.
CPM3	Input of the high precision reference
CPP1	Monitor for no load conditions. The half bridge operation is stopped when there is no load.
ADC1	Monitor for the high precision reference.
ADC2	Samples the scaled reflected voltage from the transformer.

Figure 11. Half bridge logical implementation



The control stage algorithm of the half bridge resonator makes sure that the half bridge is always driven at the correct frequency so that the amount of current sensed (CPP3) matches the target current (Iref) as selected by the user via the DALI, UART or the 0/10 interface.

The high precision signal generated by the PWM2 is used as a comparison with the actual current.

The control loop bandwidth is 10 KHz. The minimum allowed frequency is 70 KHz and maximum frequency is 400 KHz.

The STLUX385A limits the resonant output current increases or decreases rate to a maximum of 300 mA /second, in order to preserve both the output capacitors and the LED string.

5 STLUX - pinout

Table 4 describes the STLUX pins used by the STEVAL385LEDPSR demonstration board.

Table 4. STLUX385A pinout

Pin	Dir.	Function	Note
1	OUT	PWM [0]	Low side MOSFET driving signal for ZVS resonant stage (SMED0)
2	OUT/IN	DIGIN [0] /CCO	Used for internal synchronization OR a 0 - 10 V interface clock
3	IN	DIGIN [1]	Button used to initiate DALI identification procedure
4	OUT	PWM [1]	High side MOSFET driving signal for ZVS resonant stage (SMED1)
5	OUT	PWM [2]	PWM to generate high resolution reference signal (DAC) (SMED2)
6	IN	DIGIN [2]	THD optimizer input for the PFC stage
7	IN	DIGIN [3]	Zero current sensing for PFC stage
8	OUT	PWM [5]	PFC MOSFET driving signal (SMED5 and SMED4)
9	I/O	SWIM	SWIM connection
10	I/O	RESETn	Reset signal
11	PS	VDD	Power supply input
12	PS	VSS	Power supply reference voltage
13	PS	VOUT	Power supply reference voltage (core)
14	OUT	DALI TX	DALI transmit signal
15	IN	DALI RX	DALI receive signal
16	OUT	GPIO1 [4]	Reserved
17	IN	DIGIN [4]	Not assigned
18	IN	DIGIN [5]	Connected to PWM3 output
19	OUT	PWM [3]	Used for synchronization
20	OUT	GPIO0 [2]	Red LED - fault indication
21	OUT	GPIO0 [3]	Green LED - running, CPU load, indication
22	OUT	UART TX	UART TX signal
23	IN	UART RX	UART RX signal
24	A-IN	CPP3	Half bridge current sensing (SMED0)
25	A-IN	CPP2	PFC current sensing (SMED5)
26	A-IN	CMP3	Half bridge current reference (generated by PWM2)
27	A-IN	CPP1	Half bridge OVP detection (SMED1)
28	A-IN	CPP0	PFC OVP protection (SMED4)
29	PS	VDDA	Power supply input
30	PS	VSSA	Power reference voltage
31	A-IN	ADCIN [7]	Not assigned

Table 4. STLUX385A pinout (continued)

Pin	Dir.	Function	Note
32	A-IN	ADCIN [6]	3.3 V power voltage monitor
33	A-IN	ADCIN [5]	14 V power voltage monitor
34	A-IN	ADCIN [4]	0 - 10 voltage monitor
35	A-IN	ADCIN [3]	AC input voltage monitor
36	A-IN	ADCIN [2]	Half bridge auxiliary winding voltage sensing
37	A-IN	ADCIN [1]	Current reference compensation for PWM2
38	A-IN	ADCIN [0]	PFC output voltage monitor

6 Schematic diagrams

Figure 12. PSR-ZVS demonstration board schematic - STLUX385A - top

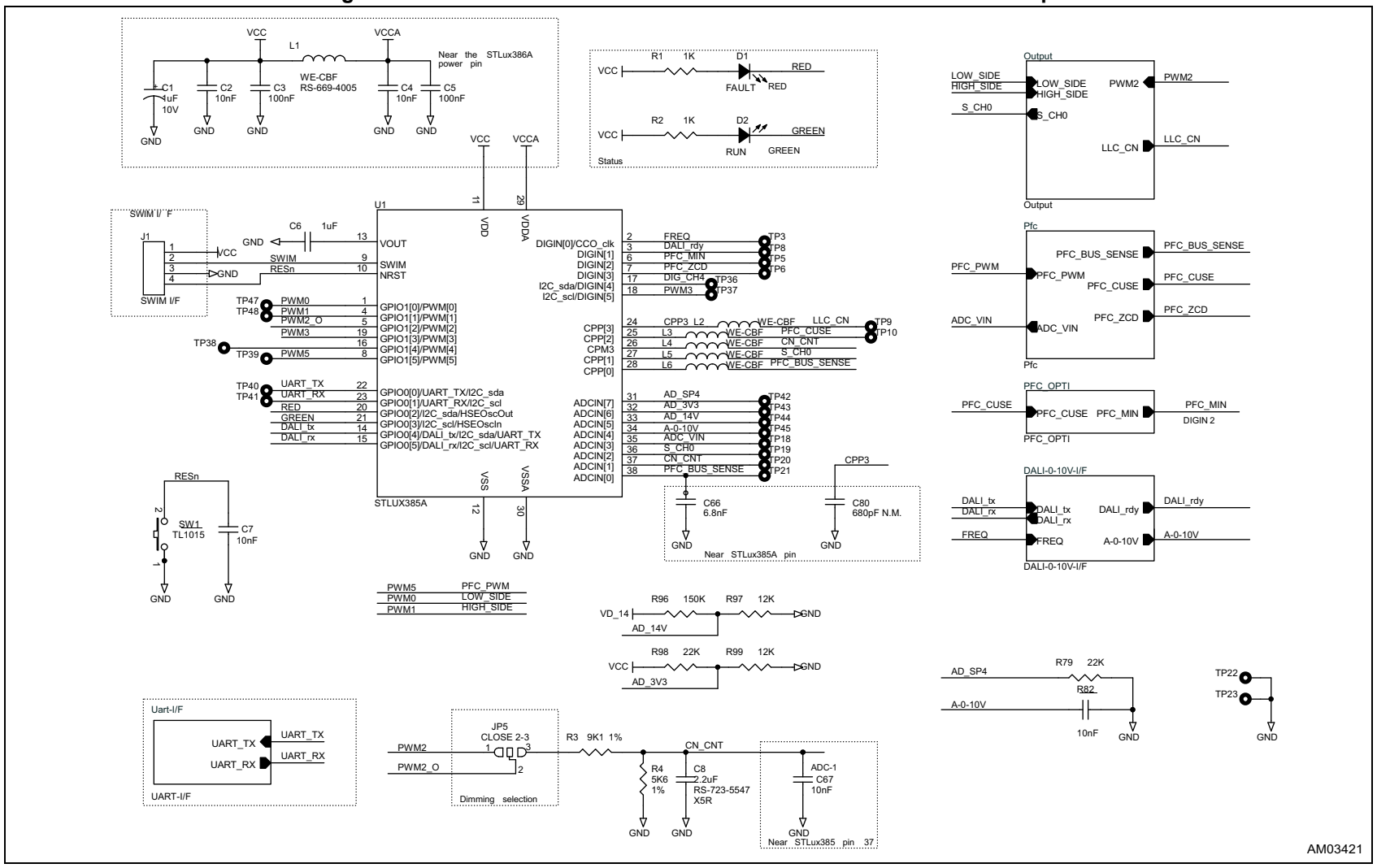


Figure 13. PSR-ZVS demonstration board schematic - PFC and DC/DC zone

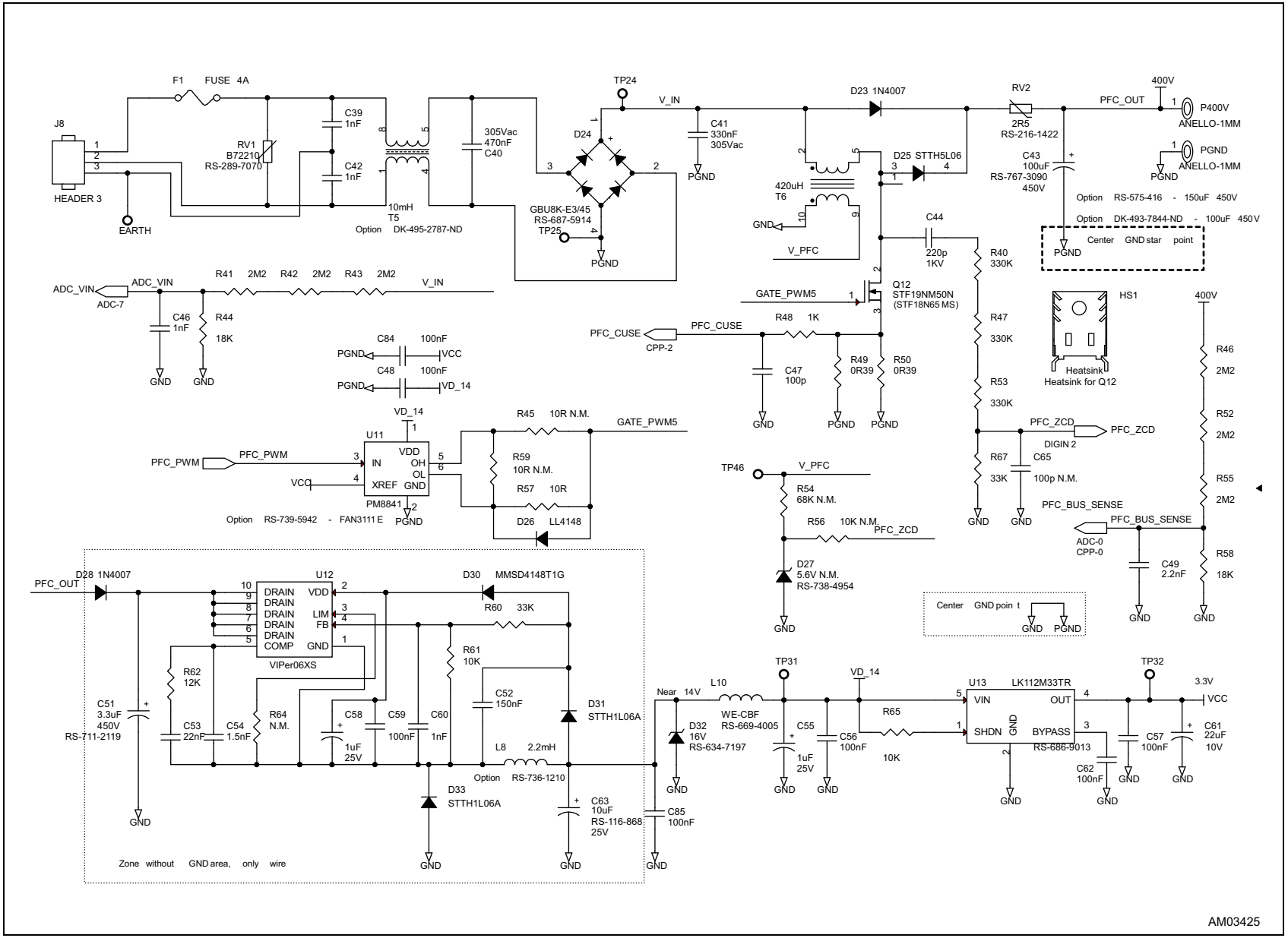


Figure 14. PSR-ZVS demonstration board schematic - PSR-ZVS stage

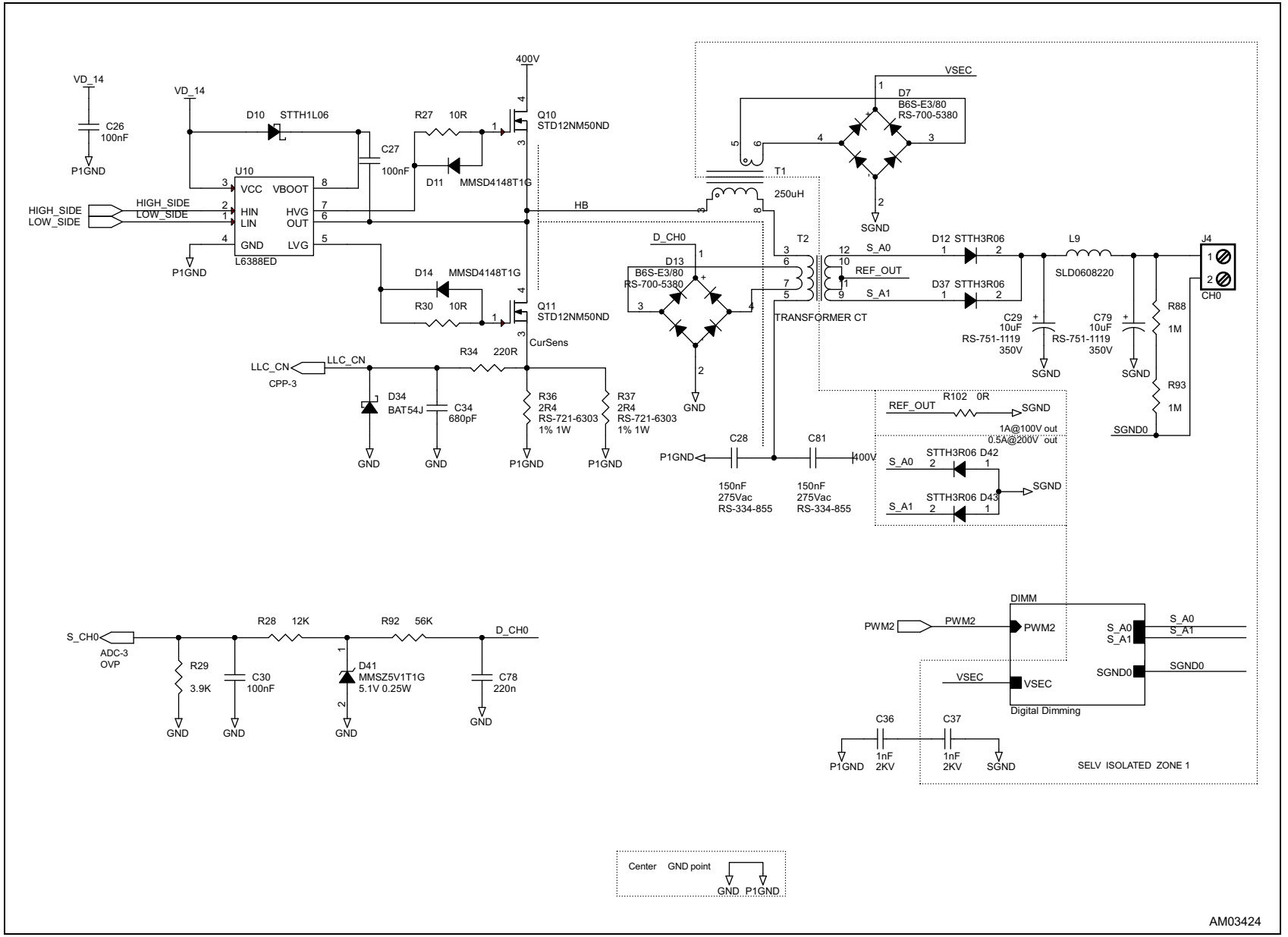


Figure 15. PSR-ZVS demonstration board schematic - digital dimming stage

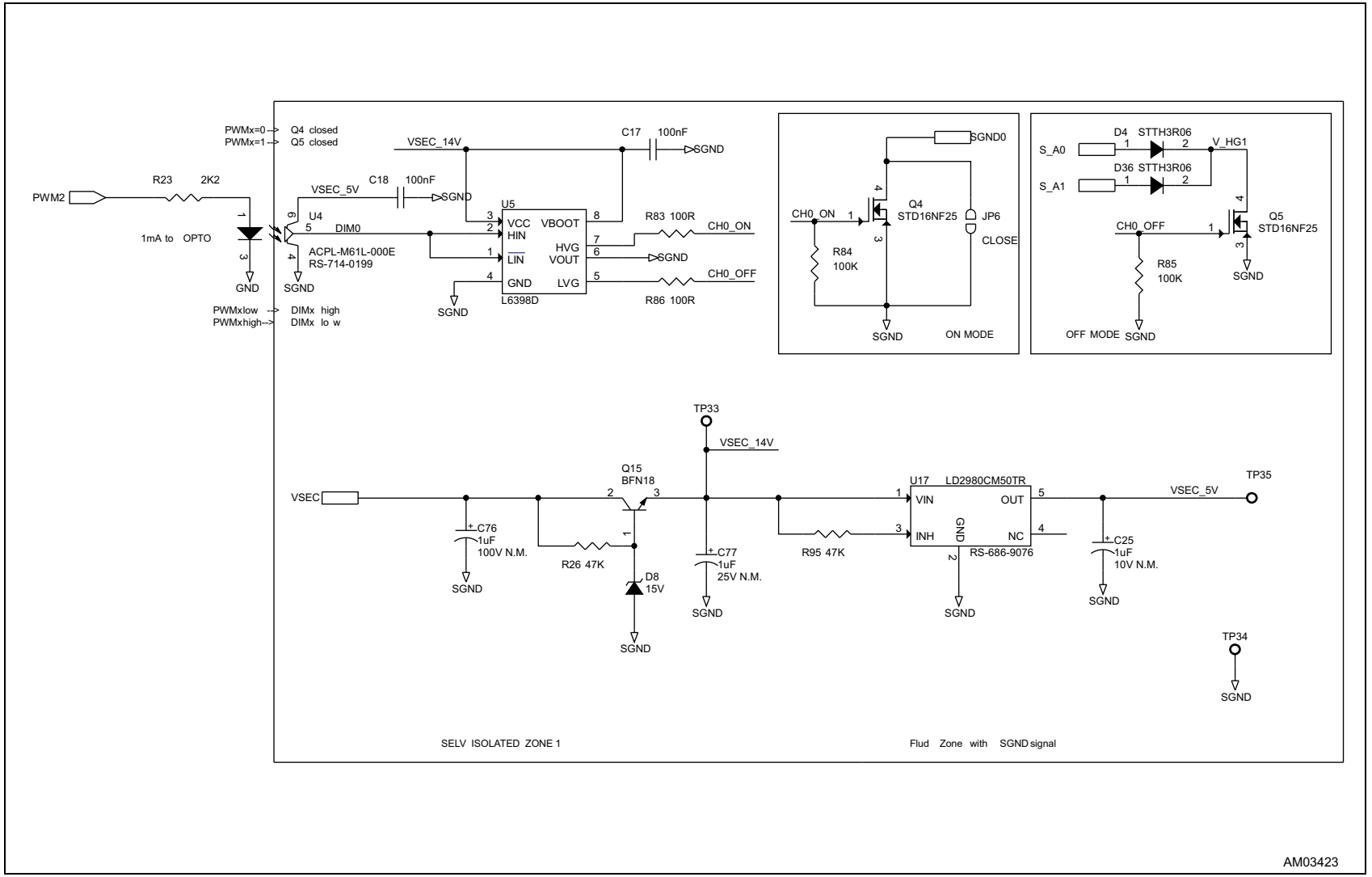


Figure 16. PSR-ZVS demonstration board schematic - THD optimizer

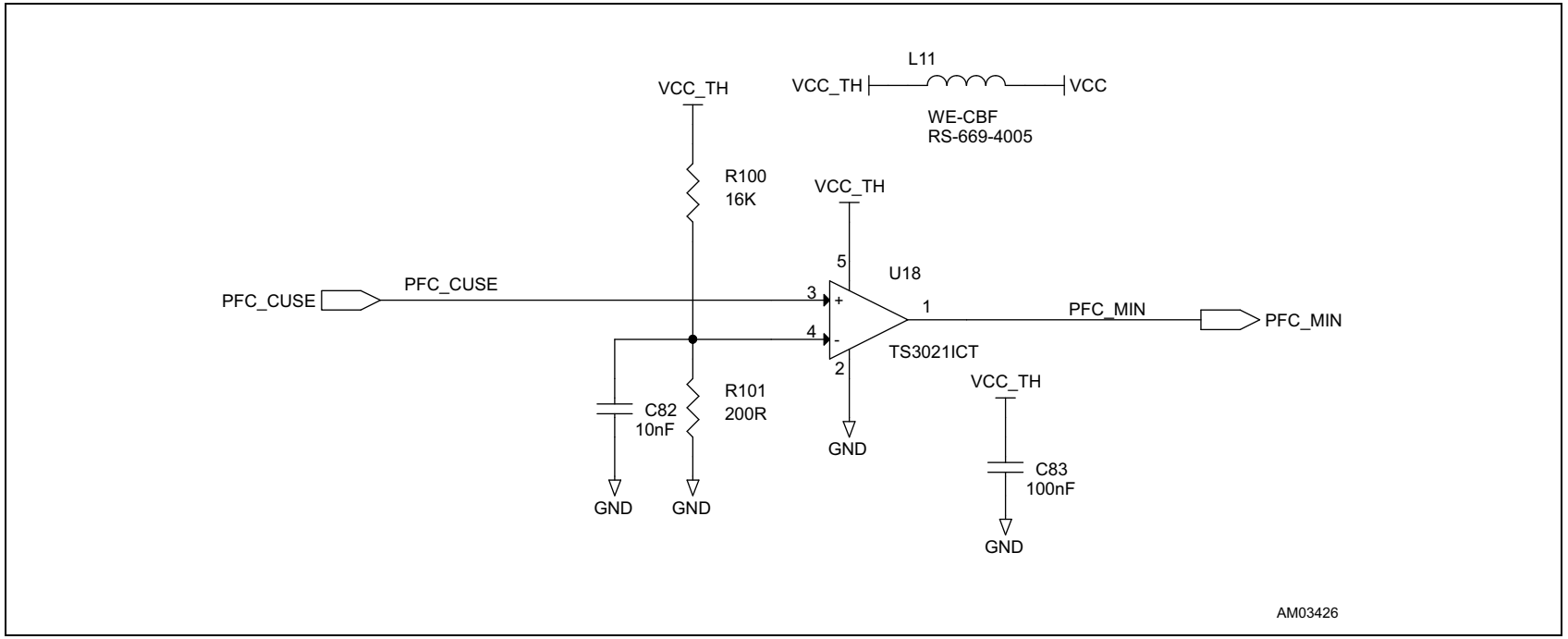


Figure 17. PSR-ZVS demonstration board schematic - DALI and 0 - 10 interfaces

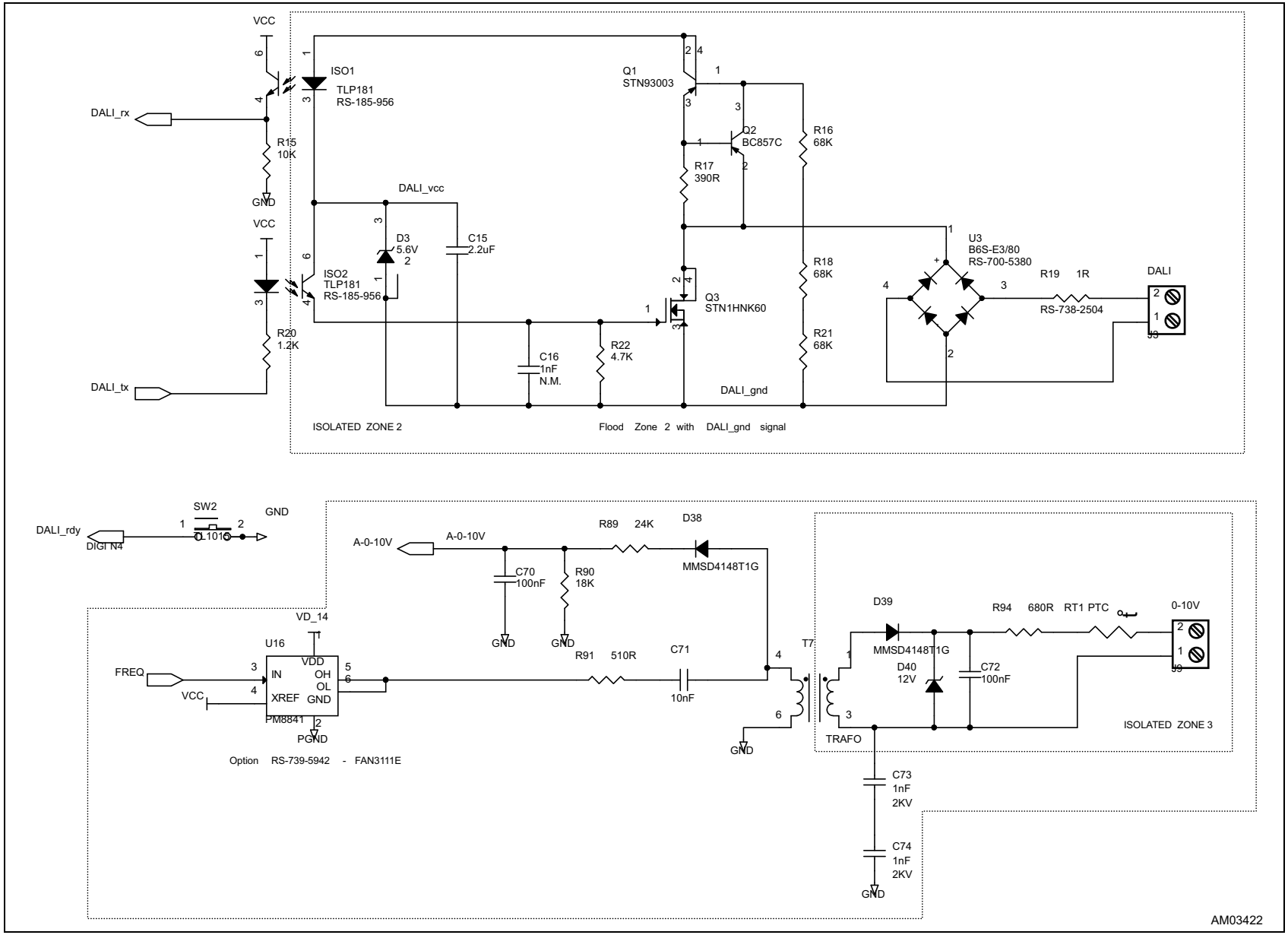
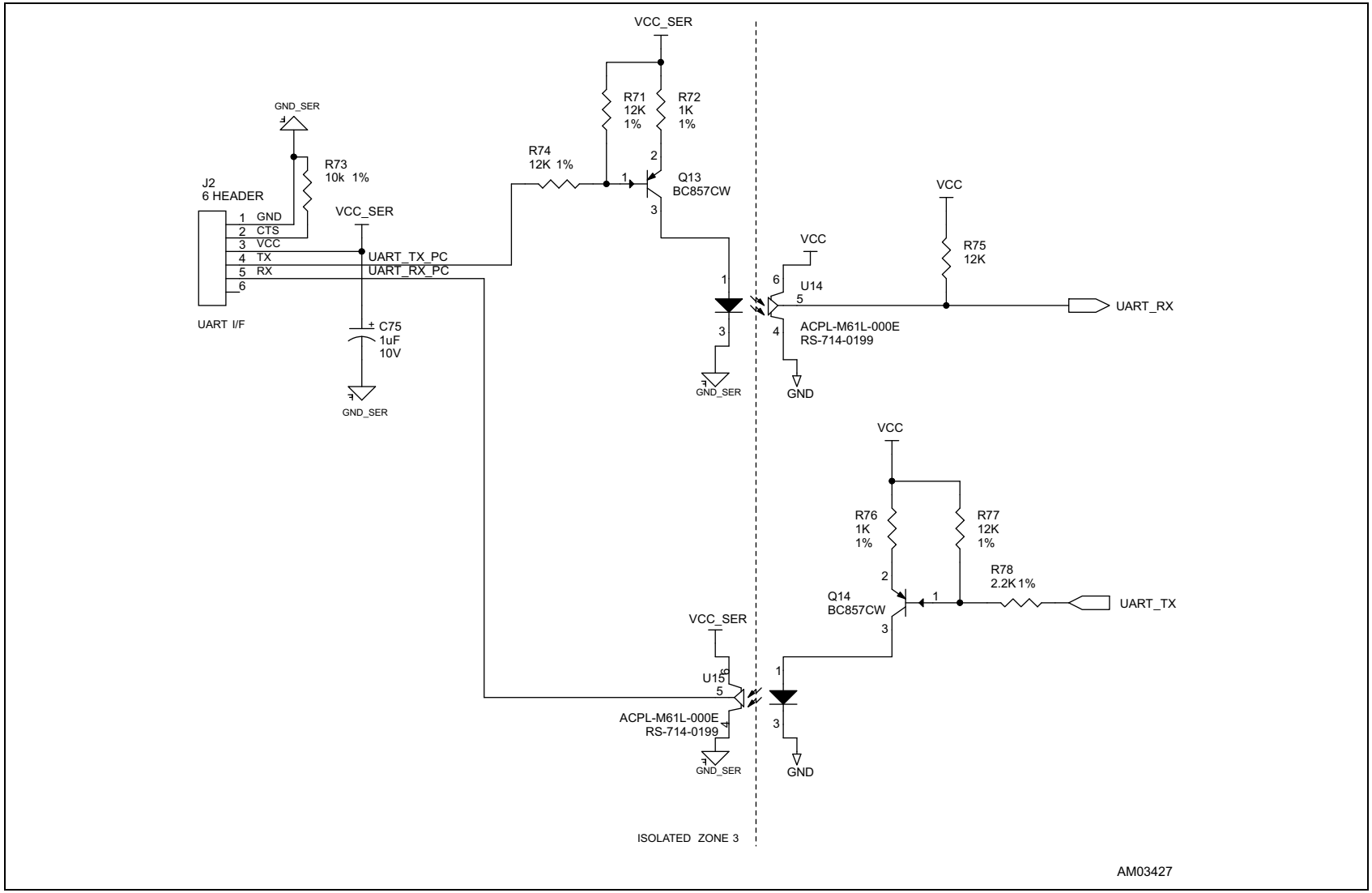


Figure 18. PSR-ZVS demonstration board schematic - serial interfaces



7 Bill of material

Table 5. Bill of material

Item	Qty.	Reference	Part	PCB footprint	Note	Manuf.	Part number
1	3	C1, C6, C75	1 µF	CAPC-0603	10 V	AVX	0603ZG105ZAT2A
2	5	C2, C4, C7, C67, C82	10 nF	CAPC-0603		AVX	06033C103KAT2A
3	2	C3, C5	100 nF	CAPC-0603		AVX	06033G104ZAT2A
4	1	C8	2.2 µF	CAPC-0603	X5R	Murata	GRM188R60J225KE19D
5	1	C15	2.2 µF	CAPC-0805		Murata	GCM21BR71C225KA64L
6	1	C16	1 nF	CAPC-0603	N. M.		
7	1	C17	100 nF	CAPC-0603	N. M.		
8	1	C18	100 nF	CAPC-0805	N. M.		
9	1	C25	1 µF	CAPC-0603	10 V N. M.		
10	9	C26, C30, C48, C56, C57, C62, C83, C84, C85	100 nF	CAPC-0603	25 V	AVX	06033G104ZAT2A
11	1	C27	100 nF	CAPC-0805		TAIYO YUDEN	HMK212BJ104KG-T
12	2	C28, C81	150 nF	CER-P15L6	275 Vac	EPCOS	B32922C3154K
13	2	C29, C79	10 µF	CAPE-R13H20-P5	350 V	Rubycon	EEUEE2W100
14	1	C34	680 pF	CAPC-0603	25 V	KEMET	C0603C681J5GAC7867
15	2	C36, C37	1 nF	C1210	2 KV	AVX	1210GC102KAT1A
16	2	C39, C42	1 nF	CAPC-1206	1 kV	KEMET	C1206C102KDRAC
17	1	C40	470 nF	CAPP-175X100X165-P15	305 Vac	Vishay	BFC233920474
18	1	C41	330 nF	CAPP-175X85X150-P15	305 Vac	Vishay	2222 339 20334
19	1	C43	100 µF	CAPE-R30H35-P10-SI	450 V	Rubycon	450VXH100MEFCSN22X25
20	1	C44	220 pF	CAPC-1206	1 KV		

Table 5. Bill of material (continued)

Item	Qty.	Reference	Part	PCB footprint	Note	Manuf.	Part number
21	1	C46	1 nF	CAPC-0603	50 V	AVX	06035C102KAT2A
22	1	C47	100 pF	CAPC-0603			
23	1	C49	2.2 nF	CAPC-0603		Vishay	VJ0603Y222KNAAO
24	1	C51	3.3 µF	CAPE-R10HXX-P5	450 V	RS	711-2119
25	1	C52	150 nF	CAPC-0603	50 V	Murata	GRM188R71E154KA01D
26	1	C53	22 nF	CAPC-0603		AVX	06035C223KAT2A
27	1	C54	1.5 nF	CAPC-0603		KEMET	C0603C152K1RAC7867
28	2	C55, C58	1 µF	CAPC-0805	25 V	Murata	GCM21BR71E105KA56L
29	1	C59	100 nF	CAPC-0603	50 V	AVX	06033G104ZAT2A
30	1	C60	1 nF	CAPC-0603	50 V	AVX	06035C102KAT2A
31	1	C61	22 µF	CAPC-1206	10 V	KEMET	C1206C226M8PAC7800
32	1	C63	10 µF	CAPE-R5H11-P25	25 V	Panasonic	ECEA1EKS100
33	1	C65	100 pF N. M.	CAPC-0603	N. M.		
34	1	C66	6.8 nF	CAPC-0603		KEMET	C0603C682K5RAC7867
35	2	C70, C72	100 nF	CAPC-0603	25 V		
36	1	C71	1 nF	CAPC-0805			
37	2	C73, C74	1 nF	C1210	2 KV	AVX	1210GC102KAT1A
38	1	C76	1 µF	CAPE-R5H11-P25	100 V N. M.		
39	1	C77	1 µF	CAPC-0805	25 V N. M.		
40	1	C78	220 nF	CAPC-0603	25 V		C0603C681J5GAC7867
41	1	C80	680 pF	CAPC-0603			
42	1	D1	FAULT	LEDC-0603		OSRAM	LS Q976
43	1	D2	RUN	LEDC-0603		OSRAM	LT Q39G-Q1S2-25-1
44	1	D3	5.6 V	SOT23		Diodes Zetex	BZX84C5V6-7-F
45	2	D4, D36	STTH3R06	DIODO-SMC	N. M.		

Table 5. Bill of material (continued)

Item	Qty.	Reference	Part	PCB footprint	Note	Manuf.	Part number
46	1	D7	B6S-E3/80	PONTE-SMD-MBXS	N. M.	Vishay	B6S-E3/80
47	2	U3, D13	B6S-E3/80	PONTE-SMD-MBXS		Vishay	B6S-E3/80
48	1	D8	Zener - 15 V	POWERDI323	N. M.		
49	1	D10	STTH1L06	DIODO-SMB		ST	STTH1L06U
50	3	D11, D14, D30	MMSD4148T1G	SOD123		ON Semiconductor®	MMSD4148T1G
51	2	D12, D37	STTH3R06	DIODO-SMC		ST	STTH3R06S
52	1	D23	1N4007	DIODO-SMA		ST	1N4007
53	1	D24	GBU8K-E3/45	KBU8XXG		TAIWAN SEMICONDUCTOR	KBU807G
54	1	D25	STTH5L06	DPAK		ST	STTH5L06B-TR
55	1	D26	LL4148	SOD80	N. M.		
56	1	D27	Zener-5.6 V N. M.	SOD123	N. M.		
57	1	D28	1N4007	DIODO-SMA		ST	1N4007
58	2	D31, D33	STTH1L06A	DIODO-SMA		ST	STTH1L06A
59	1	D32	Zener 16 V	DIODO-SMA		Vishay	SML4745-E3
60	1	D34	BAT54J	SOD323		ST	BAT54J
61	2	D38, D39	MMSD4148T1G	SOD123			
62	1	D40	Zener - 12 V	SOD123		Diodes Zetex	DDZ9699-7
63	1	D41	MMSZ5V1T1G	SOD123	5.1 V 0.25 W	ON Semiconductor	MMSZ5V1T1G
64	2	D42, D43	STTH3R06	DIODO-SMC	1 A/0.5 A sel.	ST	STTH3R06S
65	1	F1	FUSE	FUSEPTH-R85H80-P5	4 A	Wickmann	3701400000
66	2	ISO1,ISO2	TLP181	OPTO-SOP127P-700X210-6-NO25	Toshiba	TLP181 (GB, F)	
67	1	JP5	JUMPER GOCCIA	JP3SO	CLOSE 2 - 3		

Table 5. Bill of material (continued)

Item	Qty.	Reference	Part	PCB footprint	Note	Manuf.	Part number
68	1	JP6	JUMPER GOCCIA	JP2SO	CLOSE		
69	1	J1	SWIM I/F	STRIP254P-M-4			
70	1	J2	6 HEADER	STRIP254P-M-6			
71	1	J3	DALI	MOR-2POLI-WAGO-250-402	WAGO	250-402	
72	1	J4	CH0	MOR-2POLI-WAGO-250-402	WAGO	250-402	
73	1	J8	HEADER 3	MOR-3POLI-508		TE Connectivity	282837-3
74	1	J9	0 - 10 V	MOR-2POLI-WAGO-250-402			
75	3	L1, L10, L11	WE-CBF	CAPC-0603		WÜRTH ELEKTRONIK	74279262
76	5	L2, L3, L4, L5, L6	WE-CBF	CAPC-0603		WÜRTH ELEKTRONIK	74279269
77	1	L8	2.2 mH	IND-R090H120-P5	410 mA	Itacoil®	SLD0608222
78	1	L9	SLD0608220	IND-R75H92-P3		Itacoil	SLD0608220
79	1	Q1	STN93003	SOT223		ST	STN93003
80	1	Q2	BC857C	SOT23		ST	BC857C
81	1	Q3	STN1HNK60	SOT223		ST	STN1HNK60
82	2	Q4,Q5	STD16NF25	DPAK	N. M.		
83	2	Q10, Q11	STD12NM50ND	DPAK		ST	STD12NM50ND
84	1	Q12	STF19NM50N	TO220-3PIN-split1		ST	STF19NM50N
85	2	Q13, Q14	BC857CW	SOT323		ST	BC857CW
86	1	Q15	BFN18	SOT89	N. M.		
87	1	RT1	PTC	RESC1206		Bourns®	MF-USMF005-2
88	1	RV1	B72210	SIOV-S10K300		EPCOS	B72210S0301K101
89	1	RV2	2R5	NTC-EPCOS-S237		EPCOS	B57237S259M

Table 5. Bill of material (continued)

Item	Qty.	Reference	Part	PCB footprint	Note	Manuf.	Part number
90	5	R1, R2, R48, R72, R76	1 KΩ	RESC-0603		Vishay®	CRCW06031K00FKEA
91	1	R3	9.1 KΩ	RESC-0603	1%	Panasonic	ERJP03F9101V
92	1	R4	5.6 KΩ	RESC-0603	1%	Panasonic	ERJP03F5601V
93	1	R22	4.7 KΩ	RESC-0603		Bourns	CR0603-JW-472ELF
93	1	R15	10 KΩ	RESC-0603			
94	3	R16, R18, R21	68 KΩ	RESC-0603		Panasonic	ERJ3GEYJ683V
95	1	R17	390 Ω	RESC-0603		Panasonic	ERJ3GEYJ391V
96	1	R19	1 Ω	RES-900X320-P15-1W2		RS	738-2504
97	1	R20	1.2 KΩ	RESC-0603		RS	RS-0603-1k2-5%-0.1W
98	1	R23	2.2 KΩ	RESC-0603	N. M.		
99	2	R26, R95	47 KΩ	RESC-0805	N. M.		
100	3	R27, R30, R57	10 Ω	RESC-0805		Bourns	CR0805-FX-10R0GLF
101	3	R28, R97, R99	12 KΩ	RESC-0603	1%	RS	RS-0603-12k-1%-0.1W
102	1	R29	3.9 KΩ	RESC-0603			
103	1	R34	220 Ω	RESC-0603		RS	RS-0603-220R-5%-0.1W
104	2	R36, R37	2R4	RESC-2512	1% 1 W	Panasonic	ERJ1TRQF2R4U
105	3	R40, R47, R53	330 KΩ	RESC-1206		TE Connectivity	CRG1206F330K
106	6	R41, R42, R43, R46, R52, R55	2.2 MΩ	RESC-1206	1%		
107	2	R44, R58	18 KΩ	RESC-1206	0.1%		
108	2	R45, R59	10 Ω N. M.	RESC-0805	N. M.		
109	2	R49, R50	0.39 Ω	RESC-2512	1% 1 W	Panasonic	ERJ1TRQFR39U
110	1	R54	68 KΩ N. M.	RESC-0603	N. M.		
111	1	R56	10 KΩ N. M.	RESC-0603	N. M.		

Table 5. Bill of material (continued)

Item	Qty.	Reference	Part	PCB footprint	Note	Manuf.	Part number
112	1	R60	33 KΩ	RESC-0603	1%	RS	RS-0603-33k-1%-0.1W
113	1	R61	10 KΩ	RESC-0603	1%	Bourns	CR0603-FX-1002HLF
114	1	R62	12 KΩ	RESC-0603	1%	RS	RS-0603-12k-1%-0.1W
115	1	R64	N. M.	RESC-0603	1%		
116	1	R65	10 KΩ	RESC-0805		RS	RS-0805-10k-5%-0.125W
117	1	R67	33 KΩ	RESC-1206		TE Connectivity	CRG1206F33K
118	4	R71, R74, R75, R77	12 KΩ	RESC-0603		YAGEO	232270265123
119	1	R73	10 kΩ	RESC-0603		Bourns	CR0603-JW-103ELF
120	1	R78	2.2 KΩ	RESC-0603		Bourns	CR0603-FX-2201ELF
121	2	R79, R98	22 KΩ	RESC-0603		Bourns	CR0603-FX-2202ELF
121a	1	R82	10 nF	CAPC-0603		AVX	06033C103KAT2A
122	2	R83, R86	100 Ω	RESC-0805	N. M.		
123	2	R84, R85	100 KΩ	RESC-0603	N. M.		
124	2	R88, R93	1 MΩ	RESC-1206	1%	TE Connectivity	CRG1206F1M0
125	1	R89	24 KΩ	RESC-0603	1%		
126	1	R90	18 KΩ	RESC-0603	1%		
127	1	R91	510 Ω	RESC-0603	1%		
128	1	R92	56 KΩ	RESC-0603			
129	1	R94	680 RΩ	RESC-0805			
130	1	R96	150 KΩ	RESC-0603			
131	1	R100	16 KΩ	RESC-0603		Vishay	CRCW060316K0FKEA
132	1	R101	200 Ω	RESC-0603		Vishay	CRCW0603200RFKEA
133	1	R102	0 Ω	RESC-1206		Bourns	CR1206-J/-000ELF
134	2	SW1, SW2	TL1015	BUTTON-ESWITCH-TL1015		E-SWITCH	TL1015BF160QG

Table 5. Bill of material (continued)

Item	Qty.	Reference	Part	PCB footprint	Note	Manuf.	Part number
135	7	TP22, TP23, TP24, TP25, TP31, TP32	TP	TPTH-ANELLO-1MM			
136	2	P400V, PGND	TP	TPTH-ANELLO-1MM			
137	1	T1	250 µH	TRAFO-ROCCHETTO-EF20D		Itacoil	TLLE20D01
138	1	T2	TRANSFOR CT	TRAFO-STM-ETD341711		Itacoil	TSLETD3402
139	1	T5	10 mH	IND-ITACOIL-SCLE25		Itacoil	SCLE25103
140	1	T6	420 µH	INDPFC-ITACOIL-SMC037-100113		Itacoil	TCLPQ262501
141	1	T7	TRAFO	TRAFO-ITACOIL-SMLEP1303		Itacoil	SMLEP1303
142	1	U1	STLUX385A	TSSOP050P-640X120-38		STMicroelectronics®	STLUX385A
143	1	U4	ACPL-M61L-000E	OPTO-SOP127P-700X210-6-NO2	N. M.		
144	1	U5	L6398D	SOP127P-600X168-8	N. M.		
145	1	U10	L6388ED	SOP127P-600X168-8		ST	L6388ED
146	1	U11	PM8841	SOT23-6		ST	PM8841
147	1	U12	VIPer06XS	ssop100p-620x175-10		ST	VIPer06XS
148	1	U13	LK112M33TR	SOT23-5		ST	LK112M33TR
149	2	U14, U15	ACPL-M61L-000E	OPTO-SOP127P-700X210-6-NO2		AVAGO TECHNOLOGIES	ACPL-M61L-000E
150	1	U16	PM8841	SOT23-6		ST	PM8841
151	1	U17	LD2980CM50TR	SOT23-5	N. M.		
152	1	U18	TS3021ICT	SC70-5		ST	TS3021ICT

8 Board connector pinout

Table 6. Connector J8 pinout - AC-DC input

Name	Type	Function
ACIN	Power	Main AC/DC input
ACIN	Power	Main AC/DC input
EARTH	Power	Protection reference level

Table 7. Connector J4 pinout - DC output

Name	Type	Function
+	Power	Positive load connection.
-	Power	Negative load connection.

Table 8. Connector J3 pinout - DALI interfaces

Name	Type	Function
DA	DALI signal	DALI signal for isolated DALI interfaces - without polarization
DA	DALI signal	DALI signal for isolated DALI interfaces - without polarization

Table 9. Connector J9 pinout - 0 - 10 V

Name	Type	Function
+	“Positive reference	Positive reference for isolated 0 - 10 V interfaces
-	“Negative reference	Negative reference for isolated 0 - 10 V interfaces

Table 10. Connector J2 pinout - serial interfaces

Name	Type	Function
1 (black)	Negative power	Directly connected to isolated serial GND
2 (brown)	CTSn	Not used - pulled down
3 (red)	Fixed positive power	5.0 V power for the UART interfaces only
4 (orange)	TXD (input)	TXD signal - RXD on STLUX
5 (yellow)	RXD (output)	RXD signal - TXD from STLUX
6 (green)	RTSn	Not connected

Table 11. Connector J1 pinout - SWIM interfaces

Name	Type	Function
1	VCC_SWIM	Power reference from board
2	SWIM	SWIM signal to/from STLUX
3	GND_SWIM	Directly connected to primary GND
4	RESn	Connected to STLUX NRST pin

9 User interface

The user can interact with the board via multiple interfaces: the DALI, serial and 0 - 10 V interface. While the 0 - 10 V interface allows to remotely control the LED current, both DALI and serial interfaces allow the configuration of several operating and start-up parameters. The DALI and 0 - 10 V interface are mutually exclusive and the user can select which one to enable. For safety reasons, the DALI, serial and 0 - 10 V interfaces are isolated.

The serial line is convenient to connect the demonstration board to additional interfaces, such as Bluetooth®, power line modems, Wi-Fi, etc.

The user can quickly monitor the status of the board by looking at the two status LEDs (red, green) installed on the board.

9.1 Status LEDs

There are two status LEDs on the board, one green and one red.

- Green LED (status): active when the input power is correct and the STLUX385A device is running.
  - LED on: STLUX385A running.
  - LED off: STLUX385A is in IDLE mode.
  - LED toggling (1 sec. on, 1 sec. off): debug mode active. The board is not operating.
- Red LED (failure): used to report an error or the intervention of a protection to preserve the hardware. Once the error has been detected (e.g. via terminal command “st”), fixed and the “co” command line is used, the red LED goes off.

9.2 List of supported DALI commands

The internal DALI stack has implemented all the standard commands defined into DALI standard. Also the LED extension is implemented directly on the STLUX firmware.

Table 12. List of supported DALI commands

Command number	Command code	Mnemonic command name
-	YAAA AAA0 XXXX XXXX	DIRECT ARC POWER CONTROL
0	YAAA AAA1 0000 0000	OFF
1	YAAA AAA1 0000 0001	UP
2	YAAA AAA1 0000 0010	DOWM
3	YAAA AAA1 0000 0011	STEP UP
4	YAAA AAA1 0000 0100	STEP DOWN
5	YAAA AAA1 0000 0101	RECALL MAX LEVEL
6	YAAA AAA1 0000 0110	RECALL MIN LEVEL
7	YAAA AAA1 0000 0111	STEP DOWN AND OFF
8	YAAA AAA1 0000 1000	ON AND STEP UP

Table 12. List of supported DALI commands (continued)

Command number	Command code	Mnemonic command name
9	YAAA AAA1 0000 1001	ENABLE DAPC SEQUENCE
16 - 31	YAAA AAA1 0001 XXXX	GO TO SCENE
32	YAAA AAA1 0010 0000	RESET
33	YAAA AAA1 0010 0001	STORE ACTUAL LEVEL IN THE DTR
42	YAAA AAA1 0010 1010	STORE THE DTR AS MAX LEVEL
43	YAAA AAA1 0010 1011	STORE THE DTR AS MIN LEVEL
44	YAAA AAA1 0010 1100	STORE THE DTR AS SYSTEMFAILURE LEVEL
45	YAAA AAA1 0010 1101	STORE THE DTR AS POWER ONLEVEL
46	YAAA AAA1 0010 1110	STORE THE DTR AS FADE TIME
47	YAAA AAA1 0010 1111	STORE THE DTR AS FADE RATE
64 - 79	YAAA AAA1 0100 XXXX	STORE THE DTR AS SCENE
80 - 95	YAAA AAA1 0101 XXXX	REMOVE FROM SCENE
96 - 111	YAAA AAA1 0110 XXXX	ADD TO GROUP
112 - 127	YAAA AAA1 0111 XXXX	REMOVE FROM GROUP
128	YAAA AAA1 1000 0000	STORE DTR AS SHORT ADDRESS
129	YAAA AAA1 1000 0001	ENABLE WRITE MEMORY
144	YAAA AAA1 1001 0000	QUERY STATUS
145	YAAA AAA1 1001 0001	QUERY CONTROL GEAR
146	YAAA AAA1 1001 0010	QUERY LAMP FAILURE
147	YAAA AAA1 1001 0011	QUERY LAMP POWER ON
148	YAAA AAA1 1001 0100	QUERY LIMIT ERROR
149	YAAA AAA1 1001 0101	QUERY RESET STATE
150	YAAA AAA1 1001 0110	QUERY MISSING SHORT ADDRESS
151	YAAA AAA1 1001 0111	QUERY VERSION NUMBER
152	YAAA AAA1 1001 1000	QUERY CONTENT DTR
153	YAAA AAA1 1001 1001	QUERY DEVICE TYPE
154	YAAA AAA1 1001 1010	QUERY PHYSICAL MINIMUM LEVEL
155	YAAA AAA1 1001 1011	QUERY POWER FAILURE
156	YAAA AAA1 1001 1100	QUERY CONTENT DTR1
157	YAAA AAA1 1001 1101	QUERY CONTENT DTR2
160	YAAA AAA1 1010 0000	QUERY ACTUAL LEVEL
161	YAAA AAA1 1010 0001	QUERY MAX LEVEL
162	YAAA AAA1 1010 0010	QUERY MIN LEVEL
163	YAAA AAA1 1010 0011	QUERY POWER ON LEVEL
164	YAAA AAA1 1010 0100	QUERY SYSTEM FAILURE LEVEL

Table 12. List of supported DALI commands (continued)

Command number	Command code	Mnemonic command name
165	YAAA AAA1 1010 0101	QUERY FADE TIME/FADE RATE
176 - 191	YAAA AAA1 1011 XXXX	QUERY SCENE LEVEL (SCENES 0 - 15)
192	YAAA AAA1 1100 0000	QUERY GROUPS 0 - 7
193	YAAA AAA1 1100 0001	QUERY GROUPS 8 - 15
194	YAAA AAA1 1100 0010	QUERY RANDOM ADDRESS (H)
195	YAAA AAA1 1100 0011	QUERY RANDOM ADDRESS (M)
196	YAAA AAA1 1100 0100	QUERY RANDOM ADDRESS (L)
197	YAAA AAA1 1100 0101	READ MEMORY LOCATION
224 - 254	YAAA AAA1 111X XXXX	Refer to standard IEC62386 - part 207
255	YAAA AAA1 1111 1111	QUERY EXTENDED VERSION NUMBER
256	1010 0001 0000 0000	TERMINATE
257	1010 0011 XXXX XXXX	DATA TRANSFER REGISTER (DTR)
258	1010 0101 XXXX XXXX	INITIALISE
259	1010 0111 0000 0000	RANDOMISE
260	1010 1001 0000 0000	COMPARE
261	1010 1011 0000 0000	WITHDRAW
264	1011 0001 HHHH HHHH	SEARCHADDRH
265	1011 0011 MMMM MMMM	SEARCHADDRM
266	1011 0101 LLLL LLLL	SEARCHADDRL
267	1011 0111 0AAA AAA1	PROGRAM SHORT ADDRESS
268	1011 1001 0AAA AAA1	VERIFY SHORT ADDRESS
269	1011 1011 0000 0000	QUERY SHORT ADDRESS
270	1011 1101 0000 0000	PHYSICAL SELECTION
272	1100 0001 XXXX XXXX	ENABLE DEVICE TYPE X
273	1100 0011 XXXX XXXX	DATA TRANSFER REGISTER 1 (DTR1)
274	1100 0101 XXXX XXXX	DATA TRANSFER REGISTER 2 (DTR2)
275	1100 0111 XXXX XXXX	WRITE MEMORY LOCATION

Table 13. IEC62386 part 207 - command extension

Command number	Command code	Mnemonic command name
224	YAAA AAA1 1110 0000	REFERENCE SYSTEM POWER
225	YAAA AAA1 1110 0001	ENABLE CURRENT PROTECTOR - not implemented
226	YAAA AAA1 1110 0010	DISABLE CURRENT PROTECTOR - not implemented
227	YAAA AAA1 1110 0011	SELECT DIMMING CURVE
228	YAAA AAA1 1110 0100	STORE DTR AS FAST FADE TIME
237	YAAA AAA1 1110 1101	QUERY GEAR TYPE
238	YAAA AAA1 1110 1110	QUERY DIMMING CURVE
239	YAAA AAA1 1110 1111	QUERY POSSIBLE OPERATING MODES
240	YAAA AAA1 1111 0000	QUERY FEATURES
241	YAAA AAA1 1111 0001	QUERY FAILURE STATUS
242	YAAA AAA1 1111 0010	QUERY SHORT-CIRCUIT
243	YAAA AAA1 1111 0011	QUERY OPEN CIRCUIT
244	YAAA AAA1 1111 0100	QUERY LOAD DECREASE
245	YAAA AAA1 1111 0101	QUERY LOAD INCREASE
246	YAAA AAA1 1111 0110	QUERY CURRENT PROTECTOR ACTIVE
247	YAAA AAA1 1111 0111	QUERY THERMAL SHUT DOWN - not implemented
248	YAAA AAA1 1111 1000	QUERY THERMAL OVERLOAD - not implemented
249	YAAA AAA1 1111 1001	QUERY REFERENCE RUNNING - not implemented
250	YAAA AAA1 1111 1010	QUERY REFERENCE MEASUREMENT FAILED
251	YAAA AAA1 1111 1011	QUERY CURRENT PROTECTOR ENABLED
252	YAAA AAA1 1111 1100	QUERY OPERATING MODE
253	YAAA AAA1 1111 1101	QUERY FAST FADE TIME
254	YAAA AAA1 1111 1110	QUERY MIN FAST FADE TIME
255	YAAA AAA1 1111 1111	QUERY EXTENDED VERSION NUMBER
272	1100 0001 0000 0110	ENABLE DEVICE TYPE 6

Please refer to the DALI extension manual on www.dali-ag.org (IEC 62386-207) for more details on the standard.

9.3 Serial command

This section describes the terminal interface line available on the STLUX385A device. The serial line allows the configuration of the operating condition, including the current level (dimming). It also allows to enquire the board status and the value of application parameters.

This section shows a list of commands available via the serial interface according to the STEVAL385LEDPSR demonstration board firmware version V3R28.

The STLUX385A command line interface is accessible via a standard terminal utility installed on the user's PC.

The serial (TTL 0 - 3.3 V) cable is provided together with the demonstration board. The on-board connector is identified as UART I/F. The serial line uses only three lines: GND, TX, RX plus power and ground derived from USB interfaces. The predefined baud rate is 115200, no parity, 8-bit, 1 stop bit, no handshake. The user should identify the PC COM line number. The PC will also install the serial COM drivers as soon as the cable is connected. If the driver is not installed or for other problems please call your IT support.

During the power-up and reset the STLUX385A transmits the following strings to the serial line.

Figure 19. Power-up message

```
EVAL STLUX385-PSR-ZVS V3R28
Build Oct 16 2013 13:44:22 core is 385A ok
Option PFC HB Dali R enabled
Ready
```

The message is used to verify that the link between the PC and the STLUX385A device is up and that the correct baud rate is selected. Also the following information is displayed:

- The string “V3R28” reports the firmware version (3) and revision (28).
- Firmware time and the date.
- Options currently enabled. In this example the PFC, the resonant stage (HB) and the DALI interface are enabled.
- “Ready” appears when the STLUX385A is ready to receive a command.

The user can interact with the STLUX385A device using one of the following commands displayed in *Figure 20*:

Figure 20. Command list

```
Monitor channel command

ll [dat]                Set output current (2-4094)
st                      Get status
gp                      Get PFC status
gh                      Get HB  status
ad                      Get all ADC channels
ti                      Get time
co                      Clear error
in [of][val]            Set startup param, "in 0 0" to help
hf [val]                Set HB DEAD time (24<-192)
hb [val]                Set HB ON time (0 = off, 1 = on, 46<->650)
pf [val]                Set PFC 0 = off, 1 = on, 2 = minpw or (875<->920)
dt [val]                Set HB remove delay time
fr [div]                Set CCO freq
hl [??]                 help cmd [??] string
hl                      get help
?                       get help

use [enter] to end line, use [backspace] to delete char
```

The command list can be displayed using the “?” command.

Commands may require several parameters and the user shall use the correct syntax. Any incorrectly typed character can be modified using the backspace character.

Figure 20: Command list describes the commands accessible through the console. For convenience, the resonant stage is referred to as HB (“Half Bridge”).

With the exception of the parameters “in” command, all commands are volatile and their results are defaulted once the board is reset. The “in” command lets the user modify the startup value for selected parameters. Any new startup value is stored in an EEPROM memory.

Caution: The commands guarantee full access to the board configuration. Please take care when modifying the behavior of the board via commands. An incorrect configuration change may damage the board.

9.3.1 ll - configure LED output current

Change the LED output current. This command should be used only when the DALI or 0 - 10 V interfaces are not active. The DALI and 0 - 10 V have higher priority over the “ll” command. The “ll” values are in range from 2 (minimum current) to 4094 (maximum current). While operating on the STEVAL385LEDPSR demonstration board, the “ll” parameters should be configured between 539 (minimum current) and 3450 (maximum current).

The LED can be switched off using parameter 0. Once the LEDs are switched off with the command “ll”, then the LED can only be switched on again via the command “ll” (and not 0 - 10 V or DALI).

The STEVAL385LEDPSR demonstration board also limits the resonant output current variation rate to a maximum of 333 mA /second, in order to preserve both the output capacitors and the LED string.

Caution: Take care when using this command. The board injects the configured LED current independently from the LED ratings. The user shall configure a current level not greater than the maximum current allowed by the LED strings connected.

The correlation from output current and “ll” value is not linear. *Table 14* defines the value for a selected number of output current values correlated with “ll” value:

Table 14. “*ll*” <-> *output current relation*

“ll” value	Output current (1 A scale)	Output current (500 mA scale)
0	Off	Off
539	10 mA	5 mA
660	100 mA	50 mA
795	200 mA	100 mA
935	300 mA	150 mA
1070	400 mA	200 mA
1380	500 mA	250 mA
1770	600 mA	300 mA
2175	700 mA	350 mA
2600	800 mA	400 mA
3020	900 mA	450 mA
3450	1000 mA	500 mA

Syntax: ll val

Parameters:

- val [0,2-4096]: configure the output current level.
  - 0: switch off the LED
  - 2-4096: set the output current. The STEVAL385LEDPSR supports currents in the range 539-3450.

Output:

Default: none

Example: ll 539: set the minimum LED current level.

9.3.2 st - status

The command reports the actual demonstration board status. This command reports all the main internal variables, flags and the status of the board. The values are reported as sampled when the “st” command is executed.

Syntax: st

Parameters:

none

Output:

```
PSR-ZVS status is 0:2
Vin Vi = 677 Vp = 695 Vmin = 30 Vmax = 695 freq = 99
PFC st = 0x1 Vo = 903 S0 = 51 S3 = 124 maxon = 480 I = 8
HB st = 0x3 Z = 0 S0 = 33 S3 = 445 dt = 30 O0 L = 569 H = 569
PW2 ta = 3450 re = 3446 now = 3450 O1:0 dump = 37 ndump = 0 tz = 0x25
```

Table 15. Status information

Line	Parameter	Description			Unit conversion
1	*I*	**The first line (PSR-ZVS) reports the last error value**			
	is	“0” in the example is the last error; “2” is last total number of errors starting from power on or form last reset.			
2	**Vin**	**The second line reports the AC input voltage.**			
	Vi	Actual AC voltage			V = *Vi* * 0.448 V
	Vp	AC peak voltage during the last half wave AC cycle.			V = *Vp* * 0.448 V
	Vmin	Minimum input voltage during the last half wave AC cycle.			V = *Vmin* * 0.448 V
	Vmax	Maximum input voltage during the last half wave AC cycle .			V = *Vmax* * 0.448 V
	freq	Shows the input semi-sinusoidal period in units of 100 µS. In the example “freq = 99" is equal to 99 * 100 mS = 9.9 mS, i.e. ~100 Hz (or ~50 Hz full-wave).			T = *freq* * 100 µS
3	**PFC**	**The third line report the PFC status**			
	st	This parameter is a bit mask and each bit reports several PFC information:			
		Bit	**Value**	**Description**	
		0	1 0	Running Disabled	
		1	1	Overcurrent detected.	
		5	0 1	IDLE mode not selected. IDLE mode selected. *Note: during the IDLE mode the serial line is not available therefore the bit can be read by executing the command “st” within 200 ms after using command “pf 2".*	
		6	1	Stable PFC output.	
		7	1	PFC ready but generic error condition detected.	

Table 15. Status information (continued)

<table>
<tr><th>Line</th><th>Parameter</th><th>Description</th><th>Unit conversion</th></tr>
<tr><td></td><td>Vo</td><td>Output voltage. The value is update every 1.25 ms.</td><td>V = Vo * 0.448</td></tr>
<tr><td></td><td>S0</td><td>The actual Toff time.</td><td>T = S0 * 10.4 ns</td></tr>
<tr><td></td><td>S3</td><td>The actual Ton time.</td><td>T = S3 * 10.4 ns</td></tr>
<tr><td></td><td>Maxon</td><td>Maximum on-time. Depends on the AC input voltage. It is used also during the startup phase to limit the input current.</td><td>T = Maxon * 10.4 ns</td></tr>
<tr><td></td><td>I</td><td>Overcurrent protection threshold.</td><td>A = (I * 0.083) / 0.195</td></tr>
<tr><td>4</td><td>HB</td><td>The fourth line reports the HB status</td><td></td></tr>
<tr><td></td><td>st</td><td>This parameter is a bit mask and each bit reports several half bridge information:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th></tr>
<tr><td>0</td><td>1
0</td><td>Running
Disabled</td></tr>
<tr><td>1</td><td>1
0</td><td>Half bridge automatic regulation ON.
Half bridge automatic regulation OFF.</td></tr>
<tr><td>8</td><td>1</td><td>Half bridge ready but generic error detected.</td></tr>
</table></td><td></td></tr>
<tr><td></td><td>Z</td><td>Reserved</td><td></td></tr>
<tr><td></td><td>S0</td><td>Deadtime</td><td>T = S0 * 10.4 ns</td></tr>
<tr><td></td><td>S3</td><td>Half bridge on-time</td><td>T = S3 * 10.4 ns</td></tr>
<tr><td></td><td>dt</td><td>Delay time, as configured by “dt” command.</td><td>T = dt * 10.4 ns</td></tr>
<tr><td></td><td>O</td><td>Reserved</td><td></td></tr>
<tr><td>5</td><td>PW2</td><td>High precision reference status</td><td></td></tr>
<tr><td></td><td>ta</td><td>Target current value as expressed by the user via the “ll: command, DALI or 0 - 10 V interface.</td><td>See Table 14.</td></tr>
<tr><td></td><td>re</td><td>The actual reference voltage.</td><td>V = re * 305 µV</td></tr>
<tr><td></td><td>now</td><td>Actual current value, expressed as a value of the “ll: command'.</td><td>See Table 14.</td></tr>
<tr><td></td><td>O</td><td>Reserved</td><td></td></tr>
<tr><td></td><td>dump</td><td>Reserved</td><td></td></tr>
<tr><td></td><td>ndump</td><td>Reserved</td><td></td></tr>
<tr><td></td><td>TZ_flags</td><td>Reserved</td><td></td></tr>
<tr><td>6</td><td>Z10</td><td>The sixth line is shown only if the 0 - 10 V interface is enabled and shows the 0 - 10 V interface status. The line looks like the following: <code>Z10:765 is 1357, tr = 0 V14 = 845 V3 = 938</code></td><td></td></tr>
<tr><td></td><td>Z10:xxx</td><td>Actual voltage acquired from the ADC line 4 (765 on example). See Table 16 to retrieve the current value associated.</td><td>V = Z10 * 1.22 mV</td></tr>
<tr><td></td><td>is yyyy</td><td>The equivalent “ll” value corresponding to the actual 0 - 10 voltage.</td><td>See Table 14.</td></tr>
<tr><td></td><td>tr</td><td>Difference between the actual and nominal 14 V input.</td><td>V = tr * 16.5 mV</td></tr>
</table>

Table 15. Status information (continued)

Line	Parameter	Description	Unit conversion
	V14	ADC value corresponding to the 14 V input.	V = *V14* * 16.5 mV
	V3	ADC value corresponding to the 3.3 V input.	V = *V3* * 3.462 mV

Default:

Example: “st”:

9.3.3 gp - get PFC status

The “gp” command is used to retrieve the PFC status.

Syntax: gp

Parameters: none

Output:

```
PFC
f=0x0 S0=51 S3=70 e=1 Vo=27 ta=912 S0n=20 pw=0 is=1 lp=0
Mon=70:70 Moff=51:51 on=70:70 off=51:51 s_t=3
L0=:2:1:1:1:2:1
```

Table 16. PFC status information

Line	Parameter	Description	Unit
1	**PFC**		
2	*f*	Reserved	
	S0	Actual variable on-time	T = *S0* * 10.4 ns
	S3	Actual variable on-time	T = *S3* * 10.4 ns
	e	Filter gain (see *Section 3 on page 11*)	
	Vo	Output voltage	V = *Vo* * 0.448 V
	ta	Target output voltage	V = *ta* * 0.448 V
	S0n	Reserved	
	pw	Reserved	
	is	Reserved	
	lp	Reserved	

Table 16. PFC status information (continued)

Line	Parameter	Description	Unit
3	*Mon = xx : yy*	The minimum (xx) and maximum (yy) value of on-time recorded from the last “gp” command execution.	T = xx * 10.4 ns T = yy * 10.4 ns
	Moff = xx : yy	The minimum (xx) and maximum (yy) value of off-time recorded from the last “gp” command execution.	T = xx * 10.4 ns T = yy * 10.4 ns
	on = xx : yy	The minimum (xx) and maximum (yy) value of on-time recorded during the last AC half-cycle.	T = xx * 10.4 ns T = yy * 10.4 ns
	off = xx : yy	The minimum (xx) and maximum (yy) value of off-time recorded during the last AC half-cycle.	T = xx * 10.4 ns T = yy * 10.4 ns
	s_t	Reserved	
4	*L0*	Reserved	

Default: none

Example: gp

9.3.4 gh - get half bridge status

Retrieves the half bridge resonant status.

Syntax: gh

Parameters: none

Output:

```
HB st=0x80 fl=0x0 - s3=61 d0=0 d1=0 Con=65535:0 Ron=61:61
```

Table 17. Half bridge status information

Line	Parameter	Description	Value
1	**HB**		
	st	Is the HB internal status - see “*st*” command to understand.	
	fl	Reserved	
	s3	Actual on-time (without LEB time)	T = s3 * 10.4 ns
	d0	Reserved	
	d1	Reserved	
	Con	Reserved	
	Ron	Reserved	

Reports the HB status where:

Note: All the dump value (d0, d1, Con and Ron field) is correct only if the HB loop is active.

Default: none

Example: gh

9.3.5 ad - get last ADC samples

Command used to retrieve the value of the last analog to digital conversion in all ADC channels. The output value is the digital value acquired directly from the ADC registers.

Syntax: ad

Parameters: none

Output:

```
CH0=28 CH1=287 CH2=0 CH3=0 CH4=0 CH5=855 CH6=933 CH7=0
```

Default: none

Example: ad

Table 18. ADC samples

Channel	Monitor signal (on schematic)	Target value result	Target value unit	Value
CH0	PFC_OUT	408 V	912	V = CH0 * 0.448 V
CH1	CN_CNT	Variable	Variable	V = CH1 * 1.2219 mV
CH2	Vf (D_CH0)	Variable	Variable	V = CH2 * 0.11845 on J4 (total Vf on led strings)
CH3	V_IN -rectified Vac	Variable	Variable	V = CH3 * 0.448 V
CH4	A - 0 - 10 V	Variable	Variable	V = CH4 * 1.22189 mV
CH5	VD_14	14 V	849	V = CH5 * 16.5 mV
CH6	VCC	3.3 V	953	V = CH6 * 3.462 mV
CH7	Not used			

9.3.6 ti - time since power-on

The command shows the STLUX385A device up time. The output is composed of two parts, separated by the comma sign. The first part shows the number of seconds elapsed since power-on or reset. The second part represents the microseconds within the second.

Syntax: ti

Parameters: none

Output:

Default: none

Example: ti

9.3.7 co - clear error

Clears any system errors and switches off the FAULT LED. The command does not clear the error counter tracked by the “st” command. The FAULT LED may turn ON again after the “co” command should the error still be present.

Syntax: co

Parameters: none

Output:

Default: none

Example: co

Warning: The following command changes the behavior of the demonstration board and an incorrect configuration could damage the board.

9.3.8 in - enabled/disable features

Define which feature of the demonstration board are enabled or disabled at startup. With this command is possible to enable or disable the PFC, the half bridge, the DALI I/F or the 0 - 10 V interface. The configuration is stored into EEPROM and applied during the startup or reset. The command uses two parameters: the first identify the feature, the second defines the value.

Syntax: in

Parameters: [parameter] [Value]

Table 19. Startup configuration

First param.	Param. range	Definition

0	0	Shows the value of all configurable parameters stored in EEPROM.
		`1 - PFC = 1 2 - HB = 1 3 - DALI = 1 5 - HB_max = 650 6 - HB_l = 1 7 - Deb = 0 8 - 10 V = 0`
		`9 - PFC_op = 2000 10 -PFC_lp = 1 11 - PFC_dv = 25 12 - PFC_cs = 1`
		Each parameter is identified by its correct “first parameter” as used by the “in” command.

1	0, 1	0: PFC disabled 1: PFC enabled (default)
2	0, 1	0: HB enabled 1: H disabled (default) If the PFC is disabled and HB is enabled, the output current is not regulated correctly since the HB stage is automatically halted.
3	0, 1	0: DALI disabled 1: DALI enabled (default)

Table 19. Startup configuration (continued)

First param.	Param. range	Definition
5		Configures the maximum HB on-time (i.e. minimum frequency), excluding LEB time. The value is calculated as maximum_On_time / 10.4 ns. The default value 650 represents the maximum output power (more than 1A).
6	0, 1	0: disable HB compensation loop. 1: enable HB compensation loop (default). If the compensation loop is disabled, the HB works with a fixed frequency.
7	0, 1	0: enable normal startup procedure (default on new evaluation boards). 1: enable debug mode (default on new firmware upgrades). When debug mode is selected, all STLUX385A outputs are disabled with the exception of the serial line. Only the command interpreter is enabled.
8	0, 1	0: 0 - 10 V interface disabled (default) 1: 0 - 10 V interface enabled The 0 - 10 V and DALI are mutually exclusive. To enable the 0 - 10 V interfaces, first disable the DALI interface, enable the 0 - 10 V interface and reset the board.
10	0, 1	Reserved
11		Reserved
12	0, 1	Reserved

Output:

Default: none

Example: "in 2 1"; enable the half bridge operation

9.3.9 hf - configure half bridge deadtime

The command changes the deadtime applied to the half bridge resonant stage. The minimum configurable deadtime is 250 ns (*val* = 24) while the maximum is 2 µs (val = 192). Val can be calculated as:

Equation 19

$$val = deadtime * (2\ \mu s - 250\ ns) / (192-24) = deadtime * 1750\ ns / 168 = deadtime * 10.42$$

Syntax: hf [val]

Parameters:

val [24-192]: the new deadtime. 24 = 250 ns; 192 = 2 µs. Val = *deadtime* * 10.42.

Output: none

Default: 243 ns.

*Example: "*hf 24": set deadtime to 250 ns.

9.3.10 hb - configure half bridge frequency and status

This command lets the user activate/deactivate the resonant stage and manually configure the half bridge operating frequency. To manually activate the half bridge use "*hb 1*", to deactivate use "*hb 0*" or select the half bridge on-time use "*hb 46-650*".

The total half bridge switching period is given by *Equation 20*:

Equation 20

$$\text{Switching period} = 2^* (val + \text{LEB time} + \text{deadtime}) + 52\ \text{ns}$$

where:

val = configured via *"hb"*

LEB time = 250 ns

deadtime = configured via "*hf*"

Syntax: hf [val]

Parameters:

- val [0,1,46-650]: the new switching frequency or resonant status.
  - 0: switches off the half bridge
  - 1: enables the half bridge
  - 46 - 640: Select the on-time. The on-time value is calculated as *val* * 10.4 ns.
  - *Output:* none

Default: At startup the on-time value is set to 635 ns (val = 61), the deadtime is 344 ns and the LEB time is 250 ns. Therefore, the initial switching frequency is ~400 KHz.

*Example: "*hf 0": switches off the resonant stage.

9.3.11 pf - configure PFC voltage and status

The command is used to activate ("*pf 1*"), deactivate ("*pf 0*") the PFC or change the PFC output voltage. The output voltage can be configured between 390 V (val = 875) and 410 V (val = 920) and. The default value is 920 (410 V).

If the PFC is disabled ("*pf 0*") and resonant is enabled then the output current is not correctly regulated.

Caution: It is strongly suggested to avoid manually switching off the PFC stage while the HB is operating.

Command "pf 2" puts the STLUX into the IDLE mode (only if the resonant stage is off: use "*hb 0*"). Normal operations can be restored only by pushing the DALI button (SW2) or when the board receives a DALI command.

Syntax: pf [val]

Parameters:

- val [0,1,2,875-920]:
  - 0: switch off the PFC
  - 1: enable the PFC
  - 2: enter IDLE mode
  - 875-920: configure desired PFC output voltage (875 = 390 V, 920 = 410 V)

Output: none

Default: 920

*Example: "*val 0": switches off the PFC stage

9.3.12 dt -delay time compensation

This parameter is used to compensate the propagation delay from the falling edge of the PWM of the low-side MOSFET to the internal STLux385A timestamp captured during HB current regulation. See *Section 4.1.3 on page 20* for more details.

The default value is 312.5 nS. The dt value shall include an internal 50 ns delay (comparator delay).

Note that the new value is not stored into the EEPROM area and is defaulted during the startup.

Syntax: dt [val]

Parameters:

val [0,100]: the delay time expressed as: val * 10.4 ns

Output: none

Default: 312.5 ns

*Example: "*dt 30": set the delay time to 312.5 ns.

9.4 Error codes

The STLUX385A firmware performs several system checks during its execution. When an error is found:

1. The red FAULT LED is triggered.
2. The error counter is incremented.
3. The error code is stored in an internal variable. The last error code is reported by the status command (“*st*”).

The FAULT LED can only be reset via the “co” command. The “co” command also clears the error code. The error counter is reset only during power on.

Table 20. Error code

Code	Mnemonic	Meaning	Action
0	ERR_NO_ERR	No error	Nothing
1	ERR_DALI	DALI failure	No action
2	ERR_RESET	The STLUX385A device rebooted without any external reset	No action
3	ERR_PFC_OCD	PFC overcurrent	Stop HB and PFC.
4	ERR_UVLO	Undervoltage condition detected	Stop PFC and HB, automatically restart if AC input voltage returns into correct zone
5	ERR_OCP_0	Not used	
6	ERR_OCP_1	Not used	
7	ERR_OVP_CH0	No load error	Stop HB and PFC, automatically check and restart every 4 second
8	ERR_OVP_CH1	Not used	
9	ERR_OVP_CH2	Not used	
10	ERR_PFC_OT	Error during PFC startup	Restart PFC every 4 second
11	ERR_HB_DUMP	Error during HB timestamping	Output current is not regulated
12	SERV_EE_e	Error during EEPROM write operation	The startup value is not restored due to a write error check
13	ERR_FLASH	Error during EEPROM write operation generated by a DALI operation	Some DALI default initializations are missing
14	ERR_HB_NOL	No load protection: no load detected on the HB	Restart HB every 1 second

9.5 0 - 10 V interface

The 0 - 10 V interfaces can be enabled using the “in” command described in *Section 9.3 on page 46*. By default, the STEVAL385LEDPSR demonstration board is shipped with the 0 - 10 V interface disabled. The 0 - 10 V and DALI interfaces are mutually exclusive.

The 0 - 10 V reference signal can be generated via a 0 - 10 V generator. Alternatively, it is possible to simulate the signal using a potentiometer. The correct value of this potentiometer is 110 KΩ, which can be obtained using two potentiometers in series: 10 KΩ plus 100 KΩ. The 100 KΩ potentiometer shall be used when the output voltage is over 5 V, while the 10 KΩ potentiometer can be used when the output voltage is below 5 V.

The power necessary to read the input voltage is automatically generated by the STEVAL385LEDPSR demonstration board. This solution provides excellent insulation and all the features of the demonstration board. The maximum 0 - 10 V interface input voltage accepted on this is 15 V.

The on/off transaction is regulated via a hysteresis mechanism. LEDs are switched off when the 0 - 10 V interface reaches V < 1 V. LEDs are switched on when V > 1.25 V.

The relationship between the voltage applied to the 0 - 10 V interfaces and the LED output current is defined in *Table 21*.

Table 21. 0 - 10 V voltage to output current

Voltage applied to connector J9	Output current (1 A scale)	Output current (500 mA scale)
More than 10 V and less then 15 V	1 A	500 mA
10 V	1 A	500 mA
9 V	900 mA	450 mA
8 V	800 mA	400 mA
7 V	700 mA	350 mA
6 V	600 mA	300 mA
5 V	500 mA	250 mA
4 V	400 mA	200 mA
3 V	300 mA	150 mA
2 V	200 mA	100 mA
1 V	100 mA	50 mA
Below 1 V	Off	Off

10 Measurements

Section 10.1 reports several measurement results which validate the STEVAL385PSR-ZVS demonstration board performance.

The test environment is composed by:

- “Yokogawa WT210 Digital Power Meter” to measure the input parameters (Vac, Iac, power, power factor, current distortion %)
- Digital oscilloscope “Tektronix DPO7104C 1Ghz - 20GS/s“ to acquire every waveform show into this document
- Current probe “Tektronix TCP0033” to acquired input/output current when is acquired by the digital oscilloscope.
- Multimeter “Keithley 2000” when a secondary voltage or other internal AC or DC voltage is acquired.
- The nominal output load is normally composed by an appropriate numbers of “LCW CQAR.EC-MQMS-5YC8-1” OSLON LEDs by OSRAM Opto Semiconductors with a power dissipation.
- Electronic load “Chroma 6312" with “Chroma 63105 module” used only during PFC tests.

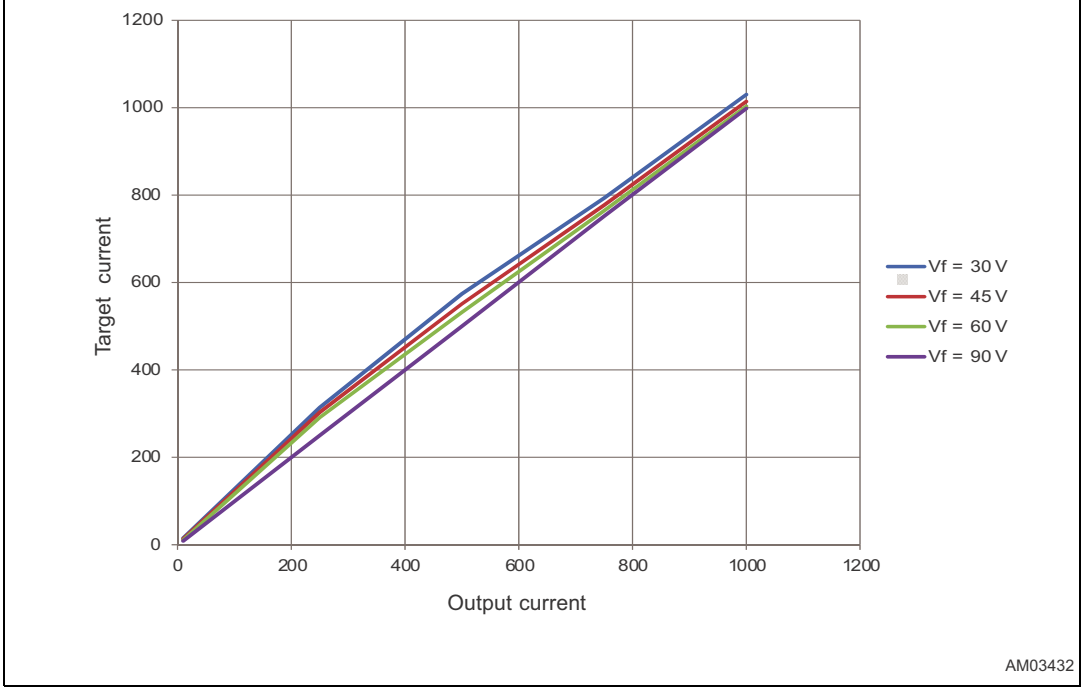
10.1 Output current precision

The first result is to demonstrate the correct current regulation at different Vf and at different output current (imposed by the DALI stack in the linear mode). The DALI working point is 1%, 25%, 50% 75% and 100% of the nominal output power.

Table 22. Output current precision

Nominal output current		Vf = 30 V	Vf = 45 V	Vf = 60 V	Vf = 75 V	Vf = 90 V
DALI	mA	mA	mA	mA	mA	mA
1%	10	15	13	11	10	8.5
25%	250	314	303	291	273	250
50%	500	574	551	532	516	500
75%	750	793	777	764	754	752
100%	1000	1030	1014	1003	998	998

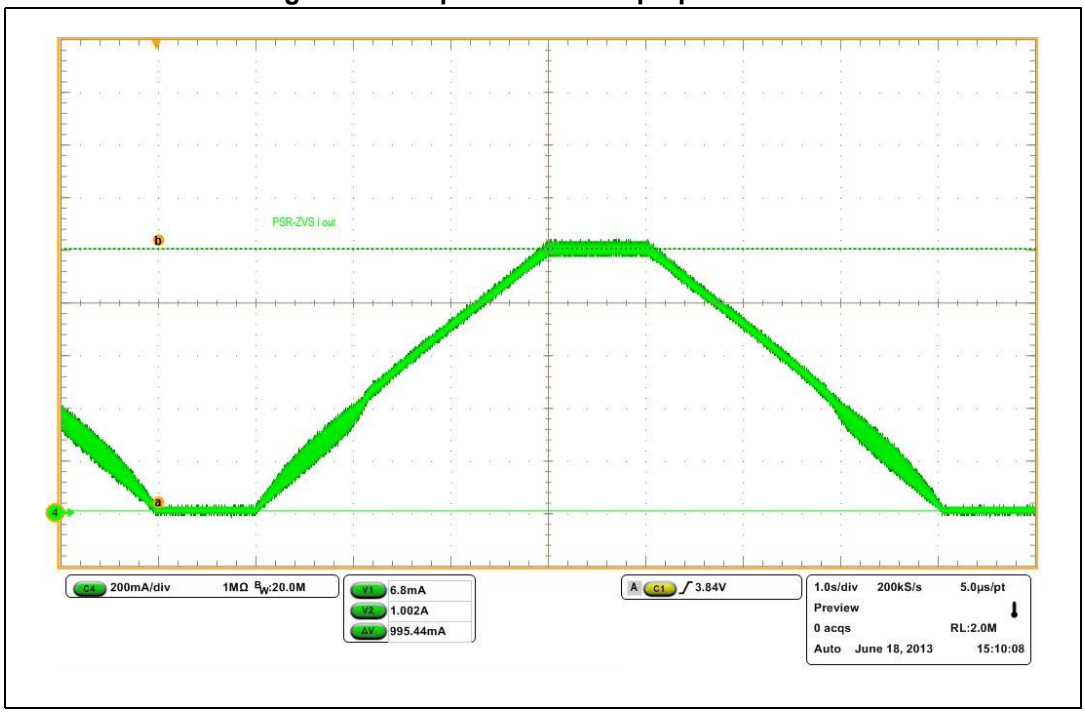
Figure 21. Output current precision



10.2 Output current regulation

This section shows the current transaction from minimum to maximum power and from maximum to minimum power. The output current level is generated using the “recall max level” and “recall min level” DALI commands, each command is sent every 4 second. The output is captured with the current probe acquired on Vf = 90 V. The total transaction (up or down) is completed into 3 seconds.

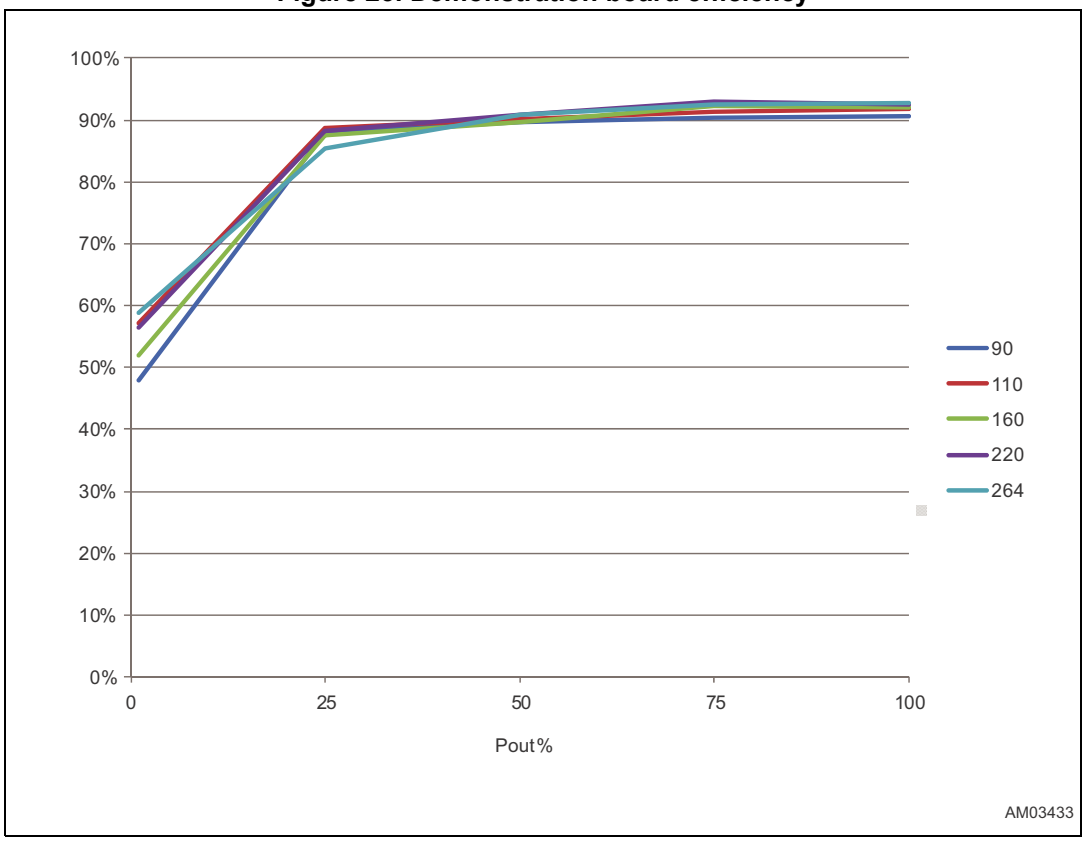
Figure 22. Output current ramp-up and down



10.3 Efficiency

Figure 23 shows the efficiency of the demonstration board at different input AC voltage and at different output power. The output power is applied via DALI commands and the output current is 10 mA, 250 mA, 500 mA, 750 mA and 1 A. The output voltage of this test is fixed at 90 V. The board efficiency peaks at 92% for high loads. When the entire input voltage range is considered, the maximum efficiency at high load is more than 90%.

Figure 23. Demonstration board efficiency



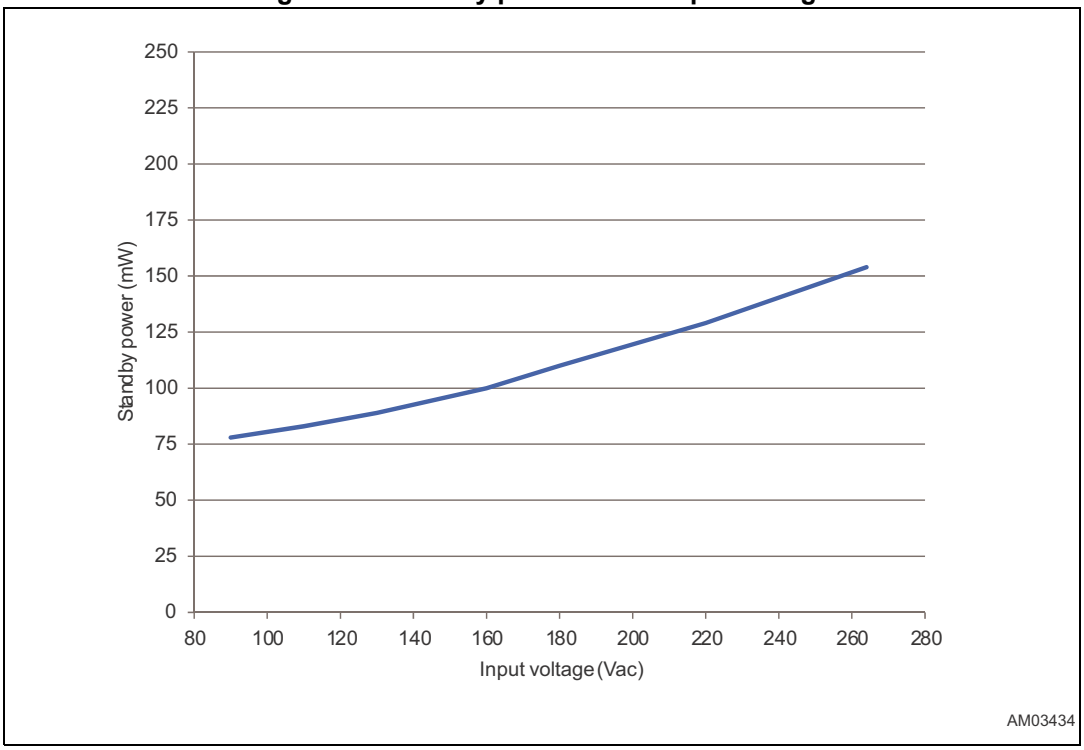
10.4 IDLE and minimum power

In *Table 23* and *Figure 24* is shown the power required from the demonstration board when the DALI sent the power-off command (no current on output LEDs string) and put the demonstration board into the standby mode. The input power required during standby is shown in *Table 23*. Also, *Table 23* shows the minimum input power when the output current during is the lowest (~10 mA).

Table 23. Board standby and minimum power

AC input voltage	IDLE (W)	Active - min. power (W)
90	0.078	1.30
110	0.083	1.35
130	0.089	1.36
160	0.104	1.28
180	0.107	1.20
220	0.129	1.15
264	0.154	1.15

Figure 24. Standby power vs AC input voltage



10.5 Demonstration board power factor and THD

Figure 25 is showing the power factor and the THD distortions of the STEVAL385LEDPSR demonstration board. The value is shown at different input AC voltage and at different load condition.

Figure 25. Demonstration board power factor

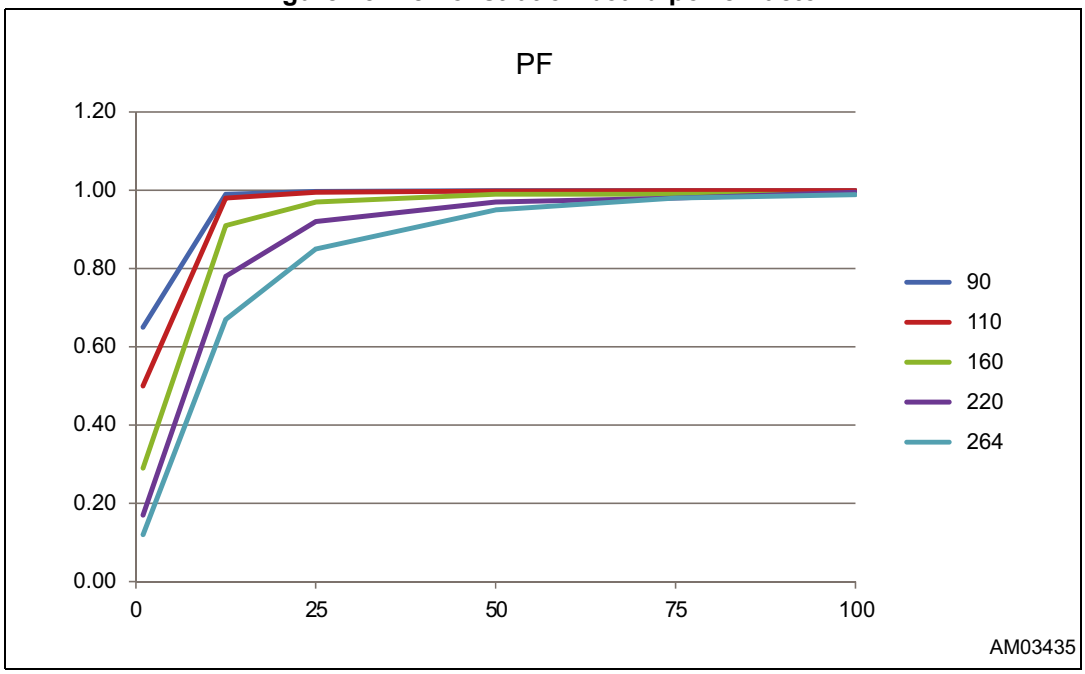
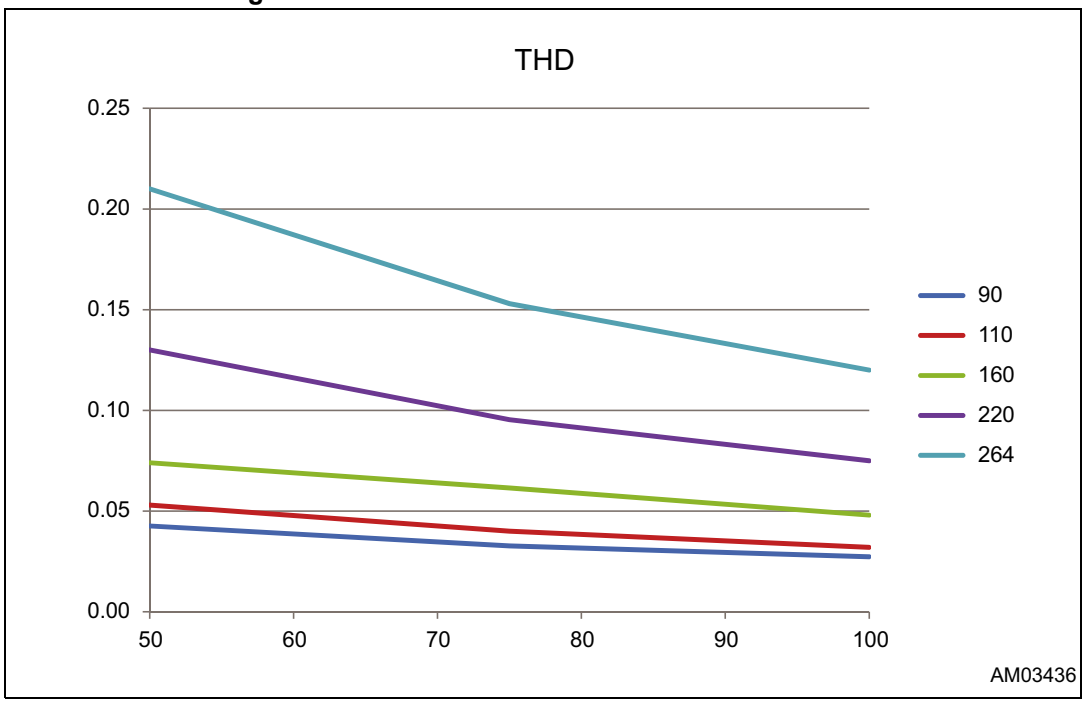


Figure 26. Demonstration board current distorsion



10.6 PFC startup phases

Figure 27 and *Figure 28* illustrate the startup signals generated by the PFC stages as different Vac input voltages are applied to the demonstration board. The maximum PFC startup time is around 500 mS. In *Figure 27* and *Figure 28*, figure the magenta line represents the PFC output voltage while the green line is the AC input current. The half bridge stage is forced to minimum power and there is a low load on the PFC stage.

Figure 27. PFC startup at 110 Vac

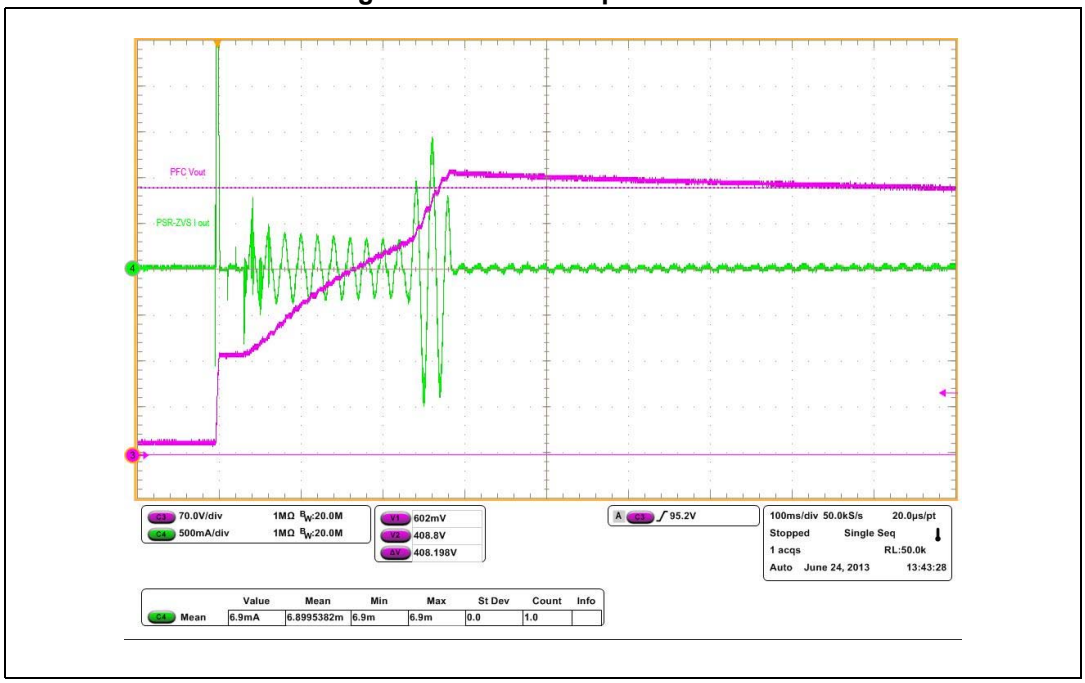
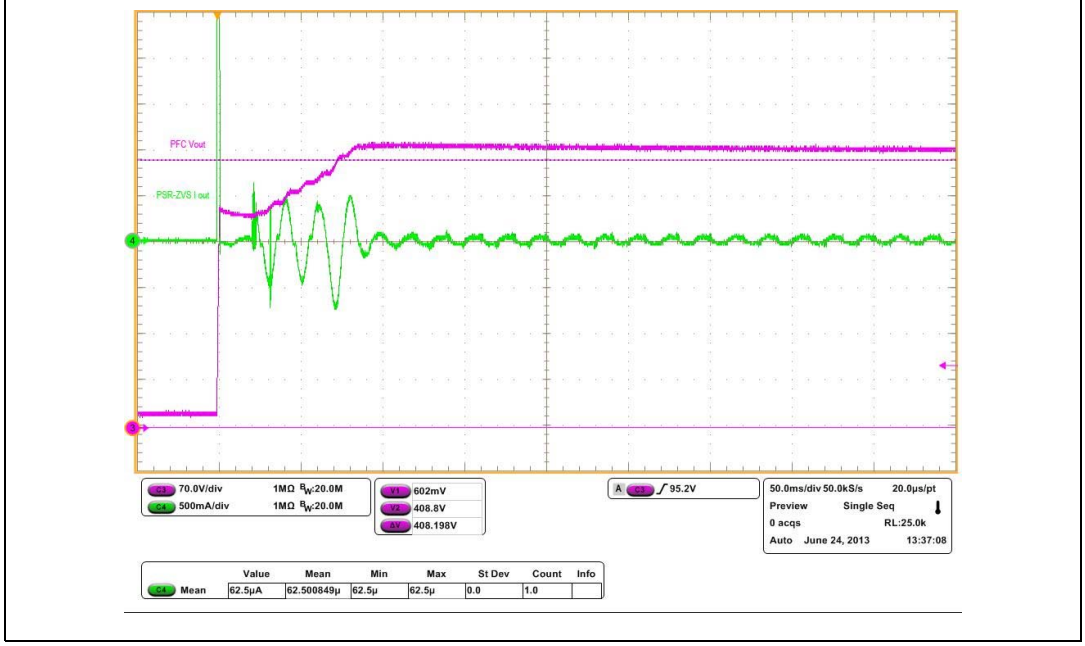


Figure 28. PFC startup at 220 Vac



11 Firmware download procedure

Danger: **High voltage is present on the PSR-ZVS demonstration board.**

Caution: Users must take care about relevant safety procedure before handling the board, even before initiating a firmware upgrade.

The firmware upgrade procedure requires the STM8_pgm.exe program provided by Raisonance. The user shall install the Raisonance RIDE 7 tool. Please refer to www.raisonance.com.

The new firmware is normally provided into a zipped file containing:

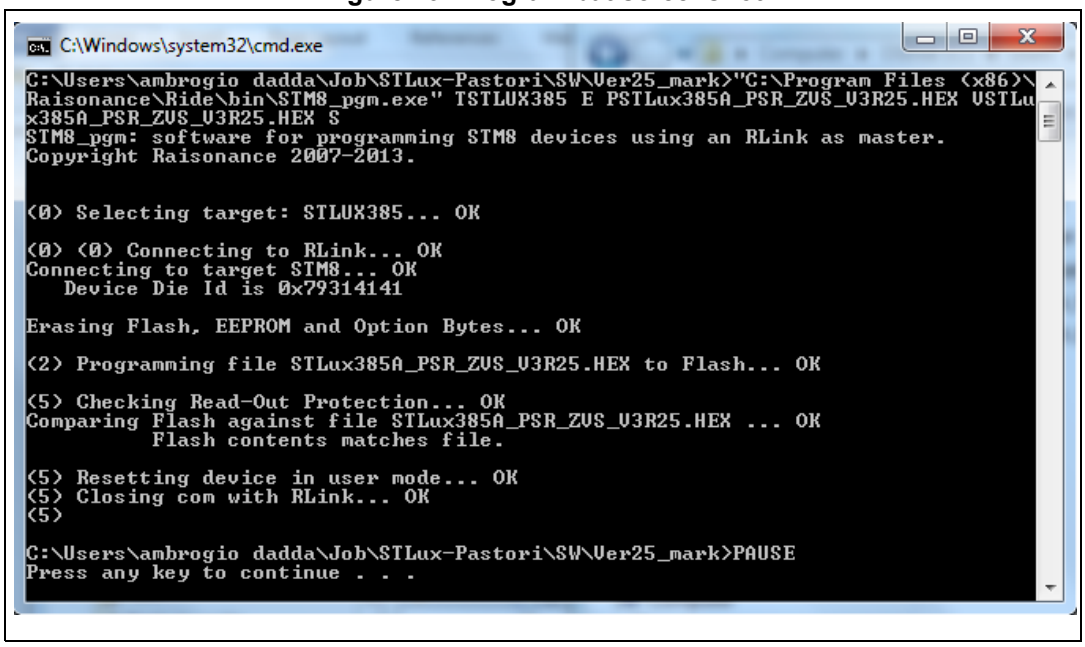
- Firmware (stlux385_PSR_ZVS_V3Rxx.hex file, where the final “xx” refers to the release number)
- Batch file (program.bat)

The batch file instruments the “STM8_pgm.exe” program to erase and program the new firmware to the STLUX385A. The batch file also verifies that the download was successful.

The following steps shall be performed:

1. Modify the “program.bat” batch file to map the current STM8_pgm.exe location.
2. Use an isolated power supply and apply 14 V (+/- 0.5 V) via TP31 (+14 V) and TP25 (GND) without any other power voltage (especially on the AC power line). This condition guarantees the safest firmware upload condition for both the user and the board.
3. Use the “program.bat” procedure. The result of this action is shown in *Figure 29*:

Figure 29. Program.bat screenshot



The user should verify that the output values for each step are marked.

4. Connect the serial interface to the computer.
5. After a correct download the STLUX385A starts and shows the version/release of new firmware, as illustrated in *Figure 30*:

Figure 30. Power-up message after a firmware update

```
EVAL STLUX385-PSR-ZVS V3R20
Build Jul  1 2013 16:01:26 core is 385A
HALT - Debug Mode Activated
```

6. After a firmware upgrade, the application starts in a safety mode. All the output PWMs are kept to low levels and both PFC and half bridge stages are disabled. This mode is identified by the string “HALT - Debug Mode Activated” shown on screen. Also the green status LED toggles (1 second on and 1 second off) on the green LED (RUN).
7. To enable the board operation, the users have to use the “in” command on the serial line, using the proper parameters as described in *Section 9.3*. The command used to enable the full functionality is “in 7 0". Only after a new power-on or a reset the new configurations are applied and the STEVAL385LEDPSR demonstration board starts with full functionality and the startup message is changed into:

Figure 31. Power-up message of a fully enabled board

```
EVAL STLUX385-PSR-ZVS V3R20
Build Jul  1 2013 16:01:26 core is 385A
Option PFC HB Dali enabled
Ready
```

As an example, in the screen capture, the PFC is active, the half bridge is active and the DALI interfaces is enable. Note the “Ready” message; it states that the STEVAL385LEDPSR board is ready to receive a new serial line command.

12 Revision history

Table 24. Document revision history

Date	Revision	Changes
04-Feb-2014	1	Initial release.

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