HD74HCT237

3-to-8-line Decoder/Demultiplexer with Address Latch

HITACHI

Description

The HD74HCT237 decodes a three-bit Address to one-of-eight active-high outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Select as a data input while holding the other one active.

The HD74HCT237 is the noninverting version of the HD74HCT137.

Features

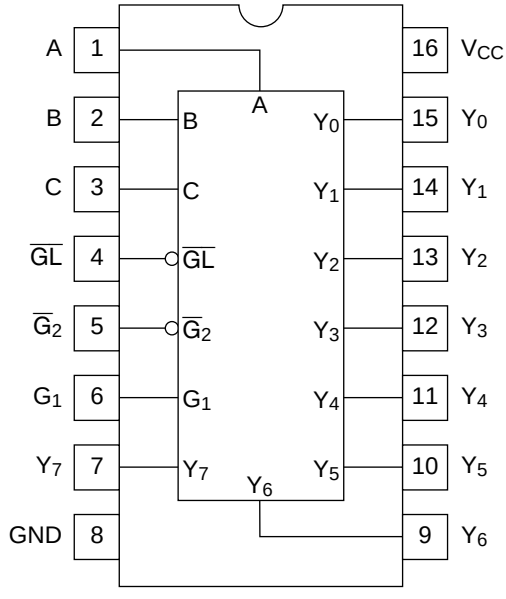
- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (A, B, C to Y) = 23 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 4.5 to 5.5 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

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Function Table

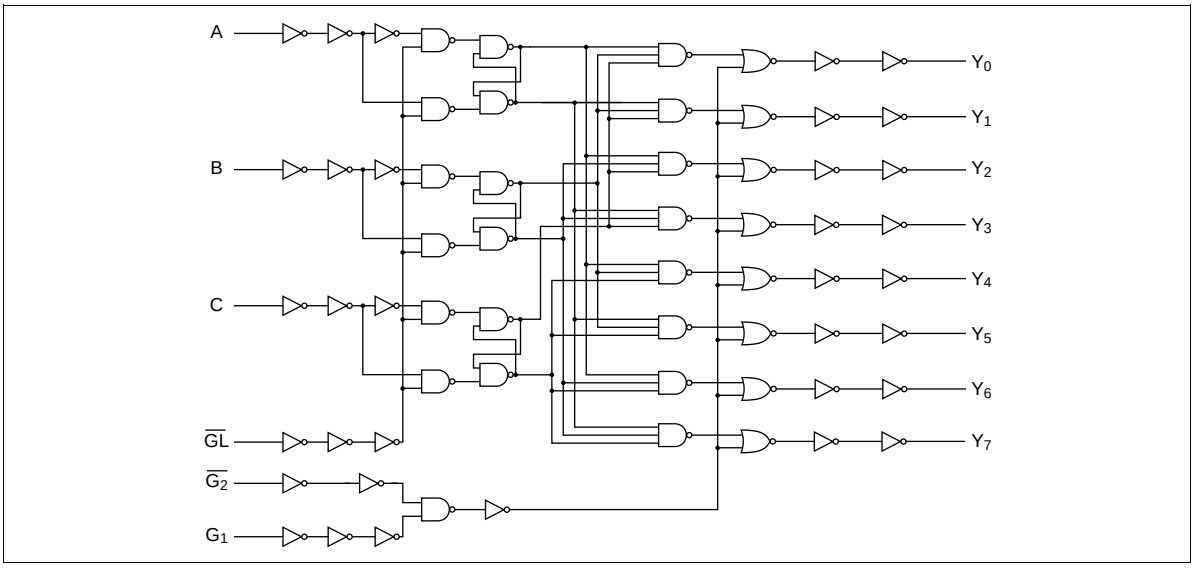
Inputs													
Enable			Select			Outputs							
$\overline{GL}$	G_1	$\overline{G}_2$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output Corresponding to stored address L; all others H							

Pin Arrangement



(Top view)

Logic Diagram



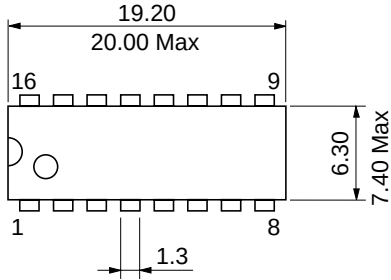
DC Characteristics

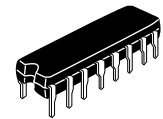
Item	Symbol	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions V_{cc} (V)		
Input voltage	V_{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5		
	V_{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5		
Output voltage	V_{OH}	4.4	—	—	4.4	—	V	4.5	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.18	—	—	4.13	—		4.5		I_{OH} = –4 mA
	V_{OL}	—	—	0.1	—	0.1	V	4.5	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		—	—	0.26	—	0.33		4.5		I_{OL} = 4 mA
Input current	Iin	—	—	±0.1	—	±1.0	µA	5.5	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	—	—	4.0	—	40	µA	5.5	Vin = V_{CC} or GND, Iout = 0 µA	

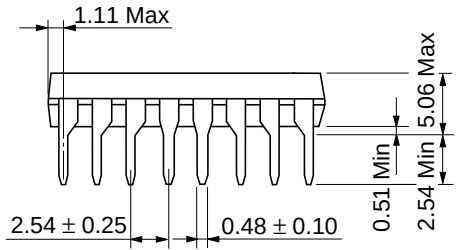
AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

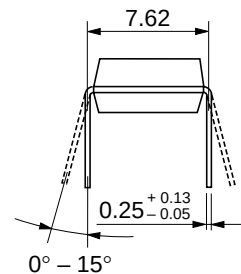
		Ta = 25°C			Ta = –40 to +85°C			Test Conditions	
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**V_{cc} (V)**	
Propagation delay time	t_{PLH}	—	21	37	—	46	ns	4.5	A, B or C to Y
	t_{PHL}	—	25	37	—	46		4.5	
	t_{PLH}	—	18	29	—	36	ns	4.5	$\overline{G_2}$ to Y
	t_{PHL}	—	14	29	—	36		4.5	
	t_{PLH}	—	16	29	—	36	ns	4.5	G_1 to Y
	t_{PHL}	—	18	29	—	36		4.5	
	t_{PLH}	—	22	38	—	48	ns	4.5	$\overline{GL}$ to Y
	t_{PHL}	—	27	38	—	48		4.5	
Pulse width	t_w	16	8	—	20	—	ns	4.5	
Setup time	t_{su}	20	6	—	25	—	ns	4.5	
Hold time	t_h	5	–1	—	5	—	ns	4.5	
Output rise/fall time	t_{TLH} t_{THL}	—	5	15	—	19	ns	4.5	
Input capacitance	Cin	—	5	10	—	10	pF	—	

Unit: mm



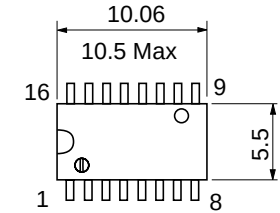


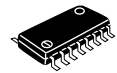


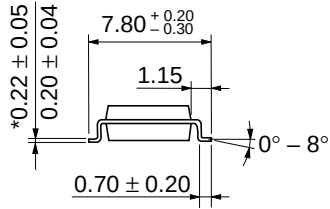


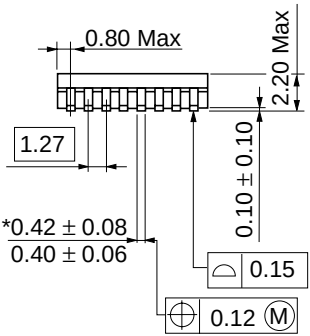
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





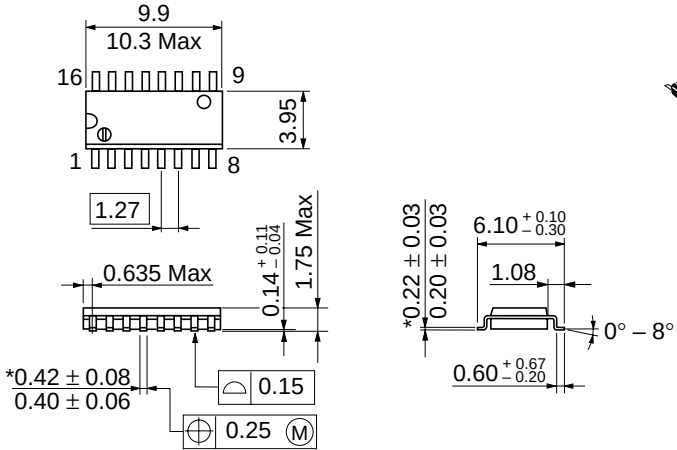


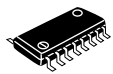


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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