Version :5.0

TECHNICAL SPECIFICATION

MODEL NO : PM102ZY3

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Please contact PVI or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

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FOR MORE INFORMATION:
AZ DISPLAYS, INC.
75 COLUMBIA, ALISO VIEJO, CA 92656
Http://www.AZDISPLAYS.com

Confirmed By Tommy Chang

Prepared By

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Revision History

Rev.	Issued Date	Revised Content
1.0	Oct 26, 2007	New
2.0	March.24.2008	Add Page 25 14.Handling Cautions 14-1 item d) Modify Page 4 2. Features
3.0	June 16,2008	Delete page: 14 10.Block Diagram 10-1) TFT-module Black Diagram If you use PM102ZY3, you can apply PVI- 2003A(Timing controller) which will timing signal to support PM102ZY3.
4.0	Dec.31.2008	Modify Page 11 6. Absolute Maximum Ratings Add Storage Temperature & Operation Temperature
5.0	August.19, 2009	Modify Page28 16.packing

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TECHNICAL SPECIFICATION

CONTENTS

NO.	*ITEM*	*PAGE*
-	Cover	1
-	Revision History	2
-	Contents	3
1	Application	4
2	Features	4
3	Mechanical Specifications	4
4	Mechanical Drawing of TFT-LCD module	5
5	Input / Output Terminals	7
6	Absolute Maximum Ratings	10
7	Electrical Characteristics	10
8	Pixel Arrangement	12
9	Display Color and Gray Scale Reference	13
10	Block Diagram	14
11	Interface Timing	15
12	Power On Sequence	21
13	Optical Characteristics	21
14	Handling Cautions	25
15	Reliability Test	27
16	Packing Diagram	28

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1.Application

This data sheet applies to a color TFT LCD module, PM102ZY3. The module applies to OA product, GPS, which require high quality flat panel display. If you must use in high reliability environment can't over reliability test condition.

2.Features

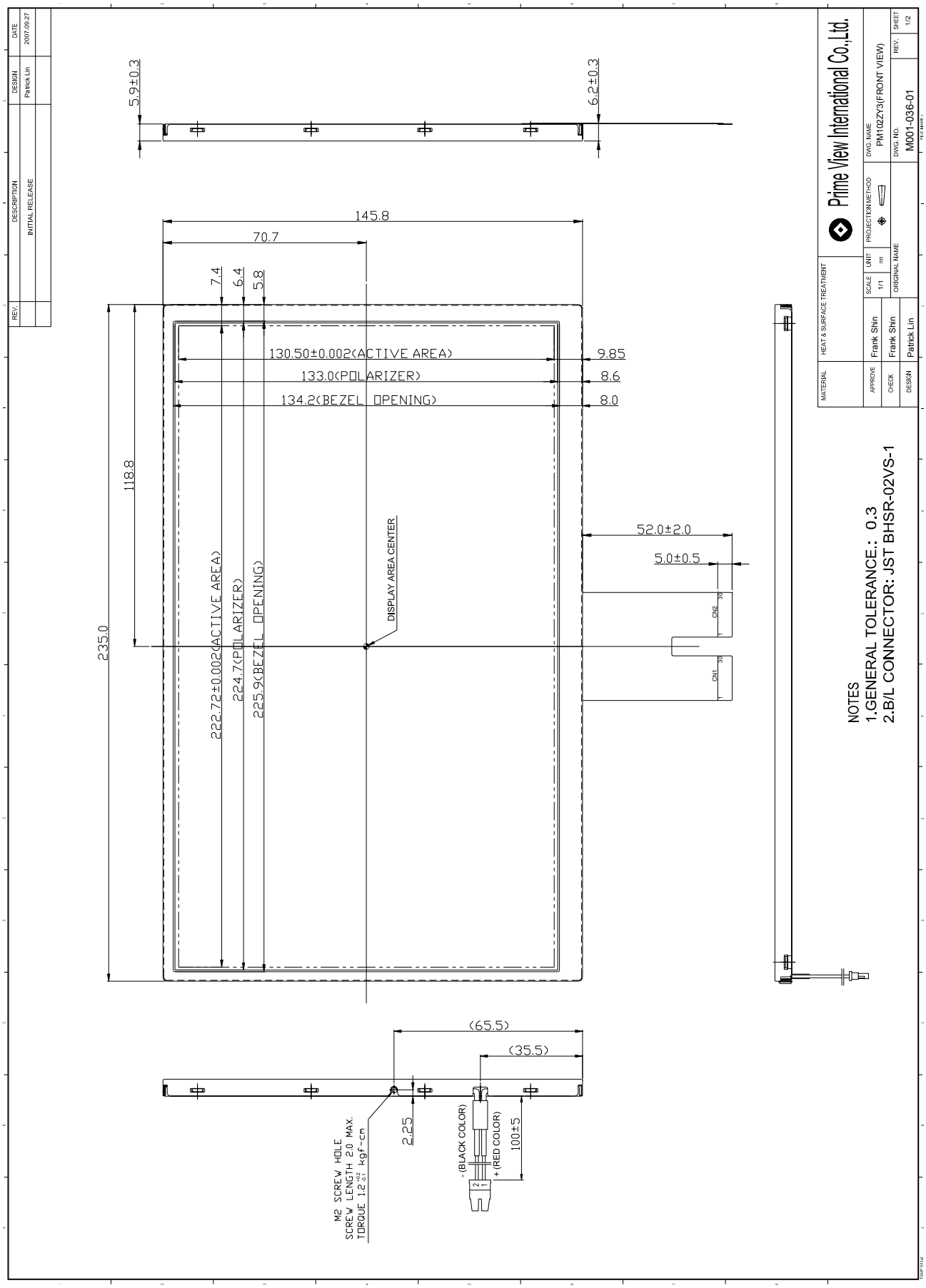
. WSVGA (1024*600 pixels) resolution
. Amorphous silicon TFT LCD panel with LED back-light unit
. Pixel in stripe configuration
. Thin and light weight
. Display Colors：262,144 colors
. Optimum Viewing Direction：6 o'clock
. Support TTL/RSDS interface.

3.Mechanical Specifications

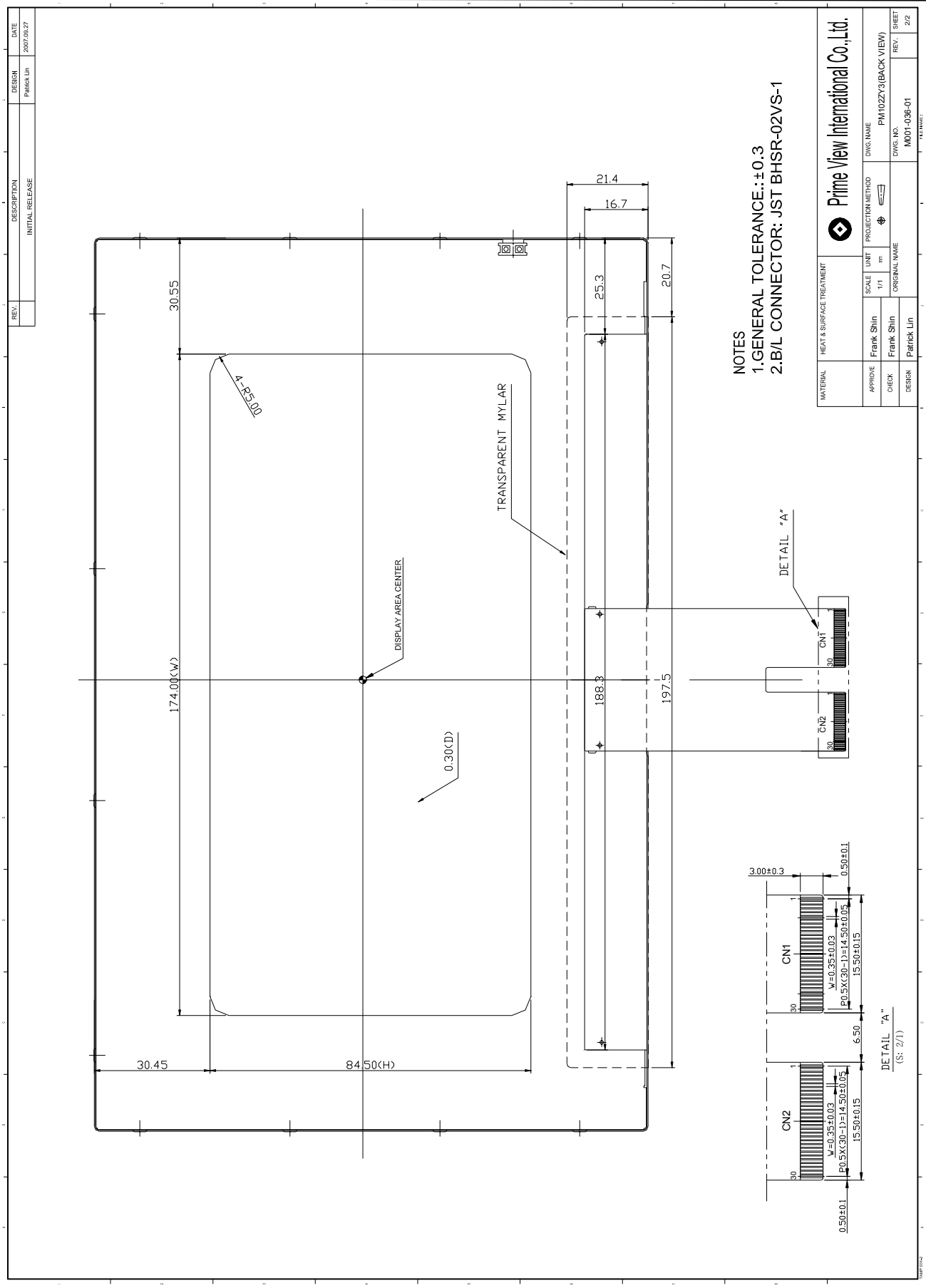
Parameter	Specifications	Unit
Screen Size	10.2" (diagonal)	inch
Display Format	1024×(RGB)×600	dot
Display Colors	262,144	
Active Area	222.72(H)×130.5(V)	mm
Pixel Pitch	0.2175(H)×0.2175(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	235.0(W)×145.8(H)×6.2(D) (typ.)	mm
Weight	314±15	g
Surface treatment	Anti-Glare and E/Wide View Film	
Display mode	Normally white	
Gray scale inversion direction	6 (ref to Note 13-1)	o'clock
Back-light	48-LED	

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4. Mechanical Drawing of TFT-LCD Module



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5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

FPC Down Connect, 30 Pins, Pitch: 0.5 mm

CN 1

Pin No.	Symbol	I/O	Function	Remark
1	DIO1	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-6
2	VSS1	I	Ground	
3	VDD1	I	Power Supply	
4	CLK	I	Shift Clock input	Note 5-10
5	CLKN	I	RSDS Shift Clock input	Note 5-11
6	R/L	I	Right / Left selection	Note 5-6
7	R0(D00)	I	Red Data (LSB)	Note 5-13
8	R1(D01)	I	Red Data	
9	R2(D02)	I	Red Data	
10	R3(D03)	I	Red Data	
11	R4(D04)	I	Red Data	
12	R5(D05)	I	Red Data (MSB)	
13	VSS1	I	Ground	
14	G0(D10)	I	Green Data (LSB)	Note 5-13
15	G1(D11)	I	Green Data	
16	G2(D12)	I	Green Data	
17	G3(D13)	I	Green Data	
18	G4(D14)	I	Green Data	
19	G5(D15)	I	Green Data (MSB)	
20	VSS1	I	Ground	
21	B0(D20)	I	Blue Data (LSB)	Note 5-13
22	B1(D21)	I	Blue Data	
23	B2(D22)	I	Blue Data	
24	B3(D23)	I	Blue Data	
25	B4(D24)	I	Blue Data	
26	B5(D25)	I	Blue Data (MSB)	
27	LD	I	Load output signal	Note 5-7
28	REV	I	Data invert control	Note 5-8
29	POL	I	Polarity selection	Note 5-9
30	DIO2	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-6

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CN 2

Pin No.	Symbol	I/O	Function	Remark
1	VSS2	I	Ground	
2	V1	I	Gamma Voltage 1	Note 5-14
3	V2	I	Gamma Voltage 2	
4	V3	I	Gamma Voltage 3	
5	V4	I	Gamma Voltage 4	
6	V5	I	Gamma Voltage 5	
7	V6	I	Gamma Voltage 6	
8	V7	I	Gamma Voltage 7	
9	VSS2	I	Ground	
10	V8	I	Gamma Voltage 8	Note 5-14
11	V9	I	Gamma Voltage 9	
12	V10	I	Gamma Voltage 10	
13	V11	I	Gamma Voltage 11	
14	V12	I	Gamma Voltage 12	
15	V13	I	Gamma Voltage 13	
16	V14	I	Gamma Voltage 14	
17	VSS2	I	Ground	
18	VDD2	I	Voltage for analog circuit	Note 5-14
19	VCOM	I	Common Voltage	
20	TTL/RSDS	I	TTL / RSDS Input mode Selection	Note 5-12
21	OE	I	Output Enable	Note 5-5
22	U/D	I	Up / Down Selection	Note 5-3
23	CKV	I	Vertical Shift Clock	Note 5-4
24	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note 5-3
25	STVD	I/O	Vertical Shift Pulse Signal Input or Output	
26	VGG	I	Gate On Voltage	Note 5-2
27	GND	I	Ground	
28	VCC	I	Voltage for logic circuit	
29	GND	I	Ground	
30	VEE	I	Gate Off Voltage	Note 5-1

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Note 5-1: Gate off voltage, VEE=-5.6V

Note 5-2: Gate on voltage, VGG=17V

Note 5-3: Select up or down shift

U/D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down

Note 5-4: Gate driver shift clock

Note 5-5: When OE is connected to high "1", the driver outputs are disabled (Gate output = VEE). Under this condition, the operation of registers will not be affected.

Note 5-6: Select left or right shift

R/L	DIO1	DIO2	Shift
1	Input	Hi-Z	Left to Right
0	Hi-Z	Input	Right to Left

Note 5-7: Latch the polarity of outputs and switch the new data to outputs. At the rising edge (LD), latch the "POL" signal to control the polarity of the outputs.

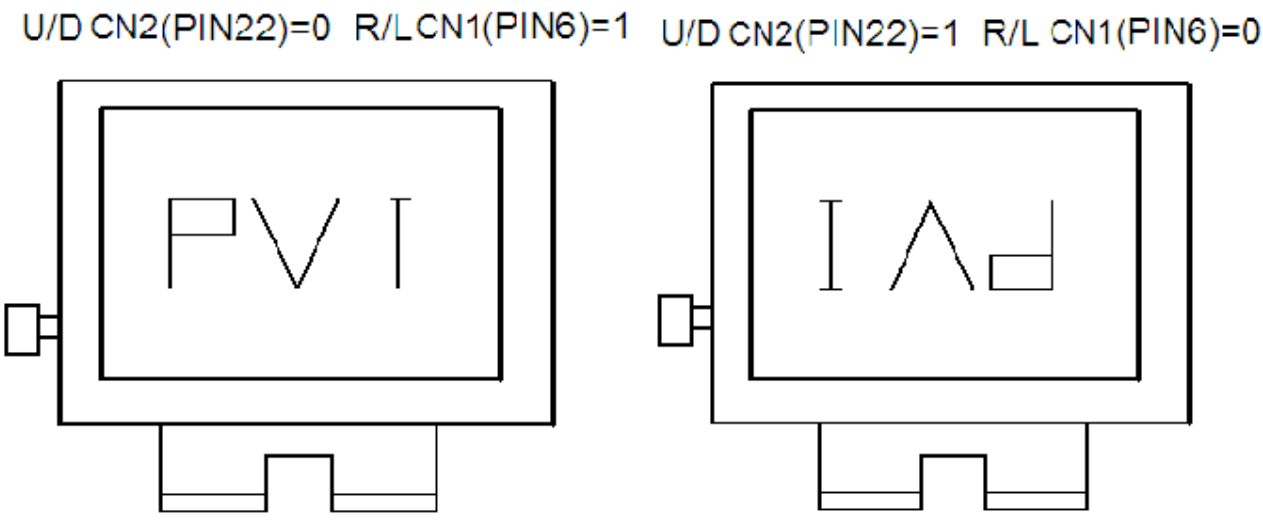
Note 5-8: Control whether the Data R0~G5 are inverted or not. (PVI suggests connecting to GND)
When "REV=1", these data will be inverted.
EX: "00"→"3F", "07"→"38", "15"→"2A"

Note 5-9: Polarity selector for dot-inversion control. Available at the rising edge of LD.
When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14; When POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 5-10: Clock signal. When RSDS input mode, CLK is used as CLKP input pin.

Note 5-11: The RSDS clock input pairs generate the internal shift clock through the comparison between CLKP and CLKN. When TTL mode, connect to GND.

Note 5-12: TTL/RSDS=H: RSDS data input
TTL/RSDS=L or open: TTL data input

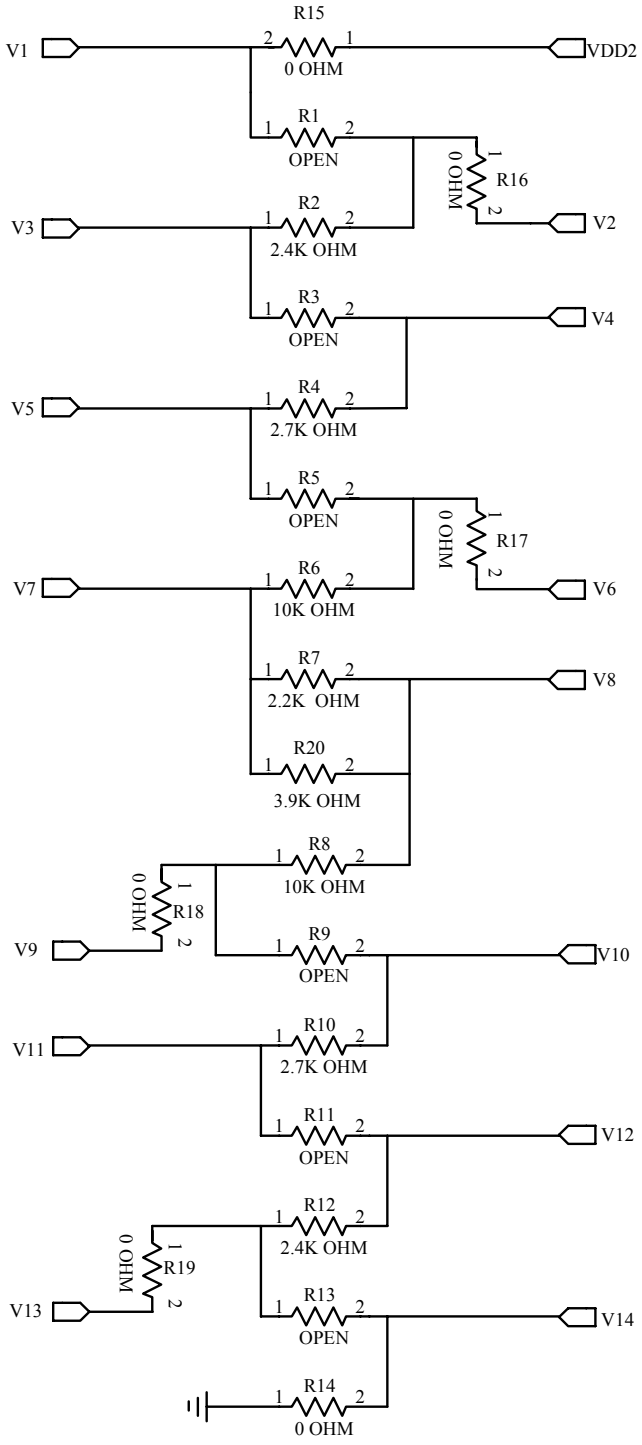


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Note 5-13:

Pin name	RSDS input mode TTLRSDS = H	TTL input mode TTLRSDS = L
D04,D02,D00	D0[2:0]N	D04,D02,D00
D05,D03,D01	D0[2:0]P	D05,D03,D01
D14,D12,D10	D1[2:0]N	D14,D12,D10
D15,D13,D11	D1[2:0]P	D15,D13,D11
D24,D22,D20	D2[2:0]N	D24,D22,D20
D25,D23,D21	D2[2:0]P	D25,D23,D21

Note 5-14:Typical Application Circuit (When VDD2 = 9.1V)



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5-2) Backlight driving

Connector type: JST BHSR-02VS-1

Pin No	Symbol	Description	Remark
1	+	Input terminal (Anode)	Red
2	-	Input terminal (Cathode)	Black

6. Absolute Maximum Ratings: VSS1=VSS2= GND=0V,Ta=25℃

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	VDD1	-0.5	5.0	V	
	VCC	-0.3	6.0	V	
	VDD2	-0.5	12.0	V	
	VGG	-0.3	40.0	V	
	VGG-VEE	-0.3	40.0	V	
	VEE	-20	0.3	V	
Storage Temperature	Tst	-30	+80	℃	
Operation Temperature	Top	-20	+80	℃	

7.Electrical Characteristics

7-1) Recommended Operating Conditions : VSS1=VSS2= GND =0V,Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	VDD1	3.0	3.3	3.6	V	
	VDD2	8.6	9.1	9.6	V	
Supply Voltage for Gate Driver	VGG	-	17	-	V	
	VEE	-	-5.6	-	V	
	VCC	3.0	3.3	3.6	V	
VCOM Voltage	VCOM	-	3.6	-	V	
Digital Input Voltage	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	
	V_{IL}	0	-	0.3 V_{CC}	V	

7-2) Recommended driving condition for LED back light

Ta = 25℃

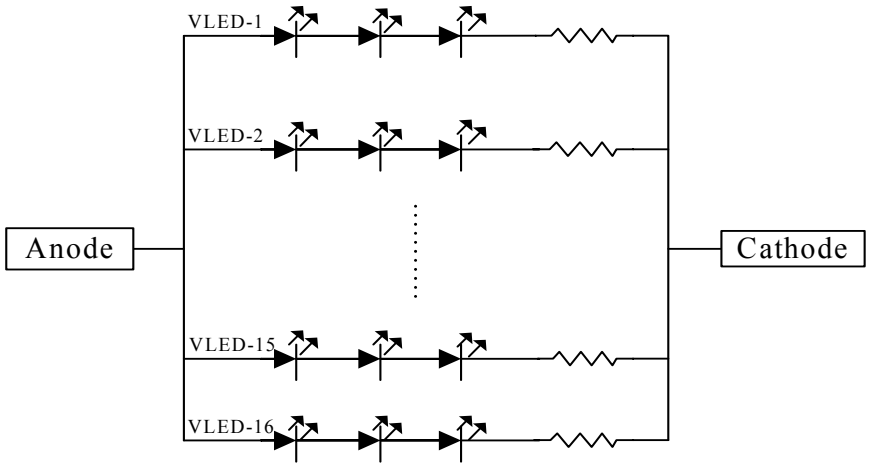
Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V_{LED}	-	-	(11.0)	V	Note 7-1
Supply current of LED backlight	I_{LED}	-	20		mA	Note 7-2
Backlight Power Consumption	P_{LED}	-	-	3.52	W	Note 7-1,Note 7-3

Note 7-1 I_{LED} =20mA, Constant Current

Note 7-2 : The LED driving condition is defined for each LED module. (3 LED Serial) Input current = 20mA * 16 =320mA

Note 7-3 : $P_{LED} = V_{LED-1} * I_{LED-1} + V_{LED-2} * I_{LED-2} \ldots\ldots + V_{LED-15} * I_{LED-15} + V_{LED-16} * I_{LED-16}$

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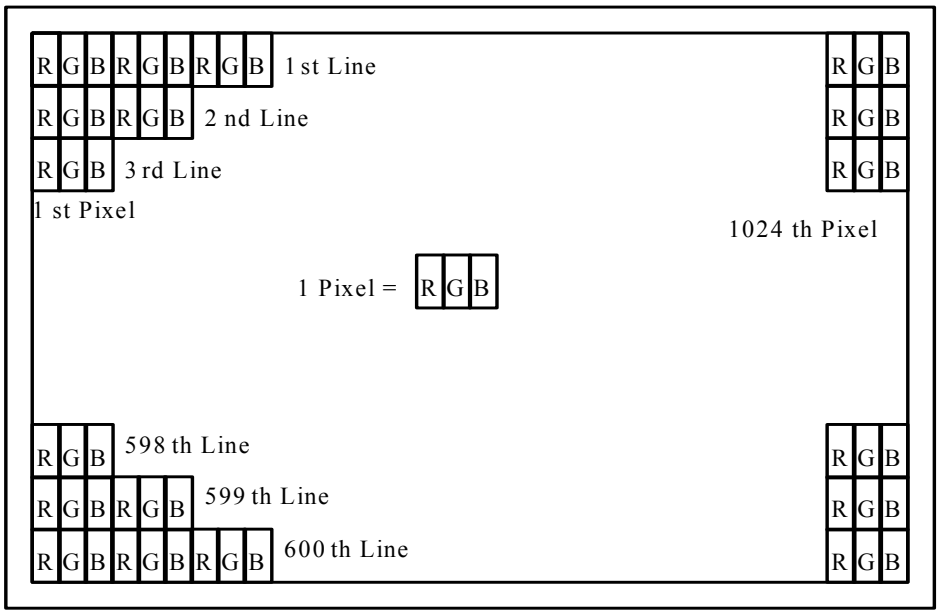


7-3)Power Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	IGG	VGG= 17V	0.19	0.57	mA	
Supply Current for Gate Driver (Low level)	IEE	VEE=-5.6V	0.98	2.94	mA	
Supply Current for Source Driver (Digital)	IDD1	VDD1= 3.3V	8.36	16.72	mA	
Supply Current for Source Driver (Analog)	IDD2	VDD2= 9.1V	35.07	70.14	mA	
Supply Current for Gate Driver (Digital)	ICC	VCC= 3.3V	0.02	0.06	mA	
LCD Panel Power Consumption	-	-	355.5	719.8	mW	Note 7-4
Back Light LED Power Consumption	-	-	-	3.52	W	Note 7-5
Total Power Consumption	-	-	-	4.24	W	

Note 7-4: The power consumption for backlight is not included.
Note 7-5: Back light power consumption is calculated by $I_L \times V_L$.

8. Pixel Arrangement



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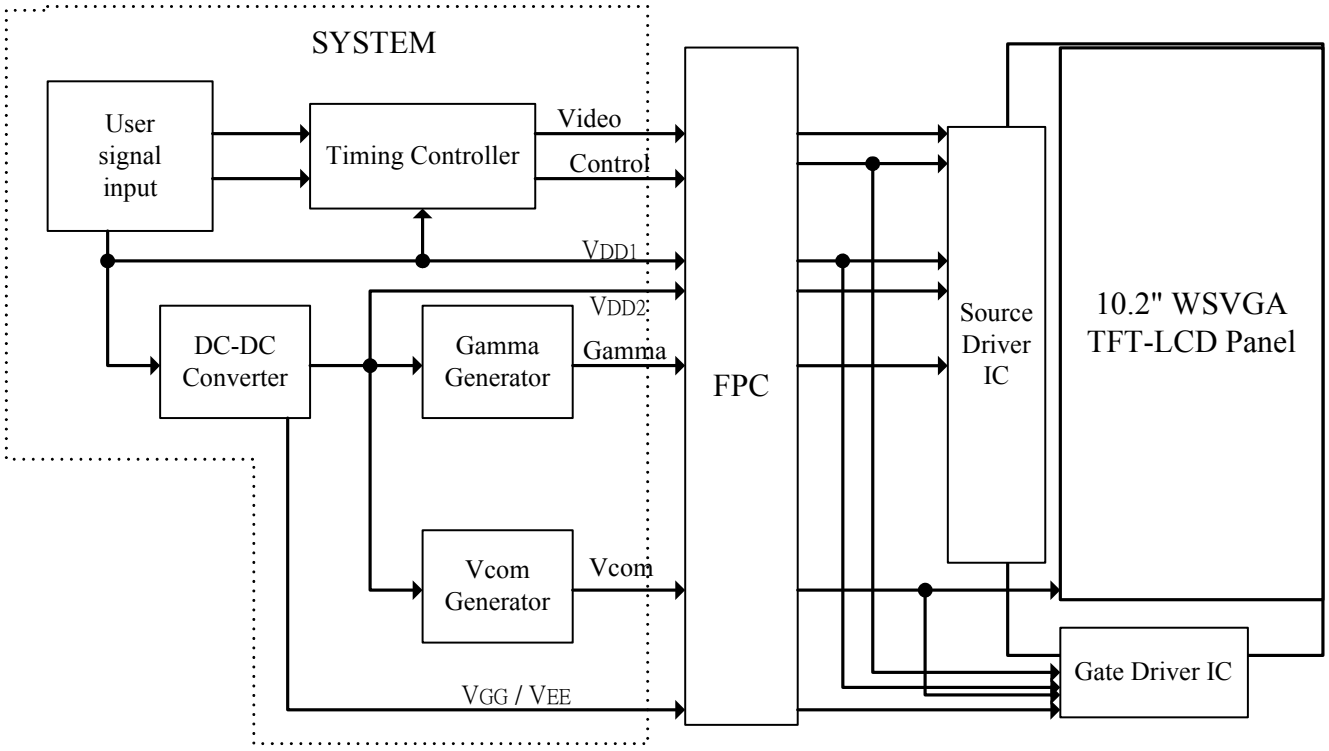
9. Display Color and Gray Scale Reference

Color		Input Color Data																	
		Red						Green						Blue					
		R5	**R4**	**R3**	**R2**	**R1**	**R0**	**G5**	**G4**	**G3**	**G2**	**G1**	**G0**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

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10. Block Diagram

10-1) TFT-module Block Diagram



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11. Interface Timing

11-1) Timing Parameters

AC Electrical Characteristics (VDD1=VCC=3.3V, VDD2=9.1V, GND=VSS1=VSS2=0V) Ta=25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Frequency	Fclk	-	50	55	MHz	
CLK Pulse Width	Tcw	18	-	-	ns	
Data Set-up Time	Tsu	4	-	-	ns	
Data Hold Time	Thd	2	-	-	ns	
Propagation Delay of DIO2/1	Tphl	6	10	15	ns	
Time That The Last Data to LD	Tld	1	-	-	Tcw	
Pulse width of LD	Twld	2	-	-	Tcw	
Time That LD to DIO1/2	Tlds	5	-	-	Tcw	
POL Set-up Time	Tpsu	6	-	-	ns	
POL Hold Time	Tphd	6	-	-	ns	
OE Pulse Width	T_{OEV}	1	-	-	μs	
CKV Pulse Width	T_{CKV}	500	-	-	ns	
STV Set-up Time	T_{SUV}	400	-	-	ns	
STV Hold Time	T_{HDV}	400	-	-	ns	
Horizontal Display Period	T_{HDP}	1024	1024	1024	Tcw	
Horizontal Period Timing Range	T_{HP}	1200	1344	1466	Tcw	
Horizontal Lines Per Field	T_V	-	625	-	T_{HP}	
Vertical Display Timing Range	T_{DV}	600	600	600	T_{HP}	
RSDS Low level Input Voltage	Vilrsds	-	-200	-100	mV	D2[2:0]P,D2[2:0]N, CLKP,CLKN
RSDS High level Input Voltage	Vihrsds	100	200	-	mV	D2[2:0]P,D2[2:0]N, CLKP,CLKN
RSDS reference Voltage	Vcomrsds	VSS1+0.1	1.2	VDD1-1.2	V	D2[2:0]P,D2[2:0]N, CLKP,CLKN

11-2) Timing Diagram

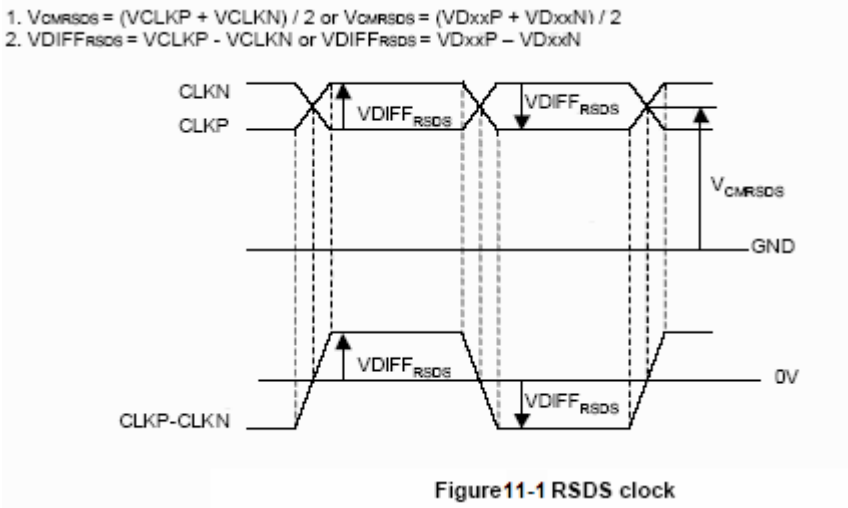


Figure11-1 RSDS clock

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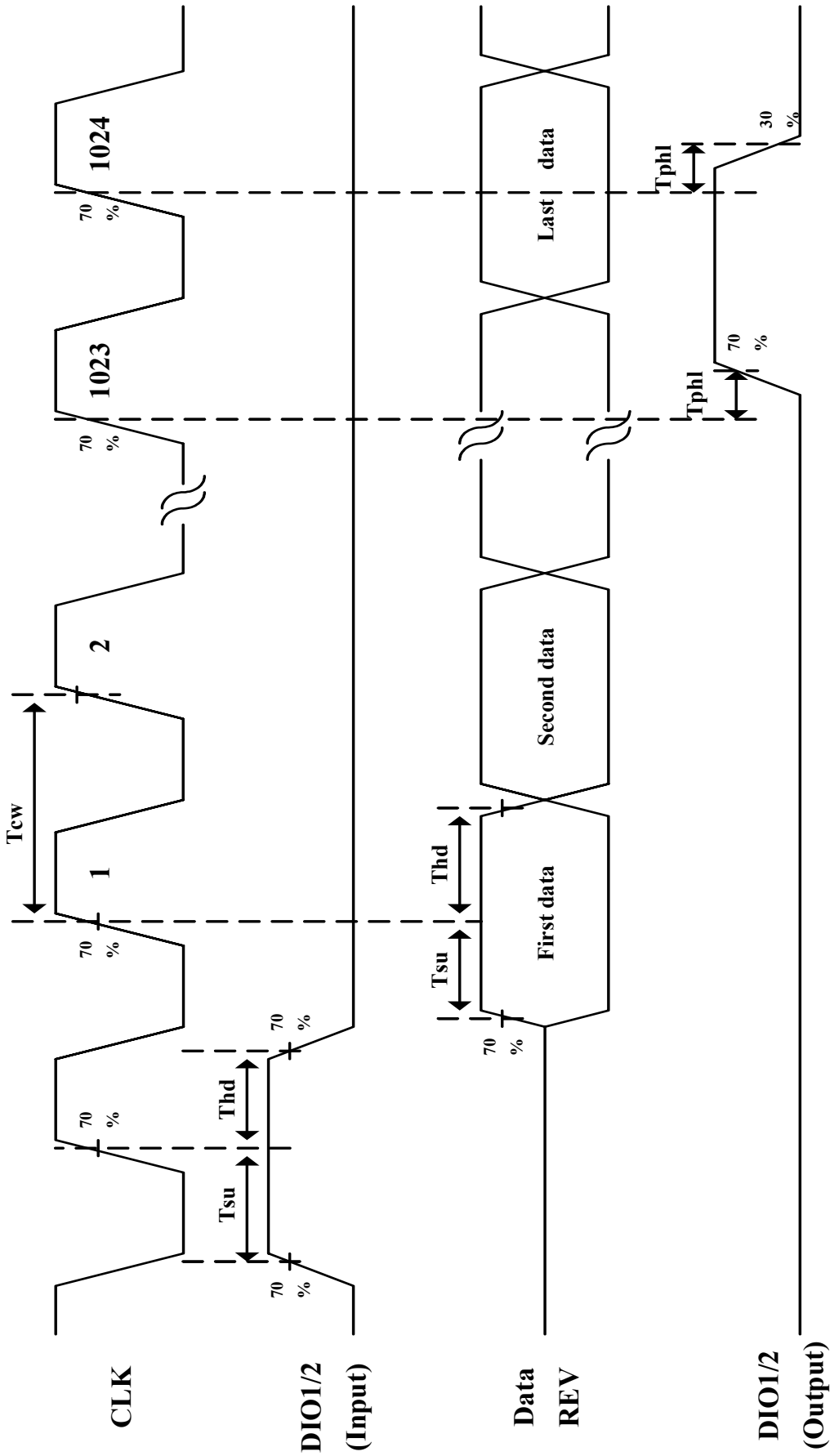


Fig. 11-2 Horizontal timing-TTL(1)

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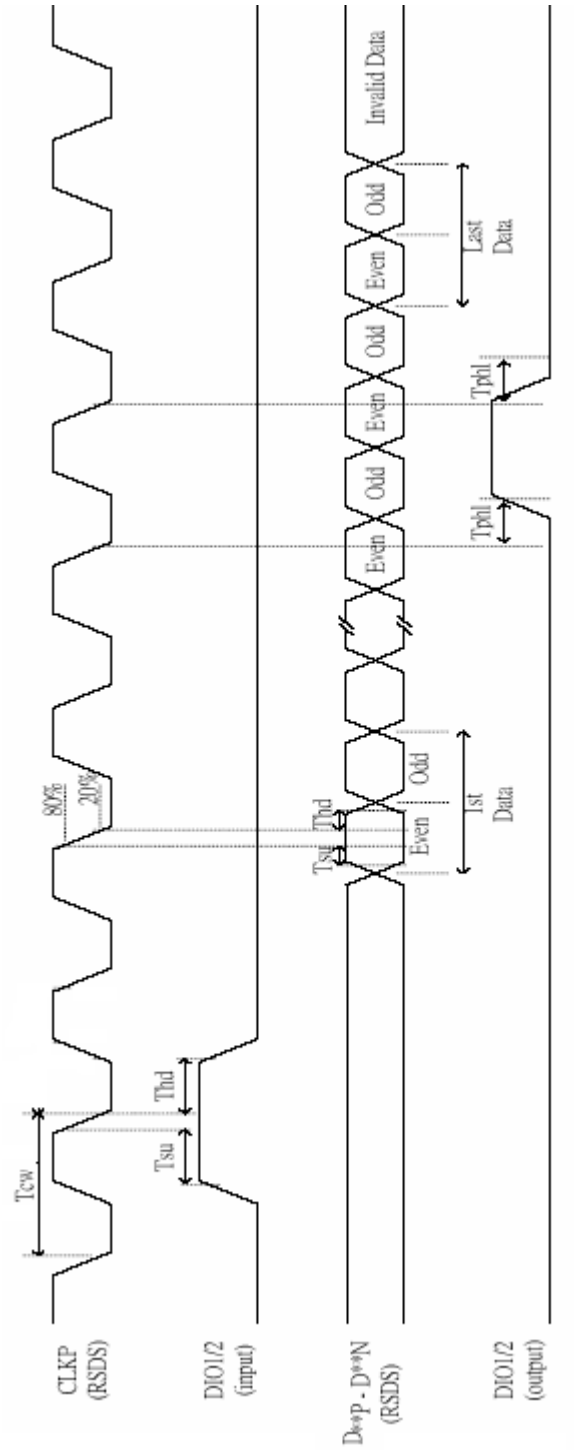


Figure 11-2 Horizontal timing-RSDS(2)

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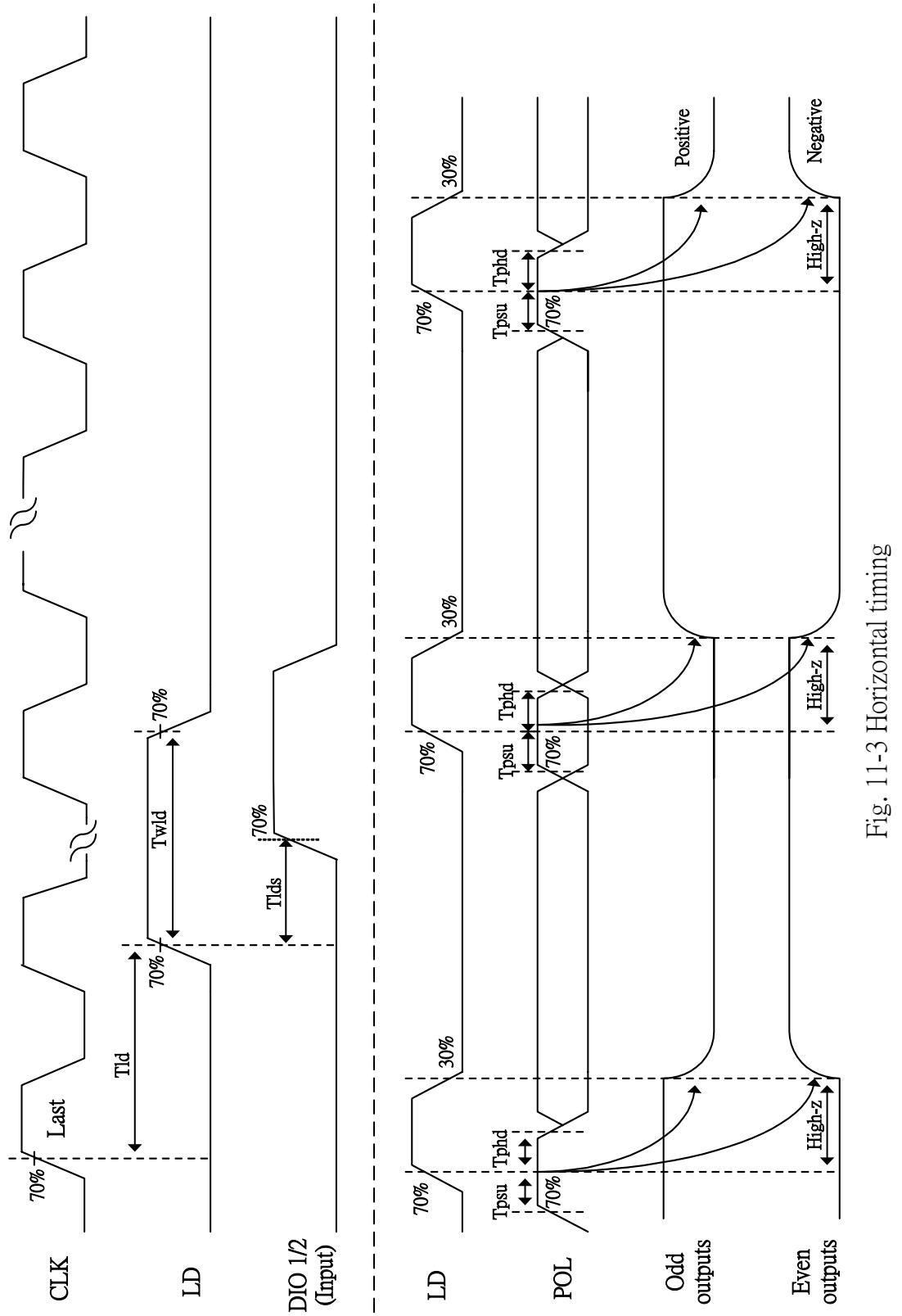


Fig. 11-3 Horizontal timing

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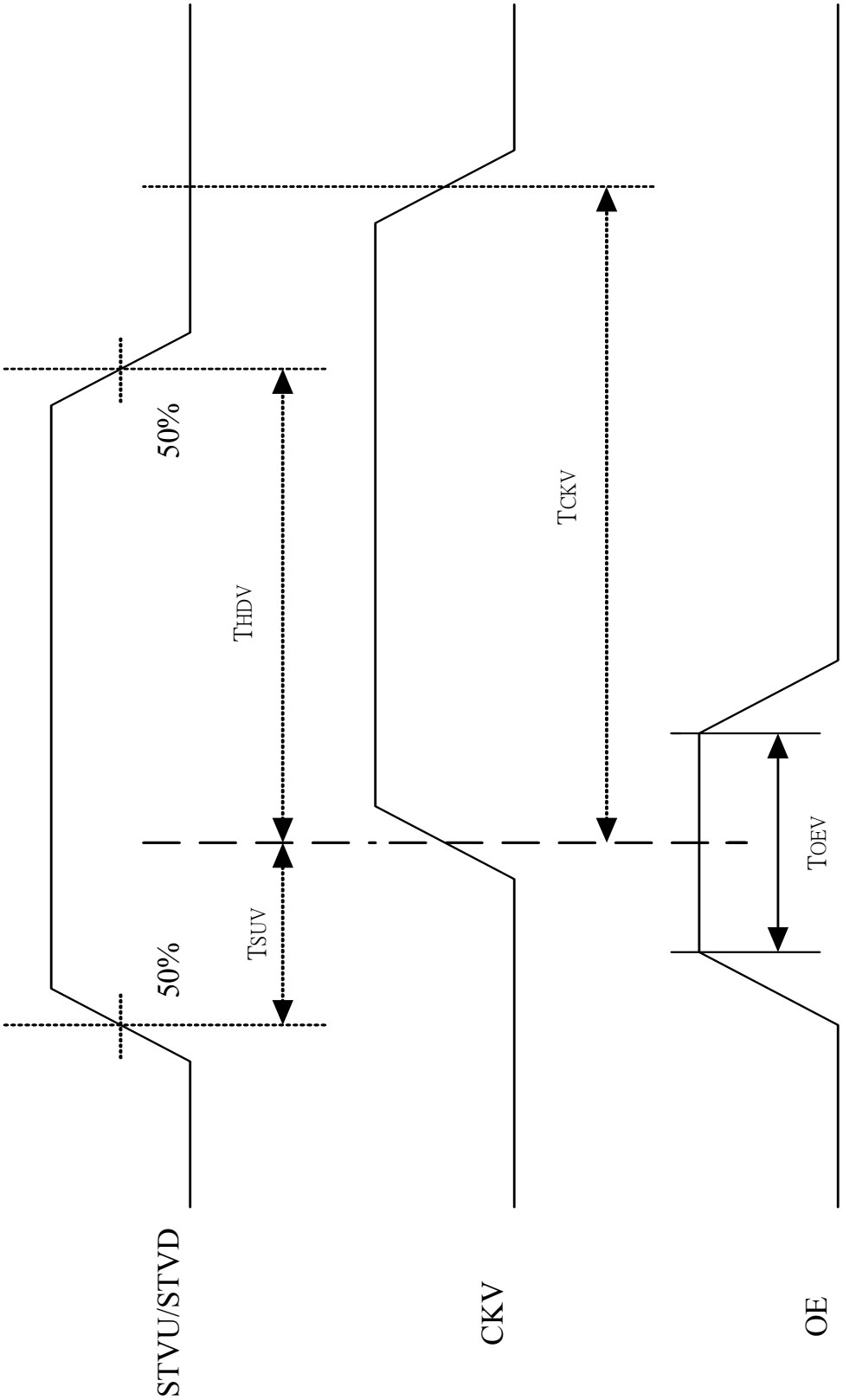


Fig. 11-4 Vertical shift clock timing

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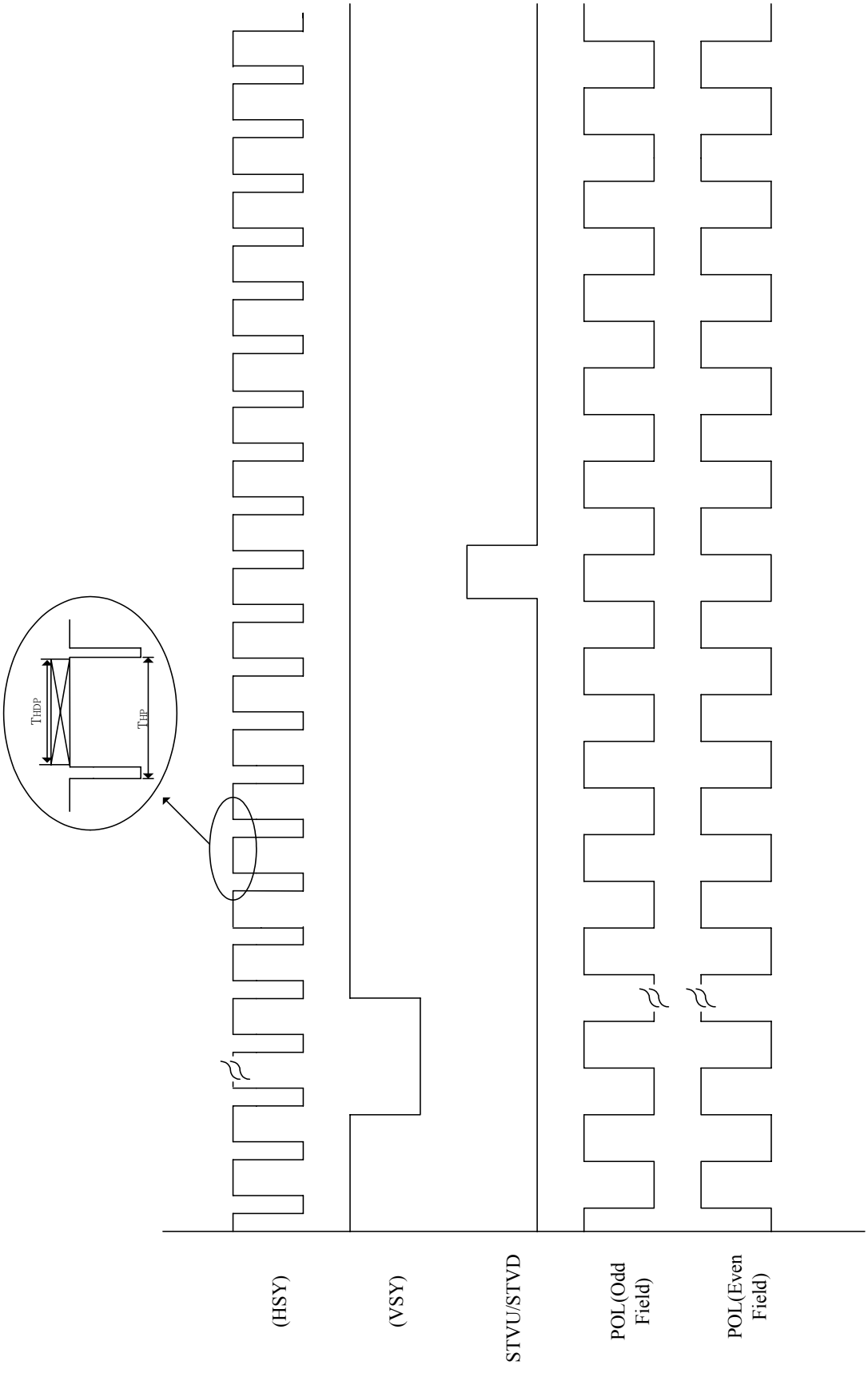
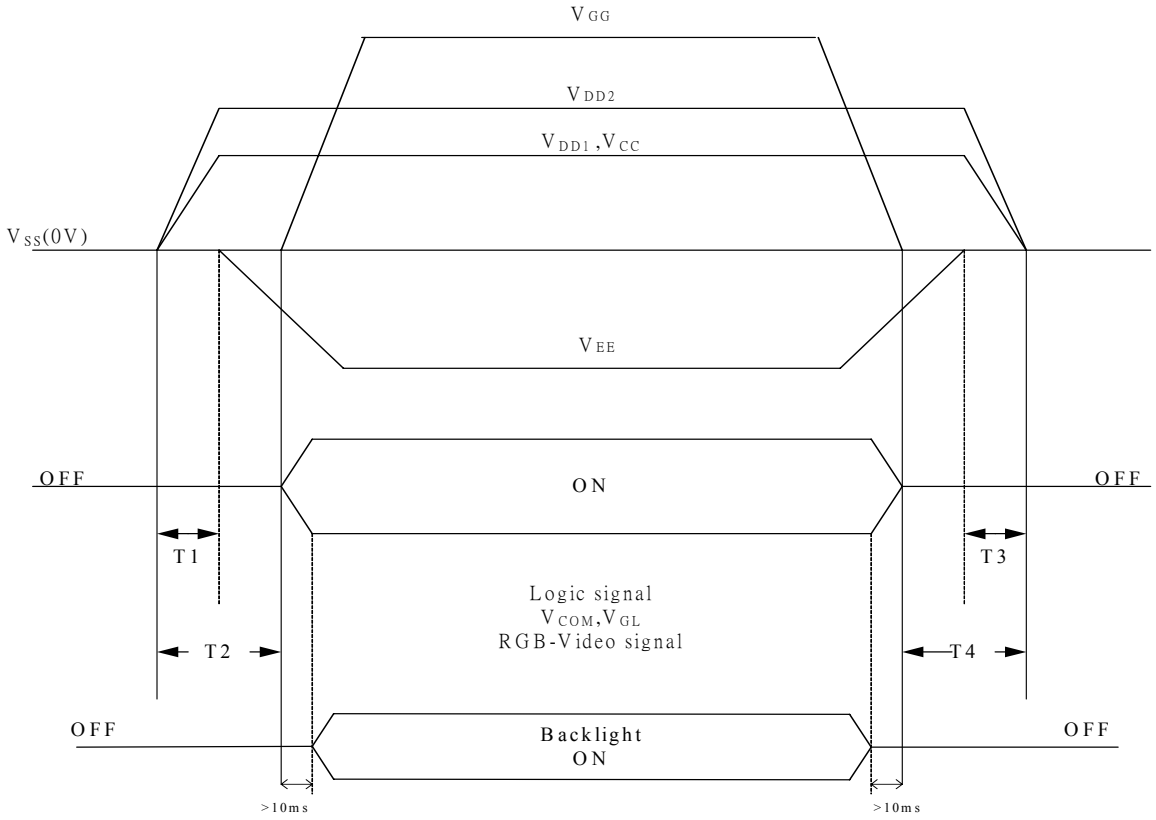


Fig. 11-5 Vertical timing

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12. Power On Sequence



1. 10ms≦T1＜T2
2. 0ms＜T3≦T4≦10ms

13. Optical Characteristics

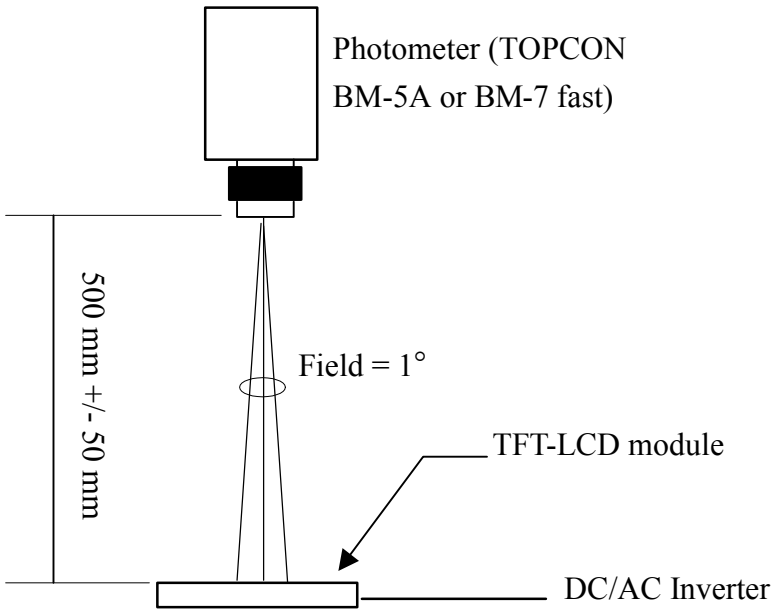
13-1) Specification:

Ta = 25℃

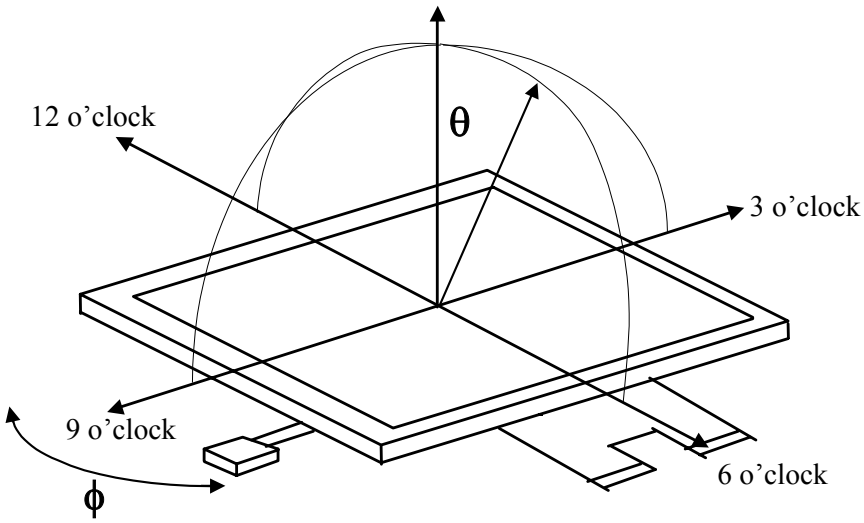
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR≥10	55	60	-	deg	Note 13-1
	Vertical	θ (to 12 'clock)		35	40	-	deg	
		θ (to 6 o'clock)		50	55	-	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	600	-	-	Note 13-2
Brightness		L	θ =0°/ φ =0	300	350	-	cd/㎡	Note 13-4
Response time	Rise	Tr	θ =0°/ φ =0°	-	15	30	ms	Note 13-3
	Fall	Tf		-	25	50	ms	
Cross Talk Ratio		CTK	-	-	-	3.5	%	Note 13-5
Luminance Uniformity		U	-	75	80	-	%	Note 13-6
White Chromaticity		x	θ =0°/ φ =0°	0.265	0.305	0.345	-	Note 13-4
		y		0.300	0.340	0.380	-	
LED Life Time			25℃	20000	30000	-	hrs	Note 13-7

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The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.



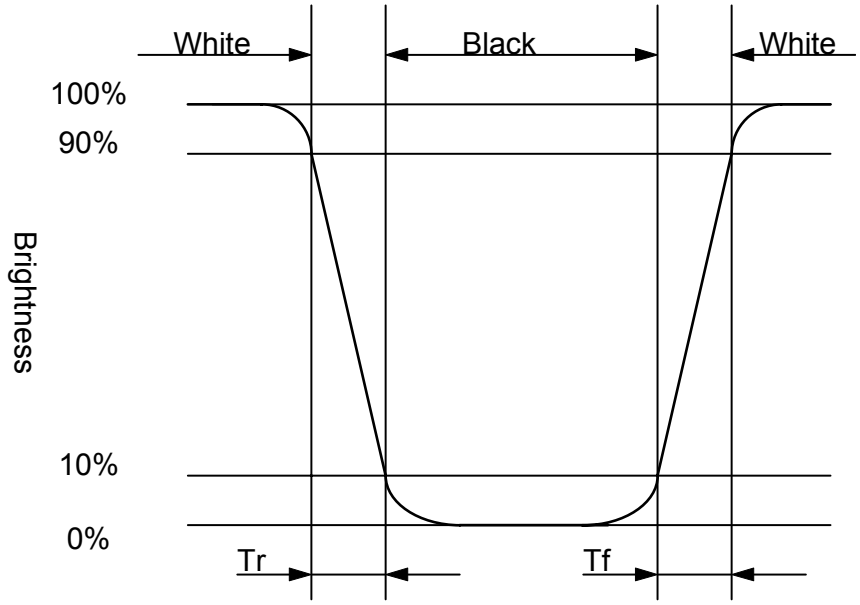
Note 13-1: The definition of viewing angles are as follow



Note 13-2 : The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

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Note 13-3: Definition of Response Time Tr and Tf:



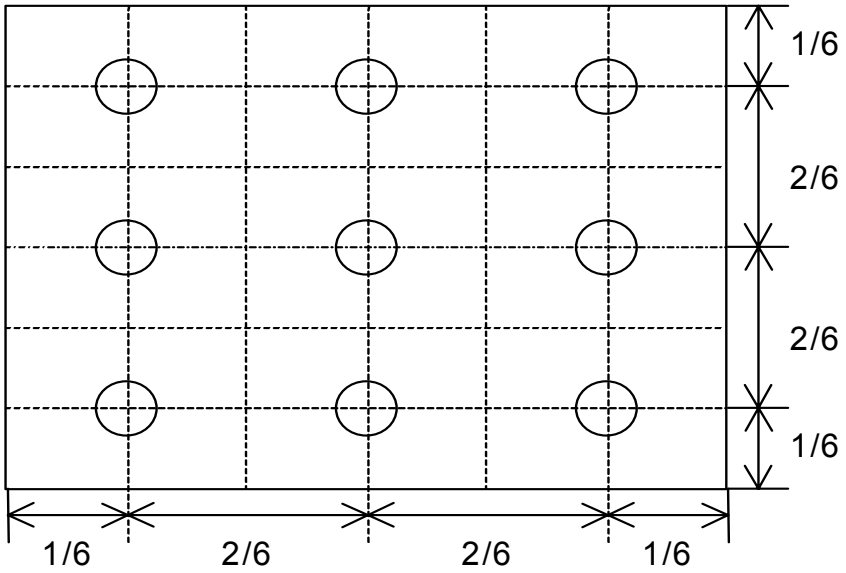
Note 13-4 : 1.Topcon BM-7(fast) luminance meter 1° field of view is used in the testing

Note 13-5 : The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter : BM-5A or BM-7 fast (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module

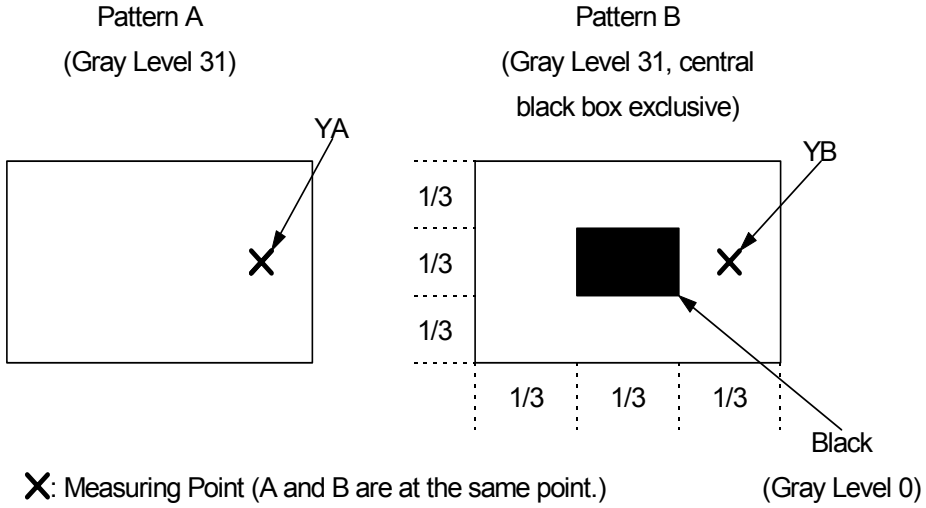
The test pattern is white (Gray Level 63).



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Note 13-5: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A
YB: Brightness of Pattern B
Luminance meter : BM 5A (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module



Note 13-7: The "LED Life time " is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25℃ and I_{LED} =320mA.

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14. Handling Cautions

14-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

c) Protective film (Laminator) is applied on surface to protect it against scratches and dir.

d) Please following the tear off direction as figure14-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

14-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the Specifications described may not be satisfied.

14-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

f) Please adjust the voltage of common electrode as material of attachment by 1 module.

14-5) Polarizer mark

The polarizer mark is to describe the direction of wide view angle film how to mach up with the rubbing direction.

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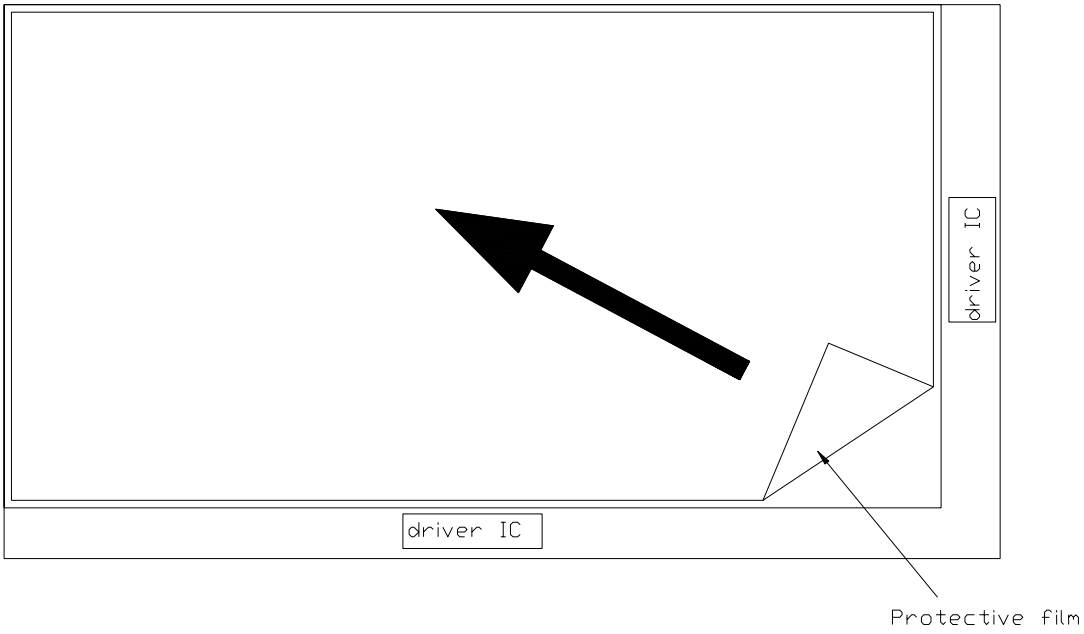


Figure 14-1 the way to peel off protective film

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15. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80℃, 240 hrs
2	Low Temperature Storage Test	Ta = -30℃, 240 hrs
3	High Temperature Operation Test	Ta = +80℃, 240 hrs
4	Low Temperature Operation Test	Ta = -20℃, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +50℃, 80%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	0℃→+60℃, 50 Cycles 1hr 1hr
7	Vibration Test (non-operating)	Frequency：10 ~ 57 $H_{Z,}$ Amplitude：0.5 mm 58~500Hz, 1G Sweep time: 11 min Test Period: 3 hrs (1 hr for each direction of X, Y, Z)
8	Shock Test (non-operating)	80G, 6ms, X,Y, Z 1 times for each direction
9	Electrostatic Discharge Test (non-operating)	200pF , 0Ω ±200V 1 time / each terminal

Ta: ambient temperature

Note: The protective film must be removed before temperature test

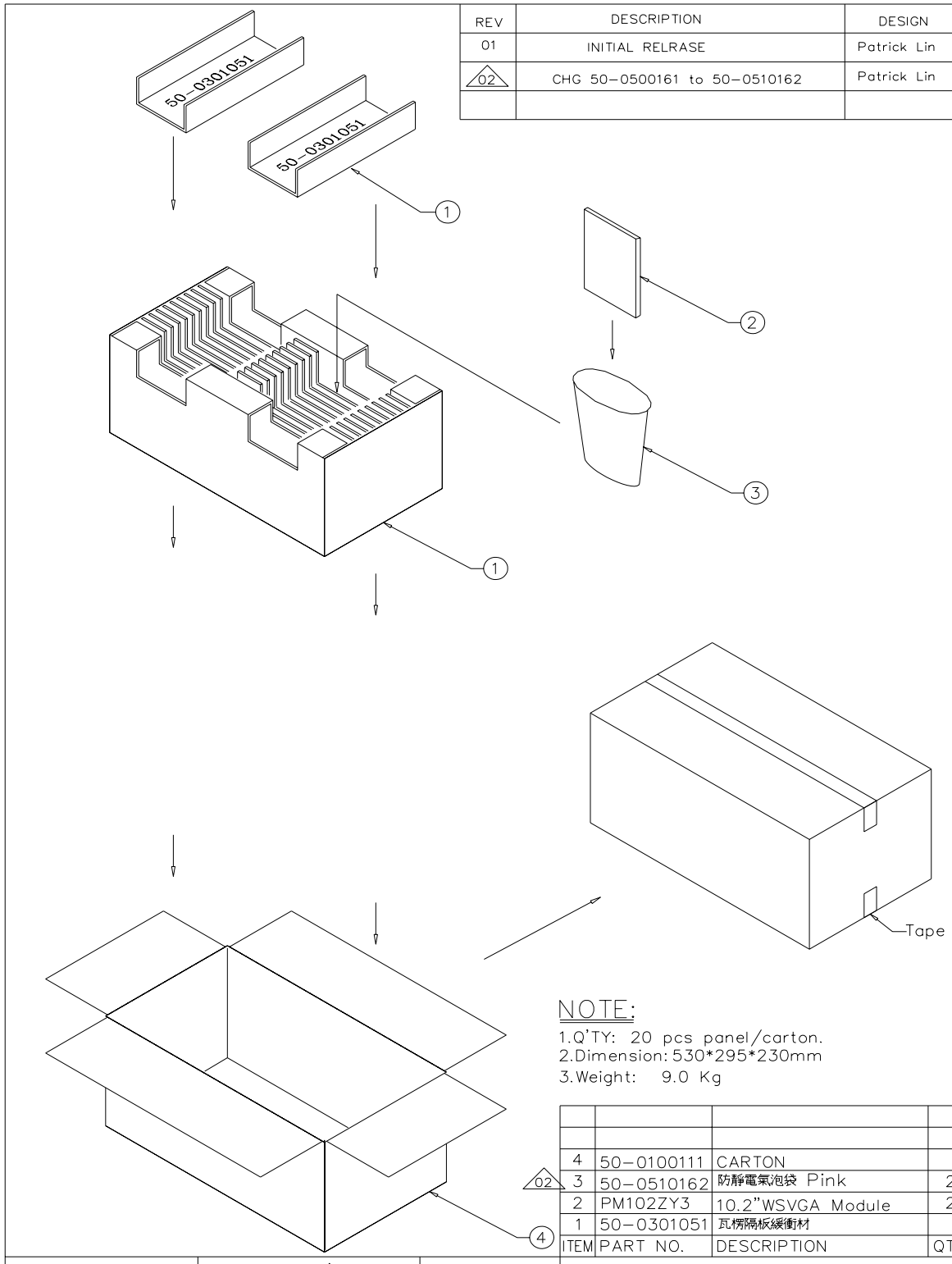
[Criteria]

In the standard conditions, there is not display function NG issue occurred. (Including: line defect , no image). All the cosmetic specification is judged before the reliability stress.

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16.Packing

REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELRASE	Patrick Lin	2007.10.26
02	CHG 50-0500161 to 50-0510162	Patrick Lin	2009.08.14



NOTE:
1.Q'TY: 20 pcs panel/carton.
2.Dimension: 530*295*230mm
3.Weight: 9.0 Kg

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
4	50-0100111	CARTON	1	
02 3	50-0510162	防靜電氣泡袋 Pink	20	抗靜電
2	PM102ZY3	10.2"WSVGA Module	20	
1	50-0301051	瓦楞隔板緩衝材	1	上蓋+ 底座

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	元太科技工業股份有限公司 Prime View International Co., Ltd.

			SCALE	UNIT	SHEET	DWG.TITLE
APPROVE	Frank Shin	'07.10.26			1 OF 1	PM102ZY3 Packing Draw
CHECK	Frank Shin	'07.10.26				
DRAWN	Patrick	'07.10.26	MTL.NO.		DWG FILE:	REV. 01 / A4 SIZE

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