Product Profile

MB87M2141 *SmartMPEG™*

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MPEG-2 Decoder for Set-Top-Boxes

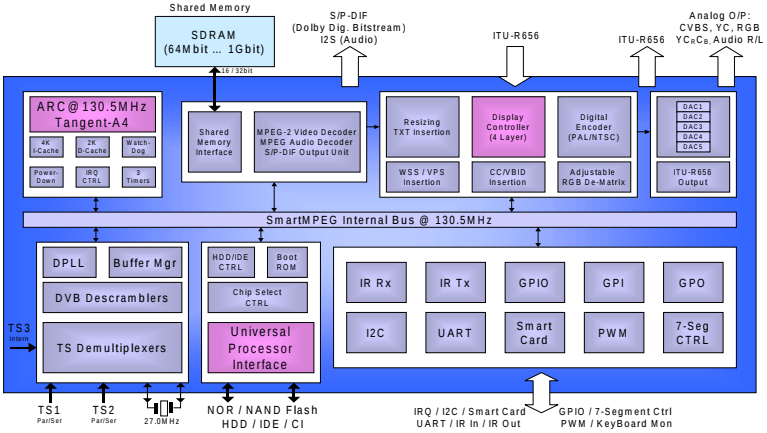
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INTRODUCTION:

The *SmartMPEG™* is an integrated set-top-box decoder. As a major component of a digital video broadcast (DVB) set-top-box or IDTV this device uses Fujitsu's industry-leading Cx81 CMOS technology (0.18µm).
It incorporates an ARC Tangent A4 RISC core (@130MHz), two transport stream demultiplexers with integrated DVB descramblers, a PAL/NTSC digital video encoder and a display controller, which overlays up to four layers of OSD. This set-top-box decoder consists of a shared memory interface for CPU and for MPEG decoding. The universal processor interface allows connection to FLASH, hard disk drives and other asynchronous devices. The minimum SDRAM required is one 64Mbit device using 16bit data bus.
The *SmartMPEG™* is the 3rd generation of Fujitsu's MPEG decoder, the successor to the MB87L2250. With the MB87L2250, Fujitsu offered a set-top-box chip, which enabled very low end product cost. Its successor, the *SmartMPEG™* incorporates all the features which are required for standard set-top-boxes. This high level of integration makes it ideally suited for todays interactive set-top-box applications.
Furthermore the Fujitsu Application Programming Interface (FAPI) ensures a short time-to-market by making the software development easier. The FAPI is the programming interface for Fujitsu DVB components as well as easing migration to future devices.

FEATURES

- MPEG2 video ISO/IEC 13818-2 (MP@ML...SP@ML)
- MPEG audio layer 1/2
- 32-bit RISC CPU (ARC Tangent A4 @130MHz)
- 4K I-cache / 2K D-cache
- Three timers / watchdog / power-down mode
- Shared memory interface (SDRAM, 16/32 bit data), 64Mbit...1Gbit
- Universal processor interface (IDE, NAND/NOR FLASH & Common Interface)
- Two transport stream decoders (decoding/recording) including DVB descrambler
- Flexible MPEG video resizing (factor 1/16 to 2)
- Display controller with up to four true colour graphic or CLUT layers
- Teletext / WSS / CC / VBID insertion
- PAL/NTSC digital encoder
- RGB De-matrix (RGB or YCrCb output)
- Control of brightness, contrast and colour saturation of RGB and YCrCb output
- 5 video DAC's @ 10bit
- ITU-R 656 video input/output (shared with TS2 input)
- S/P DIF output for PCM/AC3/MPEG
- UART / Smart Card IF / I2C / GPIO
- 7-segment LED controller for 4 digits
- Infra Red receiver / transmitter
- PWM Output
- On-chip DPLL, requiring only 27.0MHz crystal
- Bootable from NOR Flash or I2C
- FPT-208P-M06 (LQFP-Package)
- Ambient Temperature Range (Std Pkg): 0^{o}C to $+70^{o}$C
- Advanced Technology: Fujitsu CMOS Cx81 (0.18µm)
- 1.8 volt device with 3.3 volt I/O
- Power consumption: typ. 800mW



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