HIP0063

PRELIMINARY

October 1995

Hex Low Side MOSFET Driver with Serial or Parallel Interface and Diagnostic Fault Control

Features

- **Six Channel MOSFET Driver with Gate Drive Control by Serial (SPI) or Parallel Interface and an Option for PWM Logic Switching Control**
- **Drain Monitor Provides Fault Detection and Voltage Clamp for Each Channel**
- **Output Voltage Zener Clamp. . . . . 67V Typ**
- **5V CMOS Logic Level Input Control**
- **V_{CC} Logic Level Power Supply**
  - **5V V_{CC} Logic Power Supply**
  - **Turns Off Gate Drive for Low or Loss of V_{CC}**
- **V_{PWR} System Level Power Supply Management**
  - **5.5V to 17V Battery/System Level Power Supply Monitor**
  - **Over-Voltage Shutdown. . . . . 35V Typ**
- **Output Supply/Load Short and Open Load/Ground Short Fault Detection**
- **Automatic Change to Low Duty Cycle Drive Mode When Output Short-to-Supply Detected**
- **Fault Diagnostic Feedback via the SPI Bus**
- **Operating Temp Range . . . . . -40°C to +125°C**

Applications

- **Automotive and Industrial Systems**
- **Control of Solenoids, Relays and Lamp Drivers**
- **Interface to Logic and μP Controllers**
- **Robotic System Controller**

Description

The HIP0063 is a logic controlled, six channel Low Side Power Driver. As shown in the Block Diagram, the outputs are controlled via the serial data interface or, by user option, each output may be independently controlled from the respective parallel input. In addition, PWM logic switching control (HLOS) may be directly applied to channels 0 and 1 in parallel, or channels 4 and 5 in parallel.

Output fault conditions may be detected as an output load short to supply when the output is ON or as an open load/ground short when the output is OFF. If an over-current short exists at one output, gate drive goes to a low duty cycle mode. It will remain in the low duty cycle mode until switched off or the fault is cleared. Fault bits are sent to a fault register to indicate which channel is at fault. The fault bits are indicated by a logic one and is internally latched when $\overline{CS}$ goes low. A fault bit will return to zero when the fault disappears. Either an 8-bit or 16-bit SPI communication mode may be used. Refer to the application section for bit control information.

Over-voltage shutdown protection for all outputs will occur when V_{PWR} (Battery/MOSFET Supply) exceeds 35V typical. When V_{CC} is less than 3.5V, gate drive is switched off. The input and gate control logic is fully function when the V_{CC} supply is greater than 4V typical. The HIP0063 has an internal drain-to-gate zener which is used to voltage clamp the output drain-to-source voltage of the MOSFET.

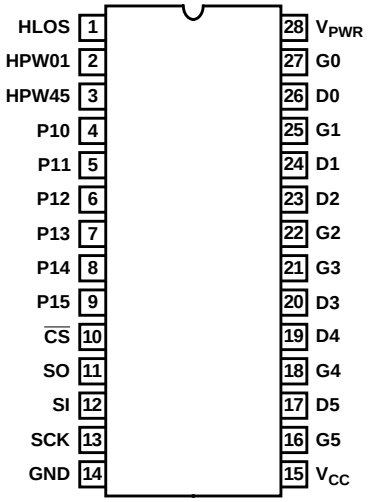
The HIP0063 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly well suited for MOSFET control in circuits driving lamps, displays, relays, and solenoids in applications requiring low operating power.

Ordering Information

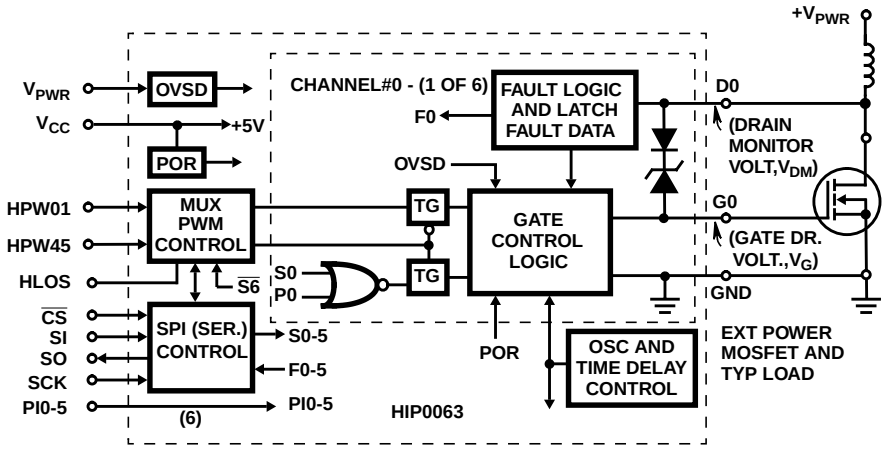
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP0063AB	-40°C to +125°C	28 Lead Plastic SOIC (W)

Pinout

HIP0063 SOIC
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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File Number **4009**

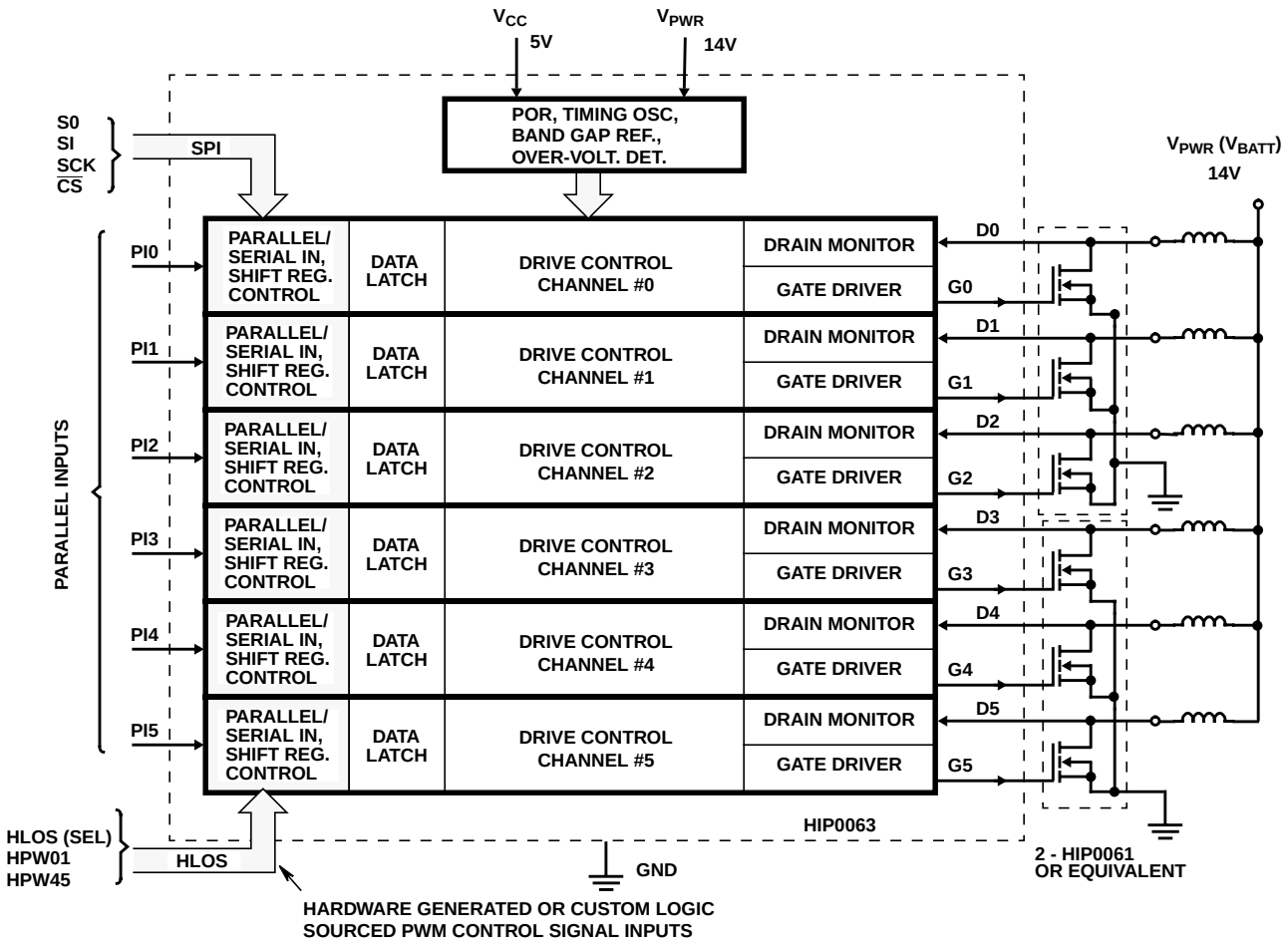


FIGURE 1. TYPICAL APPLICATION CIRCUIT FOR THE HIP0063 SHOWING HOW THE GATE DRIVE OUTPUT AND DRAIN MONITOR INPUT CONTROLS TWO HIP0061 THREE FET ARRAYS

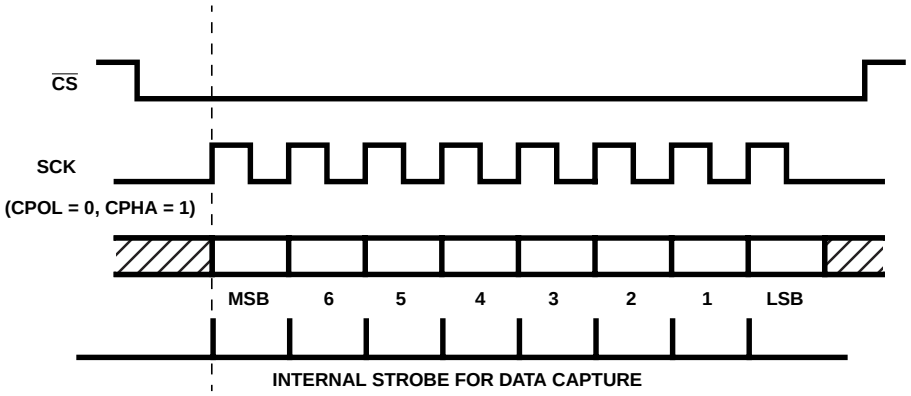


FIGURE 2. SPI DATA AND CLOCK TIMING DIAGRAM. SERIAL COMMUNICATION IS INITIATED WHEN $\overline{CS}$ GOES LOW AND SCK IS LOW. 8 OR 16 BITS OF DATA IS CLOCKED INTO SI ON THE LEADING EDGE OF SCK. DATA IS CLOCKED OUT OF SO ON THE TRAIL EDGE OF SCK. WHEN $\overline{CS}$ GOES HIGH, DATA IS LATCHED TO CONTROL EACH CHANNEL

Absolute Maximum Ratings

Logic Supply Voltage, V_{CC} . . . . . -0.3V to 7V
Max Quiescent Logic Supply Current, I_{CC} 5mA
Logic Input Voltage . . . . . -0.3V to V_{CC} + 0.3V
System Supply Voltage Monitor, V_{PWR} (Note 1)
Max Continuous . . . . . -1.5V to 38V
Max Drain Clamp Voltage, V_{DM} (Note 2) 75V
Max Gate Drive Output Voltage, V_G (Note 3) . . . . -0.3 to V_{CC} + 0.3V
Operating Ambient Temperature Range, T_A . . . . -40°C to +125°C
Operating Junction Temperature Range . . . . . -40°C to +150°C
Storage Temperature Range, T_{STG} . . . . . -55°C to +150°C
Lead Temperature (Soldering 10s Max) . . . . . +265°C

Thermal Information (Typical)

Thermal Resistance	θ_{JA}
28 Lead SOIC Package	75°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{CC} = 4.5V to 5.5V, V_{PWR} = 5.5V to 17V, T_A = -40°C to +125°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Logic Supply Quiescent Current	I_{CC}		-	-	5	mA
V_{CC} Threshold for POR Reset	V_{POR}	PI0-5 High (ON), Increase V_{CC}, Measure V_{CC} Threshold When Gate Drive Goes High	3.5	4	4.25	V
POR Hysteresis	V_{POR_HYS}	PI0-5 High, Decrease V_{CC}, Measure V_{CC} Threshold when Gate Drive goes Low, Hysteresis Equals Differential V_{CC} Voltage for Gate Drive High to Gate Drive Low	-	500	-	mV
Undervoltage Lockout, Low V_{CC}	V_{CC}	V_{PWR} = 14V	1	2	3.7	V
Battery Supply Monitor Current	I_{PWR}	V_{PWR} = 14V	-	-	150	µA
V_{PWR} Over-Voltage Shutdown Threshold	V_{PWR_OVTH}	V_{PWR} Threshold Measured When Gate Drive Voltage, V_G Goes Low	30	35	40	V
V_{PWR} Over-Voltage Shutdown Hysteresis	V_{PWR_OVHYS}		-	1	-	V
LOGIC INPUTS						
Input High Voltage; SI, SCK, $\overline{CS}$	V_{IH}		0.7V_{CC}	-	-	V
Input Low Voltage; SI, SCK, $\overline{CS}$	V_{IL}		-	-	0.3V_{CC}	V
Input Leakage Current; SI, SCK	I_{LK}		-10	0	10	µA
Input Pulldown Currents; PI0-5, HPW01, HPW45	I_{IN_PD}	0.3V_{CC} < V_{IN} < V_{CC}	3	10	25	µA
Input Pullup Currents; $\overline{CS}$, HLOS	I_{IN_PU}	GND < V_{IN} < 0.7 V_{CC}	-25	-10	-2	µA
Threshold Voltage at Falling Edge, PI0-5, HLOS, HPW01, HPW45	V_T-		1.5	2.2	3.0	V
Threshold Voltge at Rising Edge, PI0-5, HLOS, HPW01, HPW45	V_T+		1.8	2.6	3.4	V
Input Hysteresis Voltage; PI0-5, HLOS, HPW01, HPW45	V_{IN_HYS}		250	500	650	mV
Input Capacitance, SCK, SI	C_{IN}	0 < V_{IN} < V_{CC}	-	7	12	pF
DATA OUTPUT						
SO Data Output High Voltage	V_{OH}	I_O = 5mA Source Current	0.8V_{CC}	-	-	V
SO Data Output Low Voltage	V_{OL}	I_O = 5mA Sink Current	-	0.2	0.4	V
SO Three-State Leakage Current	I_{SOT}	V_{CC} = 0V to 5.5V	-10	1	10	µA
SO Three-State Capacitance	C_{SOT}	0 < V_{IN} < V_{CC}	-	15	20	pF

Electrical Specifications V_{CC} = 4.5V to 5.5V, V_{PWR} = 5.5V to 17V, T_A = -40°C to +125°C, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVE OUTPUT						
Gate Drive Output Source Current	I_{GOH}	V_G = 0V	-4.4	-	-0.5	mA
Gate Drive Output Sink Current	I_{GOL}	V_G = 4.5V	0.2	-	3.3	mA
Gate Drive Rise Time with Load	t_R	Cap. Load, Gate to GND = (TBD)pF	TBD	TBD	-	µs
Output Turn-ON Delay, Rising Edge of $\overline{CS}$ to 10% of V_G Turn-ON	t_{PHL}		-	5	10	µs
Output Turn-OFF Delay, Rising Edge of $\overline{CS}$ to 10% of V_G Turn-OFF	t_{PLH}		-	5	10	µs
DRAIN MONITOR INPUT AND PROTECTION						
D0-5 Drain Monitor Clamp Voltage	V_{DM}	D0-5 Clamp Current, I_{DM} = 2mA; t_{PW} =100µs, Duty Cycle <1%, Gate Drive Voltage, V_G Low (Note 2)	58	64	74	V
D0-5 Drain Monitor Pulldown Current Sink	I_{DM}	$0.3V_{CC} < V_{DM} < V_{CC}$	3	10	25	µA
Fault Threshold Voltage Sensed at the Drain Monitor Input, Shorts/Opens	V_{DM_FTH}		$0.3V_{CC}$	$0.4V_{CC}$	$0.5V_{CC}$	V
Short Circuit Sense Fault Time $V_{DM} > V_{DM_FTH}$, Gate ON/High	t_{SC_ON}	T_A = -40°C to 25°C	18	28	39	µs
		T_A = 25°C to 150°C	19	28	36	µs
Over-Current Refresh Time During Short Circuit (Gate Drive OFF)	t_{SC_REF}	T_A = -40°C to 25°C	11.4	16.4	21.4	ms
		T_A = 25°C to 150°C	12.0	16.4	19.6	ms
Over-Current ON Time Duty Cycle		Duty Cycle = $t_{SC}/(t_{SC} + t_{REF})$	0.31	0.34	0.37	%
Open-Load "OFF" Sense Time $V_{DM} < V_{DM_FTH}$, Gate OFF/Low	t_{OL_OFF}		18	28	39	µs

NOTE:

1. Refer the Figure 3 recommended application circuit for V_{PWR} protection given system power supply conditions of +24V for double battery voltage, -14V for reverse battery voltage and +80V system level load dump voltages.
2. V_{DM} refers to the specified Drain Monitor voltage input at pins D0 thru D5, that monitor the drain status from the respective external MOSFET.
3. V_G refers to the specified Gate Drive voltage at the output pins, G0 thru G5, that drive the Gate of the respective external MOSFET.

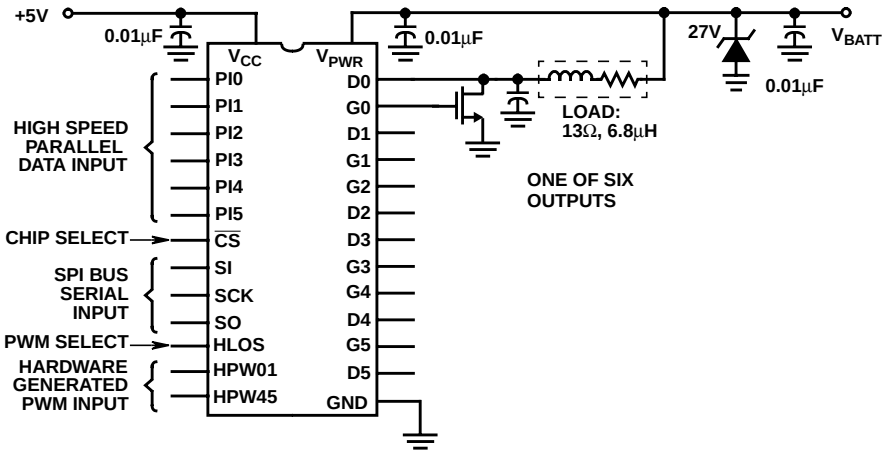


FIGURE 3. TYPICAL APPLICATION CIRCUIT FOR THE HIP0063 SHOWING THE V_{PWR} SUPPLY INTERFACE WITH CIRCUIT PROTECTION COMPONENTS. FOR THE VALUES SHOWN, GIVEN A LOAD DUMP OF 80V THAT DECAYS TO THE V_{PWR} LEVEL IN 350ms, THE 27V ZENER DIODE IS REQUIRED TO CLAMP THE TRANSIENT TO 60V MAXIMUM. FOR THE REVERSE BATTERY PROTECTION, THE ZENER DIODE CLAMPS NEGATIVE VOLTAGES

Serial Peripheral Interface Timing (See Figure 4)

PARAMETERS	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Clock Operating Frequency	f_{SCK}	C_L = 200pF	1.8	4	-	MHz
Clock Period	t_{SCK}	SCK = 0.8V to 0.8V	-	250	555	ns
Clock High Time	t_{WH}	SCK = 2V TO 2V; f_{SCK} = 1.8MHz	-	100	248	ns
Clock Low Time	t_{WL}	SCK = 0.8V TO 0.8V; f_{SCK} = 1.8MHz	-	100	248	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCK	t_{LEAD}	$\overline{CS}$ = 0.8V to SCK = 2V	-	150	200	ns
Falling Edge of SCK to Rising Edge of $\overline{CS}$	t_{LAG}	SCK = 0.8V to $\overline{CS}$ = 2V	-	50	200	ns
SI to SCK Setup Time	t_{SU2}	SI = 0.8, 2V to SCK = 2V; f_{SCK} = 2.25MHz	-	25	55	ns
SI Hold After SCK Rise	t_{H2}	SCK = 2V to SI Hold	-	10	55	ns
Rise Time of Incoming Signals	t_{rSI}	C_L = 200pF	-	-	120	ns
Fall Time of Incoming Signals	t_{fSI}	C_L = 200pF	-	-	120	ns
SO Data Valid to Falling Edge of SCK	t_{SU1}	SO = 0.8, 2V to SCK = 0.8V; C_L = 200pF	80	-	-	ns
Falling Edge of SCK to SO	t_{H1}	SO = 0.8, 2V to SCK = 0.8V; C_L = 200pF	80	125	-	ns
Rise Time of SO	t_{rSO}	C_L = 200pF	-	30	50	ns
Fall Time of SO	t_{fSO}	C_L = 200pF	-	30	50	ns
Falling Edge of $\overline{CS}$ to SO Operational (1kΩ Pulldown on SO Pin)	t_{SOEN}	$\overline{CS}$ = 0.8V to SO Low Impedance	-	150	300	ns
Rising Edge of $\overline{CS}$ to SO Three-State (1kΩ Pulldown on SO Pin)	t_{SODIS}	$\overline{CS}$ = 2V to SO Three-State	-	150	200	ns
Rising Edge of SCK to SO (Data Valid)	t_{VALID}	C_L = 200pF, 1.8MHz	-	-	172	ns
		C_L = 200pF, 2.25MHz	-	-	117	ns

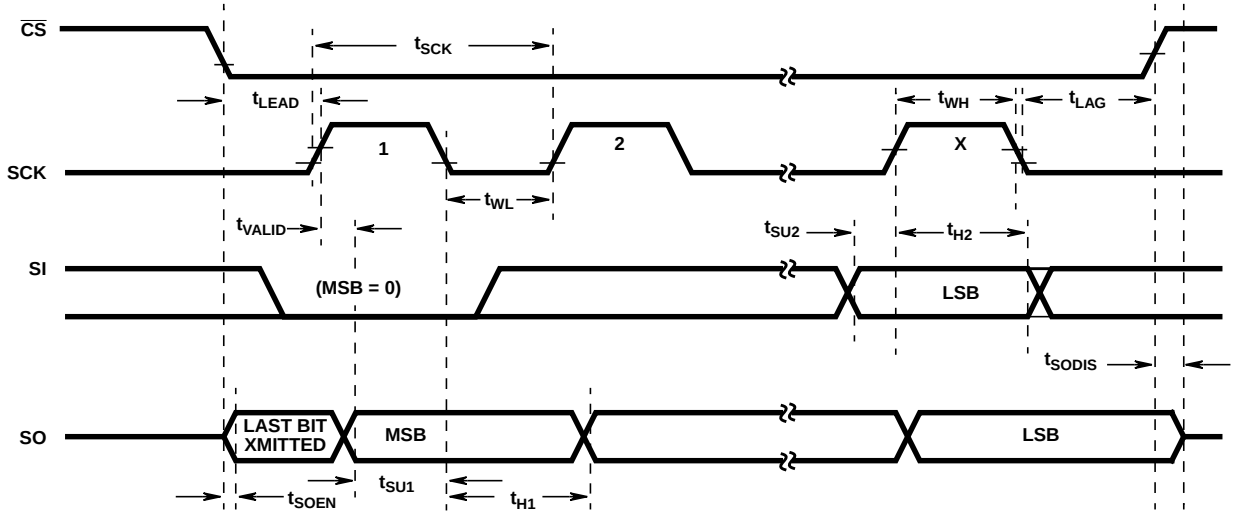


FIGURE 4. TIMING DIAGRAM FOR THE HIP0063 SHOWING THE SPI BUS INPUT CONTROL SIGNALS

Applications

Input Control

The application circuit for the HIP0063 is shown in Figure 1 while details of input control are shown in the block diagram. Gate control and diagnostic fault management are provided for each of six channels. Gate controlled switching is OR'd by the SPI Bus microcontroller interface or the independent parallel logic inputs (PI0-1) as a user option. The six control channels provide gate drive (G0-5) for the MOS output drivers while detecting fault conditions at each output via the drain monitor pins (D0-5). An HLOS input control overrides the serial input and modifies the parallel operation.

SI (serial input) data from a SPI controller is clocked into the input register on the positive leading edge of the clock pulse, SCK while $\overline{CS}$ is low. (Data is clocked from the SO output on the trailing edge of the SCK clock pulse.) Either 8-bit or 16-bit control may be used. The input data is clocked MSB first and all unused bits should be low. Detailed information on the bit structure for both 8-bit and 16-bit operation is shown in Table 1.

A special feature of the HIP0063 is a PWM mode of operation set by a high on the HLOS pin. This mode is primarily used to control fuel injectors and allows direct access to control channels 0 and 1 from the HPW01 Pin and channels 4 and 5 from the HPW45 Pin. When HLOS is high, the serial input is disabled and SO goes to three-state. Channel#2 and Channel#3 are independently controlled from the parallel input during the HLOS/PWM operation. A pullup is needed on the SO pin to keep the SO output high when HLOS/PWM is active.

Fault Protection

Output fault conditions are monitored at the Drain Monitor pin, DO. Feed back of the fault condition is returned by the SPI SO data output when new data is clocked by SCK into the SI data input.

Output Load Short conditions are detected at the drain monitor pin when the Output is ON and the drain voltage is greater than the specified V_{DM_FTH} voltage threshold for a time greater than t_{SC_ON}. When the output load short is detected, the output goes to a low duty cycle mode. The duty cycle is a ratio of the ON time required to sense and enter the low duty cycle mode (t_{SC_ON}) and the following refresh OFF time, t_{SC_REF}.

Open Load fault conditions are detected when the Output is OFF and the drain voltage falls below the V_{DM_FTH} threshold level for a time greater than t_{OL_OFF}. If the Output is ON, Open Load faults will not be detected.

For Load Short and Open Load fault conditions, a fault bit with a logic state of "1" is placed in the respective fault register. If the fault is terminated, the bit returns to "0". When $\overline{CS}$ goes low for serial communication, all fault bits are latched. Fault data is read at SO when $\overline{CS}$ is low and SCK is clocked. When $\overline{CS}$ goes high, new data may enter the fault register.

The V_{PWR} pin monitors the supply voltage (battery supply) for over-voltage fault conditions. Over-voltage protection shuts down all output drivers when the over-voltage threshold of typically 35V is detected at the V_{PWR} pin. If the V_{CC} supply is low or off, V_{PWR} supplies the necessary bias to switch off all output gates.

Each output of the HIP0063 has a drain-to-gate zener diode clamp to limit peak voltage at the drain of the output drivers. The voltage pulse from switched inductive loads is clamped when the drain-to-gate zener forces the output driver into conduction. The MOSFET drain-to-source output clamp voltage level is typically 67V.

Diagnostic Feedback

Normal operation in the SPI mode calls for bits 0 thru 5 to be sent as a "1" to control turn-on. Bit 6 is always low (reserved for use as a test bit) and bit 7 should be low to provide a flag for HLOS/PWM operation. When there is no fault condition, the return bits from SO will be the same as the bits sent. Fault conditions return the XOR complement. When the complement is received, it may also indicate an error in communication or HLOS/PWM controlled operation has occurred. A CPU instruction to send the last command will verify HLOS action. After the HLOS action is terminated, resending the previous command will verify normal opera-

TABLE 1. SPI DATA FORMAT - BIT DEFINITION FOR DATA INPUT AND OUTPUT

8-BIT MODE:

7	6	5	4	3	2	1	0
MSB							LSB

Bits 0 to 5:	Turns-ON the corresponding output gate when set HIGH.
Bit 6:	Not used, set LOW (Reserved as a test bit).
Bit 7:	Bit 7 can be used as an HLOS flag. Always set LOW. If the complement is returned, then HLOS is active. (i.e., HLOS forces SO into a three-state mode and a HIGH will be returned).
Note:	Fault Bits clocked out when data clocked in.

16-BIT MODE:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB															LSB

Bits 0 to 5:	Turn-ON the corresponding channel output gate when set HIGH and will always be returned as sent.
Bit 6:	Not used, set LOW. (Reserved as a test bit).
Bit 7:	Not used, (Will be returned as sent).
Bits 8 to 13:	Fault bits for outputs 0 to 5 respectively. Returned as sent or returned as the complement to indicate an output fault.
Bit 14:	Not used, (Will be returned as sent).
Bit 15:	HLOS bit, (See bit 7 for the 8-bit mode).

tion. If there is still a problem in verifying the data sent, a communication error and further diagnosis is required. If the 16-bit mode is used, the data sent in the first byte should be the same as the data received in the second byte.

Pin Descriptions

V_{CC} - Logic Level Power Supply Pin

The V_{CC} pin is the primary power supply input to the IC with a +5V logic level voltage. The normal operating voltage range is 4.5V to 5.5V. At turn-on and when V_{CC} is less than the POR Threshold, the POR forces a reset which turns-off the Gate Drive outputs.

V_{PWR} - Battery Voltage Level Power Supply Monitor Pin

All MOSFETs are normally controlled by the HIP0063 and are separately biased by a Battery or System level power supply. The V_{PWR} pin monitors the Battery/System Power Supply and forces over-voltage shutdown under excessive high voltage conditions by forcing all Gate Drive outputs low. The V_{PWR} input also supplies the necessary bias under low V_{CC} reset conditions to switch off the Gate Drive output.

GND Pin

The GND (Ground) pin is the 5V logic supply ground for the IC and is a common ground for all functions on the chip.

SCK SPI Clock Pin

SCK is the bit shift clock input of the SPI interface and is connected to the SCK pin of the master device. Available control bits are clocked into the SI serial data input on the rising edge of the SCK pulse. SCK is low when $\overline{CS}$ goes active low. Each rising edge transition shifts in 1 bit of data. The SCK clock pulse has a 50% duty cycle and a CMOS logic level. The negative edge transition of SCK shifts available data out of the SO data output pin.

SI Serial Data In Pin

SI is the Serial Data Input pin of the SPI interface and receives command data from the master device on the rising edge of SCK when $\overline{CS}$ is low. Six Gate Drive control bits and the HLOS monitor bit are contained in the serial data byte at the SI input. The SI data input is an 8-bit or 16-bit control byte sent MSB first. (Refer to Table 1 for bit information.) Outputs are switched on with “1” state. Unused bits, including the HLOS bit, are set to the “0” state. This is a CMOS logic level input with an internal active pulldown.

SO Serial Data Out Pin

SO is the Serial Data Output pin of the SPI interface and transmits control status and fault data to the master device. The SO Serial Data Output is switched to an active state while $\overline{CS}$ is low and three-states when $\overline{CS}$ is high or HLOS is active. Otherwise, this is a CMOS logic level output with available data shifted out at SO on the negative edge of the SCK clock pulse. The normal SO output data is the same as the SI input data and is returned MSB first. If any of the channels are returning fault bits, the respective bit will be returned as a complement. If the HLOS control mode is active, the HLOS bit is returned as a complement. (Refer to Table 1 for bit information. Refer to the Input Control section of Applications for further details on transfer of control with HLOS/PWM switching).

$\overline{CS}$ Chip Select (Enable) Pin for the SPI interface

The $\overline{CS}$ Chip Select is an active low input pin. SPI bus communication with the master device becomes active when $\overline{CS}$ is switched low. When $\overline{CS}$ is active low, data may then be shifted into SI and out of SO with each SCK clock pulse. When $\overline{CS}$ goes high, the SO output switches to three-state and SPI communication is terminated. When $\overline{CS}$ goes active low, fault bits in the internal fault register are latched (with no further change during data transmission). When $\overline{CS}$ goes high, the fault status register is then open to new fault information. The $\overline{CS}$ input is a CMOS logic level output with an internal active pullup.

PI0 Thru PI5 Parallel Inputs

Each gate control channel has an OR’d input for control of the Gate Drive output. The control bits from the SPI input are OR’d with the respective parallel input control bit. Turn-on control for each channel may be initiated either from the SPI control input or the independent parallel input. Each PIx input has CMOS logic level control with an internal active pulldown and must be switched high to turn-on the Gate Drive output. (Refer to the Input Control section of Applications for further details on transfer of control with HLOS/PWM switching).

HLOS, HPW01, HPW45 Pins

The HLOS pin is switched high by an I/O select line to initiate PWM operation using the HPW01 and HPW45 pins. When active, the SPI inputs and the PI0, PI1, PI4 the PI5 parallel inputs are disabled. The channels 0 and 1 are under the direct control of the HPW01 pin and channels 4 and 5 are under the direct control of the HPW45 pin. Channels 2 and 3 have direct and independent control by the PI2 and PI3 inputs. These pins have CMOS logic level control. The HLOS pin has an internal active pullup and the HPW01 and HPW45 have internal active pulldowns. The state of the HPW01 and HPW45 pins are “don’t care” when the HLOS pin is low.

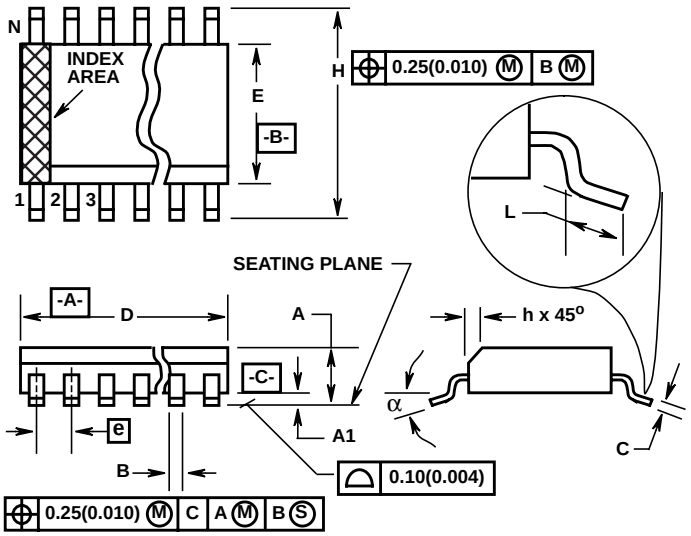
Go Thru G5 Gate Drive Pins

The Gate Drive pins each drive external NDMOS or equivalent MOSFETs to provide low side switching control of the output loads. The Gate Drive pins are switched high to turn-on the MOSFET output. The Gate Drive output is switched to a low duty cycle mode during over-current fault conditions or switched low during low V_{CC} POR reset conditions.

D0 Thru D5 Drain Monitor Pins

The Drain Monitor input pins sense an over-current fault at the drain of the output MOSFET driver by detecting the drain voltage to be higher than an internal voltage reference when the output is on. Open Load conditions are sensed at the Drain Monitor input when the output is off by detecting the drain voltage of the MOSFET to less than in internal reference. For each channel, a single fault bit is returned for either condition. For each channel, an internal zener diode connects the Drain Monitor input to the Gate Drive output to provide voltage clamping when an inductive load is switched off. When the drain to gate zener diode conducts, the gate is turned-on sufficiently to clamp the inductive kick voltage pulse.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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