



FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 134,217,728 x 1 bit structure
- 4096 equal sectors with 4K byte each
256 equal sectors with 64K byte each
 - Any sector can be erased
- Single Power Supply Operation
 - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V

PERFORMANCE

- High Performance
 - Fast access time: 50MHz serial clock (30pF + 1TTL Load)
 - Fast program time: 1.4ms/page (typical, 256-byte per page) and 9us/byte (typical)
 - Fast erase time: 60ms/sector (4KB per sector), 0.7s/block (64KB per block) and 80s/chip
 - Acceleration mode:
 - Chip erase time: 50s (typical)
- Low Power Consumption
 - Low active read current: 25mA (max.) at 50MHz
 - Low active programming current: 20mA (max.)
 - Low active erase current: 20mA (max.)
 - Low standby current: 20uA (max.)
 - Deep power-down mode 20uA (max.)
- Typical 100,000 erase/program cycle
- 10 years data retention

SOFTWARE FEATURES

- Input Data Format
 - 1-byte Command code
- Advanced Security Features
 - Block lock protection
 - The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
 - Additional 512-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
 - Automatically erases and verifies data at selected sector
 - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
 - JEDEC 1-byte manufacturer ID and 2-byte Device ID
 - RES command, 1-byte Device ID
 - REMS command, ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

HARDWARE FEATURES

- SCLK Input
 - Serial clock input
- SI Input
 - Serial Data Input
- SO
 - Serial Data Output
- WP#/ACC Pin
 - Hardware write protection and Program/erase acceleration
- HOLD# pin
 - pause the chip without deselecting the chip
- PACKAGE
 - 16-pin SOP (300mil)
 - **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

The MX25L12805D is a CMOS 134,217,728 bit serial Flash Memory, which is configured as 16,777,216 x 8 internally. The MX25L12805D features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

The MX25L12805D provides sequential read operation on whole chip. User may start to read from any byte of the array. While the end of the array is reached, the device will wrap around to the beginning of the array and continuously outputs data until CS# goes high.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, and erase command is executed on sector (4K-byte), or block(64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

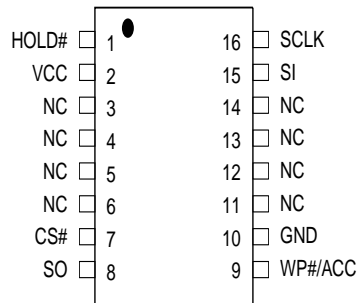
Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 20uA DC current.

The MX25L12805D utilizes MXIC's proprietary memory cell which reliably stores memory contents even after 100,000 program and erase cycles.

PIN CONFIGURATIONS

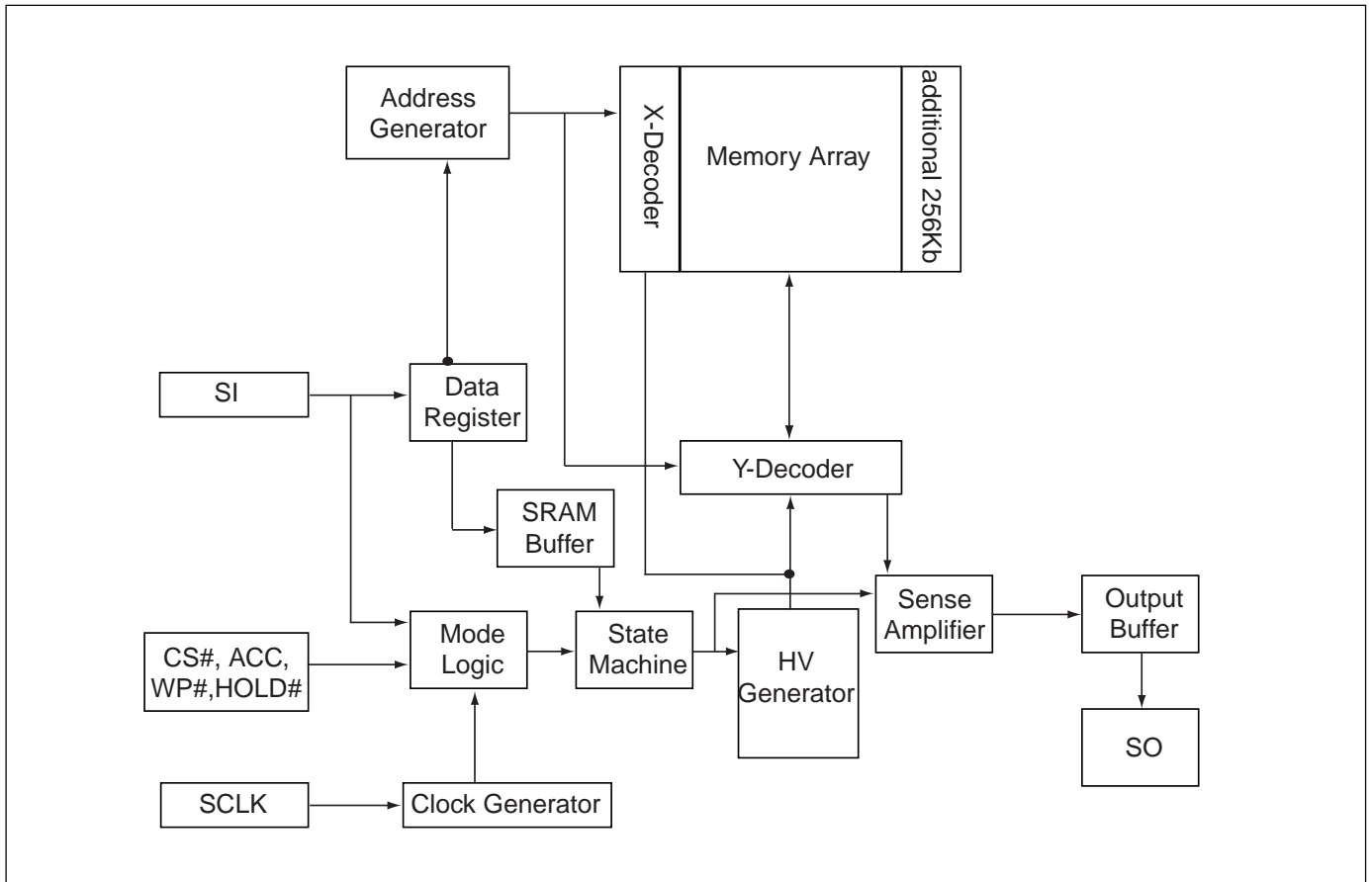
16-PIN SOP (300 mil)



PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
HOLD#	Hold, to pause the serial communication
WP#/ACC	Write Protection: connect to GND; 11V for program/erase acceleration: connect to 11V
VCC	+ 3.3V Power Supply
GND	Ground
NC	No Internal Connection

BLOCK DIAGRAM



DATA PROTECTION

The MX25L12805D are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Power-on reset and tPUW: to avoid sudden power switch by system power supply transition, the power-on reset and tPUW (internal timer) may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
 - Power-up
 - Write Disable (WRDI) command completion
 - Write Status Register (WRSR) command completion
 - Page Program (PP) command completion
 - Sector Erase (SE) command completion
 - Block Erase (BE) command completion
 - Chip Erase (CE) command completion
- Software Protection Mode (SPM): by using BP0-BP3 bits to set the part of Flash protected from data change.
- Hardware Protection Mode (HPM): by using WP# going low to protect the BP0-BP3 bits and SRWD bit from data change.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of "Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

Please refer to table of "protected area sizes".

- The Hardware Protected Mode (HPM) use WP#/ACC to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit.

II. Additional 512-bit secured OTP for unique identifier: to provide 512-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to table 3. 512-bit secured OTP definition.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 512-bit secured OTP by entering 512-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 512-bit secured OTP mode by writing EXSO command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command

to set customer lock-down bit1 as "1". Please refer to table of "security register definition" for security register bit definition and table of "512-bit secured OTP definition" for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 512-bit secured OTP mode, array access is not allowed.

512-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxxx00~xxxx0F	128-bit	ESN (electrical serial number)	Determined by customer
xxxx10~xxxx3F	384-bit	N/A	

Table 1. Protected Area Sizes

Status bit				Protection Area
BP3	BP2	BP1	BP0	128Mb
1	1	1	1	All
1	1	1	0	All
1	1	0	1	All
1	1	0	0	All
1	0	1	1	All
1	0	1	0	All
1	0	0	1	All
1	0	0	0	Upper half (hundred and twenty-eight sectors: 128 to 255)
0	1	1	1	Upper quarter (sixty-four sectors: 192 to 255)
0	1	1	0	Upper eighth (thirty-two sectors: 224 to 255)
0	1	0	1	Upper sixteenth (sixteen sectors: 240 to 255)
0	1	0	0	Upper 32nd (eight sectors: 248 to 255)
0	0	1	1	Upper 64th (four sectors: 252 to 255)
0	0	1	0	Upper 128th (two sectors: 254 and 255)
0	0	0	1	Upper 256th (one sector: 255)
0	0	0	0	None

Note:

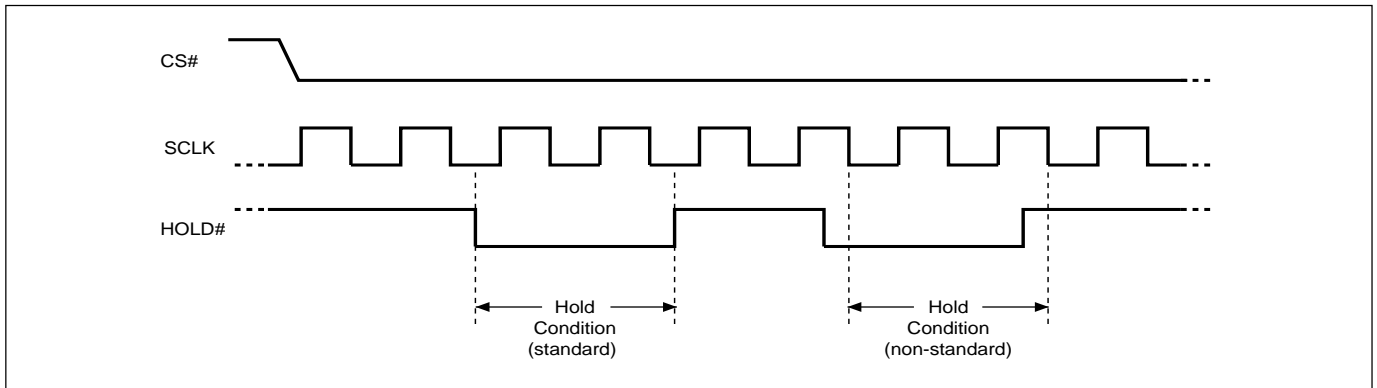
1. The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select(CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low(if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see Figure 1.

Figure 1. Hold Condition Operation

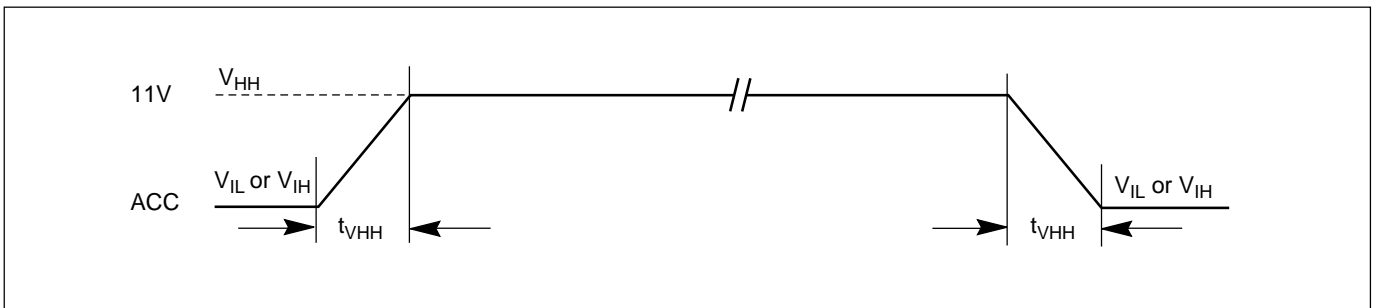


The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

PROGRAM/ERASE ACCELERATION

To activate the program/erase acceleration function requires ACC pin connecting to 11V voltage (see Figure 2), and then to be followed by the normal program/erase process. By utilizing the program/erase acceleration operation, the performances are improved as shown on table of "ERASE AND PROGRAM PERFORMANCE".

Figure 2. ACCELERATED PROGRAM TIMING DIAGRAM



Note: t_{VHH} (V_{VHH} Rise and Fall Time) min. 250ns

Table 2. COMMAND DEFINITION

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	FAST READ (fast read data)	SE (Sector erase)
1st byte	06 (hex)	04 (hex)	9F (hex)	05 (hex)	01 (hex)	03 (hex)	0B (hex)	20 (hex)
2nd byte						AD1	AD1	AD1
3rd byte						AD2	AD2	AD2
4th byte						AD3	AD3	AD3
5th byte							X	
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte manufacturer ID & 2-byte device ID	to read out the values of the status register	to write new values to the status register	n bytes read out until CS# goes high	n bytes read out until CS# goes high	to erase the selected sector

COMMAND (byte)	BE (block erase)	CE (chip erase)	PP (Page program)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)	AB (hex)	AB (hex)	90 (hex)
2nd byte	AD1		AD1			x	x
3rd byte	AD2		AD2			x	x
4th byte	AD3		AD3			x	ADD(note 1)
5th byte							
Action	to erase the selected block	to erase whole chip	to program the selected page	enters deep power down mode	release from deep power down mode	to read out 1-byte device ID	output the manufacturer ID & device ID

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first

COMMAND (byte)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)
1st byte	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)
2nd byte				
3rd byte				
4th byte				
5th byte				
Action	to enter the 512-bit secured OTP mode	to exit the 512-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)

Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Table 3. Memory Organization

Block	Sector	Address Range	
255	4095	FFF000h	FFFFFFh
	⋮		
	4080	FF0000h	FF0FFFh
254	4079	FEF000h	FEFFFFh
	⋮		
	4064	FE0000h	FE0FFFh
253	4063	FDF000h	FDFFFFh
	⋮		
	4048	FD0000h	FD0FFFh
252	4047	FCF000h	FCFFFFh
	⋮		
	4032	FC0000h	FC0FFFh
251	4031	FBF000h	FBFFFFh
	⋮		
	4016	FB0000h	FB0FFFh
250	4015	FAF000h	FAFFFFh
	⋮		
	4000	FA0000h	FA0FFFh

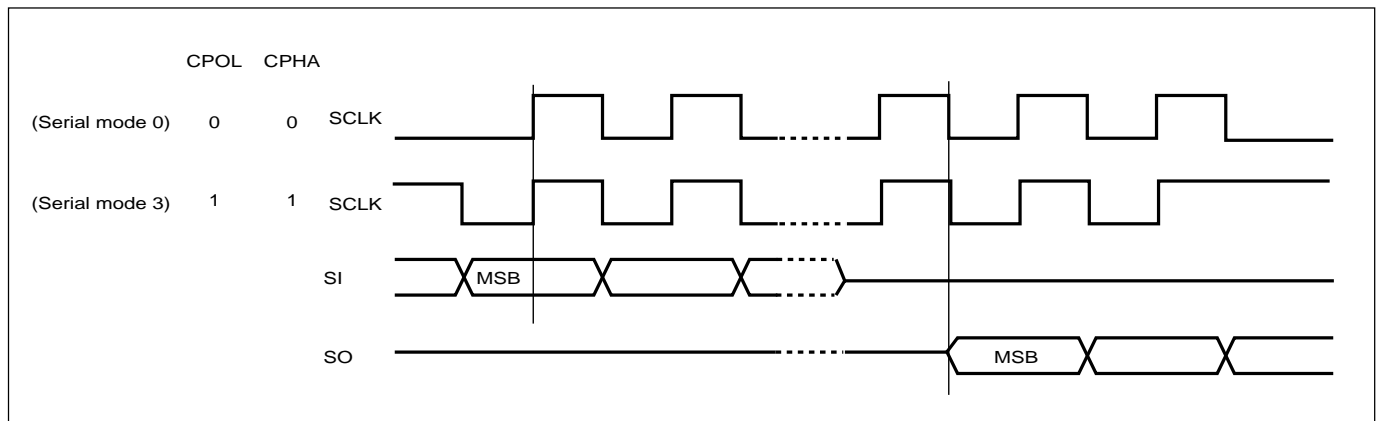


5	95	05F000h	05FFFFh
	⋮		
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	⋮		
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	⋮		
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	⋮		
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	⋮		
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	⋮		
	0	000000h	000FFFh

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as Figure 3.
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RES and REMS the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, RDP, DP, ENSO, EXSO, and WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 3. Serial Modes Supported



Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

COMMAND DESCRIPTION

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, BE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low-> sending WREN instruction code-> CS# goes high. (see Figure 12)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for re-setting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low-> sending WRDI instruction code-> CS# goes high. (see Figure 13)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte device ID, and the individual device ID of second-byte ID is as followings: 18(hex).

The sequence of issuing RDID instruction is: CS# goes low-> sending RDID instruction code -> 24-bits ID data out on SO -> to end RDID operation can use CS# to high at any time during data out. (see Figure. 14)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low-> sending RDSR instruction code-> Status Register data out on SO (see Figure. 15)

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and not affect value of WEL bit if it is applied to a protected memory area.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area(as defined in table 1) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed).

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP# pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRWD Status Register Write Protect	reserved	BP3 the level of protected block	BP2 the level of protected block	BP1 the level of protected block	BP0 the level of protected block	WEL (write enable latch)	WIP (write in progress bit)
1= status register write disable		(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation

Note: 1. see the table "Protected Area Sizes".

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in table 1). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low-> sending WRSR instruction code-> Status Register data on SI-> CS# goes high. (see Figure 16)

The WRSR instruction has no effect on b6, b1, b0 of the status register.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 4. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode(SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:

1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in Table 1.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note: If SRWD bit=1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP# to against data modification.

Note: to exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low-> sending READ instruction code-> 3-byte address on SI -> data out on SO-> to end READ operation can use CS# to high at any time during data out. (see Figure. 17)

(7) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low-> sending FAST_READ instruction code-> 3-byte address on SI-> 1-dummy byte address on SI->data out on SO-> to end FAST_READ operation can use CS# to high at any time during data out. (see Figure. 18)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector and 1K-byte parameter sector while parameter sectors are enable. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table 3) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low -> sending SE instruction code-> 3-byte address on SI -> CS# goes high. (see Figure 20)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the page.

(9) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte sector erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see table 3) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low -> sending BE instruction code-> 3-byte address on SI -> CS# goes high. (see Figure 21)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the page.

(10) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (see table 3) is a valid address for Chip Erase (CE) instruction. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low-> sending CE instruction code-> CS# goes high. (see Figure 22)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

(11) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If the eight least significant address bits (A7-A0) are not all 0, all transmitted data which goes beyond the end of the current page are programmed from the start address if the same page (from the address whose 8 least significant address bits (A7-A0) are all 0). The CS# must keep during the whole Page Program cycle. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed. If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the request address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low-> sending PP instruction code-> 3-byte address on SI-> at least

1-byte on data on SI-> CS# goes high. (see Figure 19)

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

(12) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low-> sending DP instruction code-> CS# goes high. (see Figure 23)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (RES instruction to allow the ID been read out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not be executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

(13) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in Table 6. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP, RES, and REMS are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The sequence is shown as Figure 24,25.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power Down Mode.

(14) Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 26. The Device ID values are listed in Table of ID Definitions on page 20. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table of ID Definitions:

1. RDID:			
	manufacturer ID	memory type	memory density
MX25L12805D	C2	20	18
2. RES:			
	electronic ID		
MX25L12805D	17		
3. REMS:			
	manufacturer ID	device ID	
MX25L12805D	C2	17	

(15) Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 512-bit secured OTP mode. The additional 512-bit secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low-> sending ENSO instruction to enter Secured OTP mode -> CS# goes high.

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

(16) Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 512-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low-> sending EXSO instruction to exit Secured OTP mode-> CS# goes high.

(17) Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low-> sending RDSCUR instruction -> Security Register data out on SO-> CS# goes high.

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non- factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 512-bit Secured OTP area cannot be update any more. While it is in 512-bit secured OTP mode, array access is not allowed.

Table of Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	x	x	x	LDSO (indicate if lock-down)	Secured OTP indicator bit
reserved	reserved	reserved	reserved	reserved	0	0 = not lock-down 1 = lock-down (cannot program/erase OTP)	0 = non-factory lock 1 = factory lock
volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit

(18) Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. Unlike write status register, the WREN instruction is not required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 512-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low-> sending WRSCUR instruction -> CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

POWER-ON STATE

The device is at below states when power-up:

- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, after VCC reaching the VWI level, a tPUW time delay is required before the device is fully accessible for commands like write enable(WREN), page program (PP), sector erase(SE), block erase (BE), chip erase(CE) and write status register(WRSR). If the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:

- tPUW after VCC reached VWI level
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL, even time of tPUW has not passed.

Please refer to the figure of "power-up timing".

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended.(generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40° C to 85° C for Industrial grade
Storage Temperature	-55° C to 125° C
Applied Input Voltage	-0.5V to 4.6V
Applied Output Voltage	-0.5V to 4.6V
VCC to Ground Potential	-0.5V to 4.6V

NOTICE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to 4.6V or -0.5V for period up to 20ns.
4. All input and output pins may overshoot to VCC+0.5V while VCC+0.5V is smaller than or equal to 4.6V.

Figure 4. Maximum Negative Overshoot Waveform

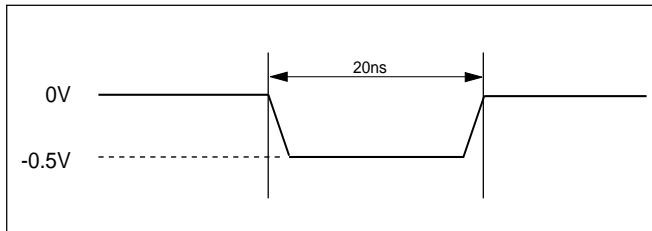
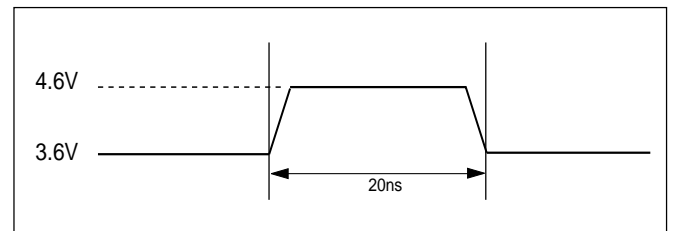


Figure 5. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25° C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			10	pF	VIN = 0V
COUT	Output Capacitance			10	pF	VOUT = 0V

Figure 6. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

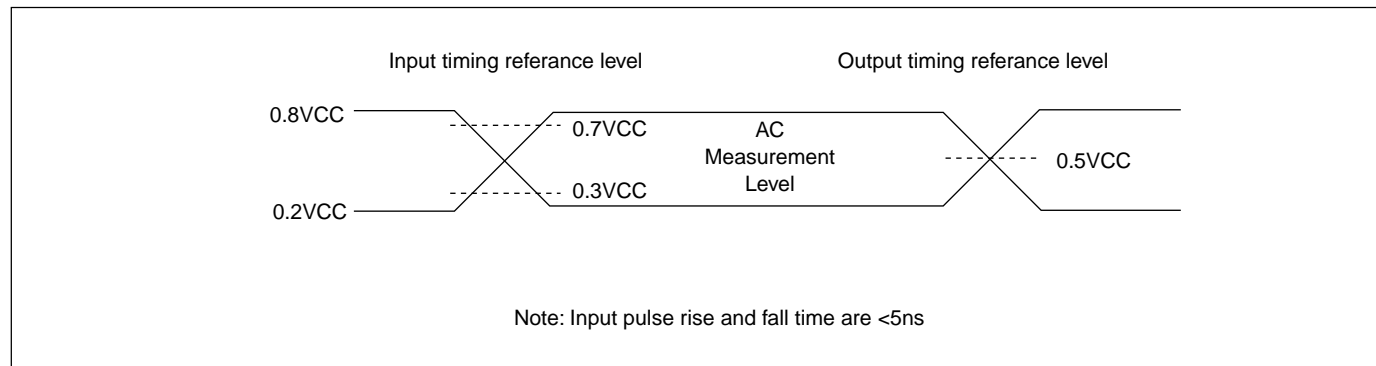


Figure 7. OUTPUT LOADING

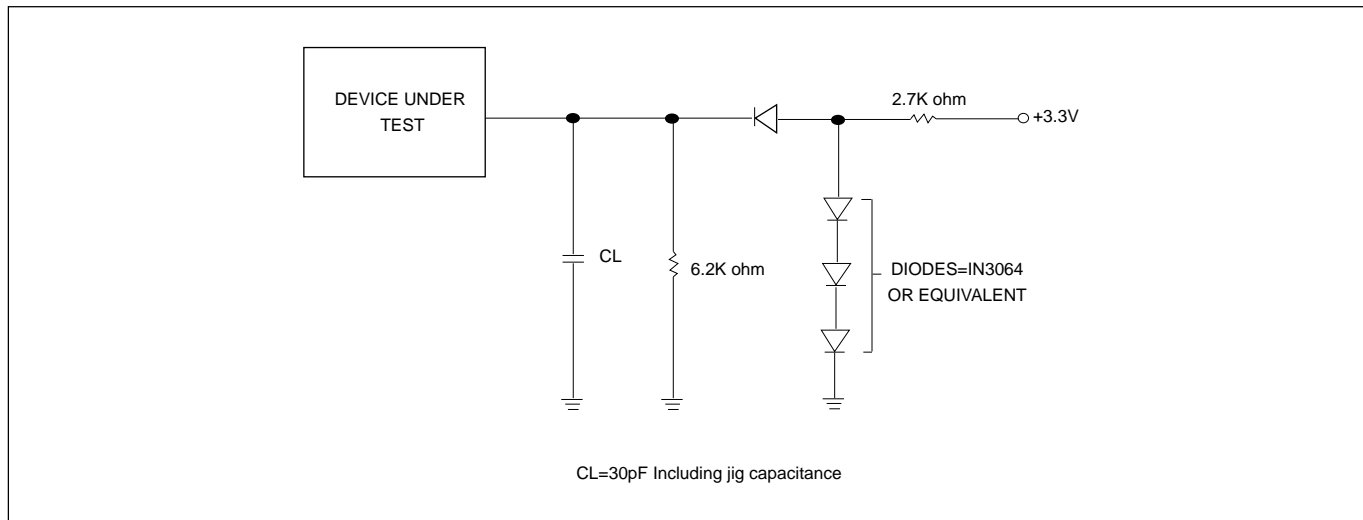


Table 5. DC CHARACTERISTICS (Temperature = -40° C to 85° C, VCC = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1			± 2	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			± 2	uA	VCC = VCC Max VIN = VCC or GND
ILIHV	HV pin input Leakage Current				35	uA	WP#/ACC=11.5V
ISB1	VCC Standby Current	1			20	uA	VIN = VCC or GND CS# = VCC
ISB2	Deep Power-down Current				20	uA	VIN = VCC or GND CS# = VCC
ICC1	VCC Read	1			25 15	mA mA	f=50MHz (serial) f=33MHz (serial)
ICC2	VCC Program Current (PP)	1			20	mA	Program in Progress CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current				20	mA	Program status register in progress CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1			20	mA	Erase in Progress CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1			20	mA	Erase in Progress CS#=VCC
VHH	Voltage for ACC Program Acceleration	1		11	11.5	V	VCC=2.7V~3.6V
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

NOTES:

1. Typical values at VCC = 3.3V, T = 25° C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 6. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V)

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RES,RDP WREN, WRDI, RDID, RDSR, WRSR	10K		50M (Condition:30pF)	Hz
fRSCLK	fR	Clock Frequency for READ instructions	10K		33M	Hz
tCH(1)	tCLH	Clock High Time	7			ns
tCL(1)	tCLL	Clock Low Time	7			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)	0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)	0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			ns
tDVCH	tDSU	Data In Setup Time	2			ns
tCHDX	tDH	Data In Hold Time	5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	5			ns
tSHSL	tCSH	CS# Deselect Time	100			ns
tSHQZ(2)	tDIS	Output Disable Time	2.7V-3.6V		10	ns
			3.0V-3.6V		8	ns
tCLQV	tV	Clock Low to Output Valid	2.7V-3.6V		10	ns
			3.0V-3.6V		8	ns
tCLQX	tHO	Output Hold Time	0			ns
tHLCH		HOLD# Setup Time (relative to SCLK)	5			ns
tCHHH		HOLD# Hold Time (relative to SCLK)	5			ns
tHHCH		HOLD Setup Time (relative to SCLK)	5			ns
tCHHL		HOLD Hold Time (relative to SCLK)	5			ns
tHHQX(2)	tLZ	HOLD to Output Low-Z	2.7V-3.6V		10	ns
			3.0V-3.6V		8	ns
tHLQZ(2)	tHZ	HOLD# to Output High-Z	2.7V-3.6V		10	ns
			3.0V-3.6V		8	ns
tWHSL(4)		Write Protect Setup Time	20			ns
tSHWL(4)		Write Protect Hold Time	100			ns
tDP(2)		CS# High to Deep Power-down Mode			10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read			8.8	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read			8.8	us
tW		Write Status Register Cycle Time		40	100	ms
tBP		Byte-Program		9	300	us
tPP		Page Program Cycle Time		1.4	5	ms
tSE		Sector Erase Cycle Time		60	300	ms
tBE		Block Erase Cycle Time		0.7	2	s
tCE		Chip Erase Cycle Time		80	200	s

Notes:

1. tCH + tCL must be greater than or equal to 1/ fC
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. Test condition is shown as Figure 5.

Table 7. Power-Up Timing and VWI Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low	200		us
tPUW(1)	Time delay to Write instruction	1	10	ms
VWI(1)	Write Inhibit Voltage	1.5	2.5	V

Note: 1. These parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Figure 8. Serial Input Timing

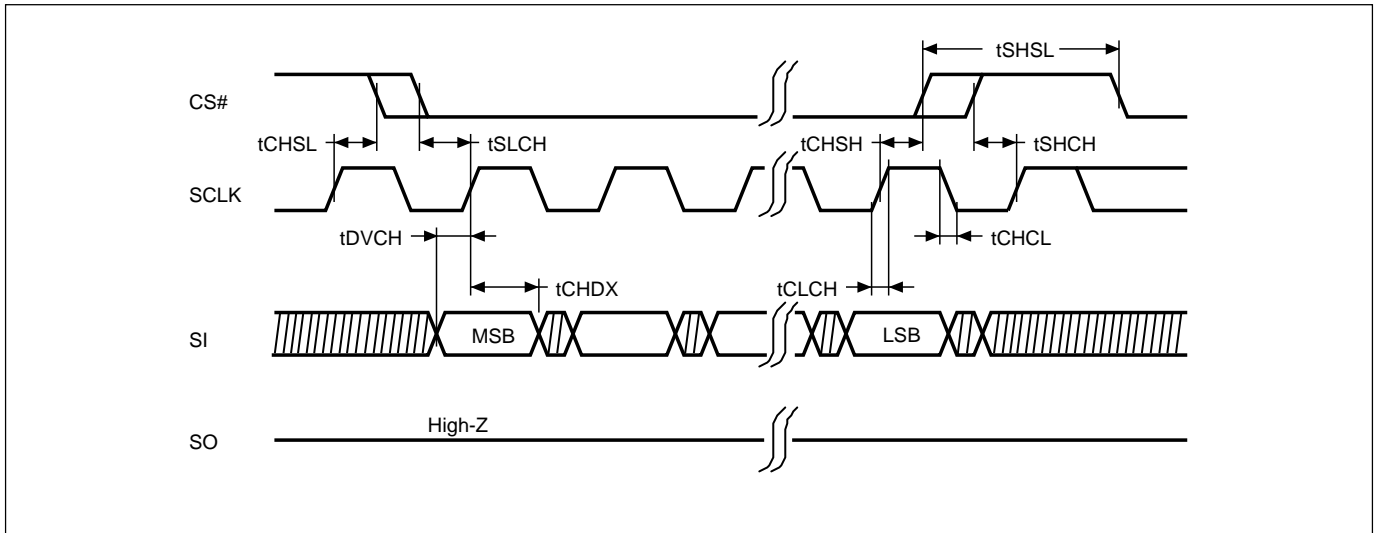


Figure 9. Output Timing

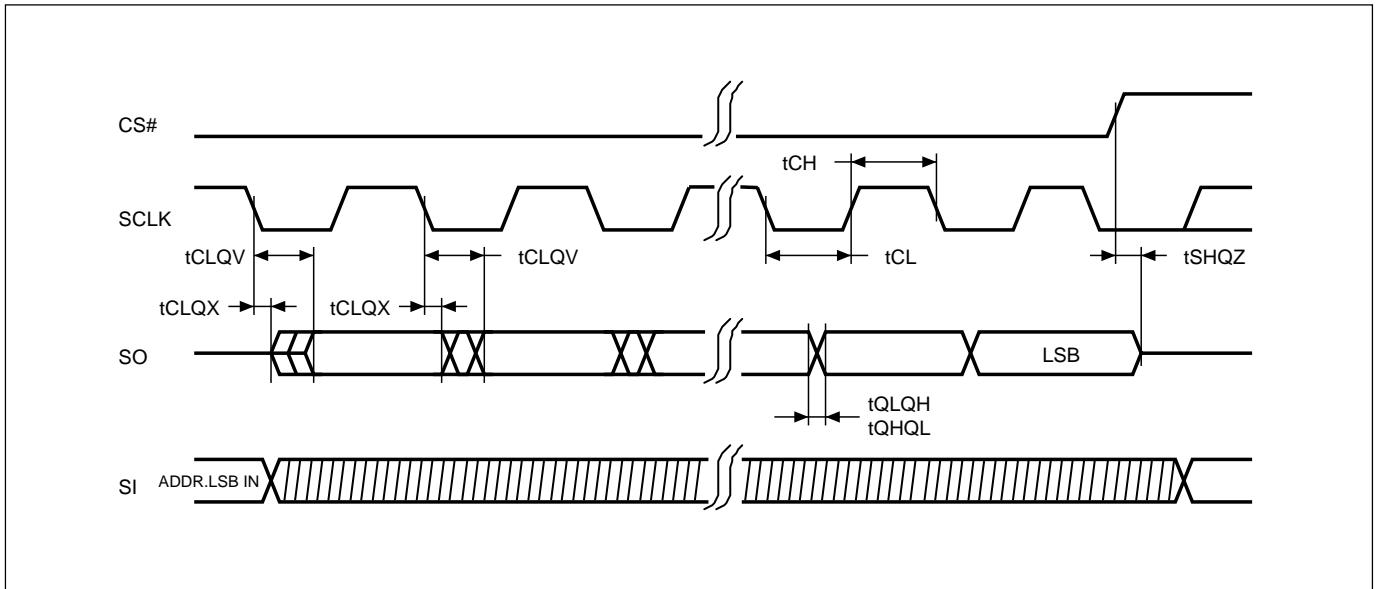
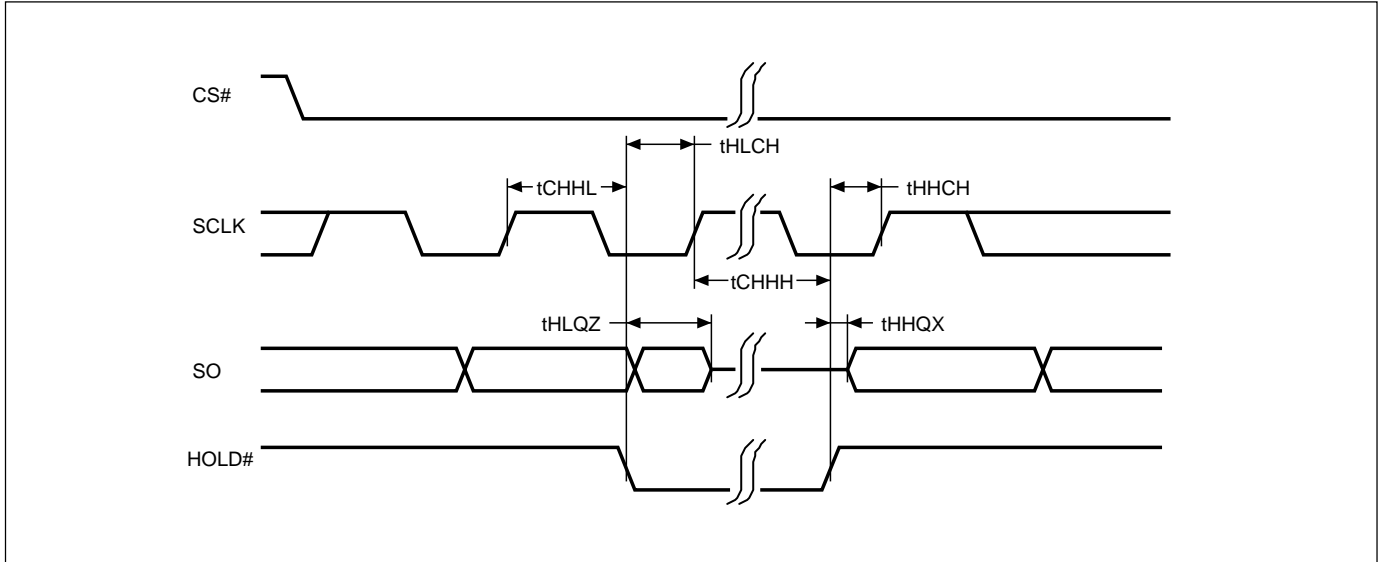


Figure 10. Hold Timing



* SI is "don't care" during HOLD operation.

Figure 11. WP# Disable Setup and Hold Timing during WRSR when SRWD=1

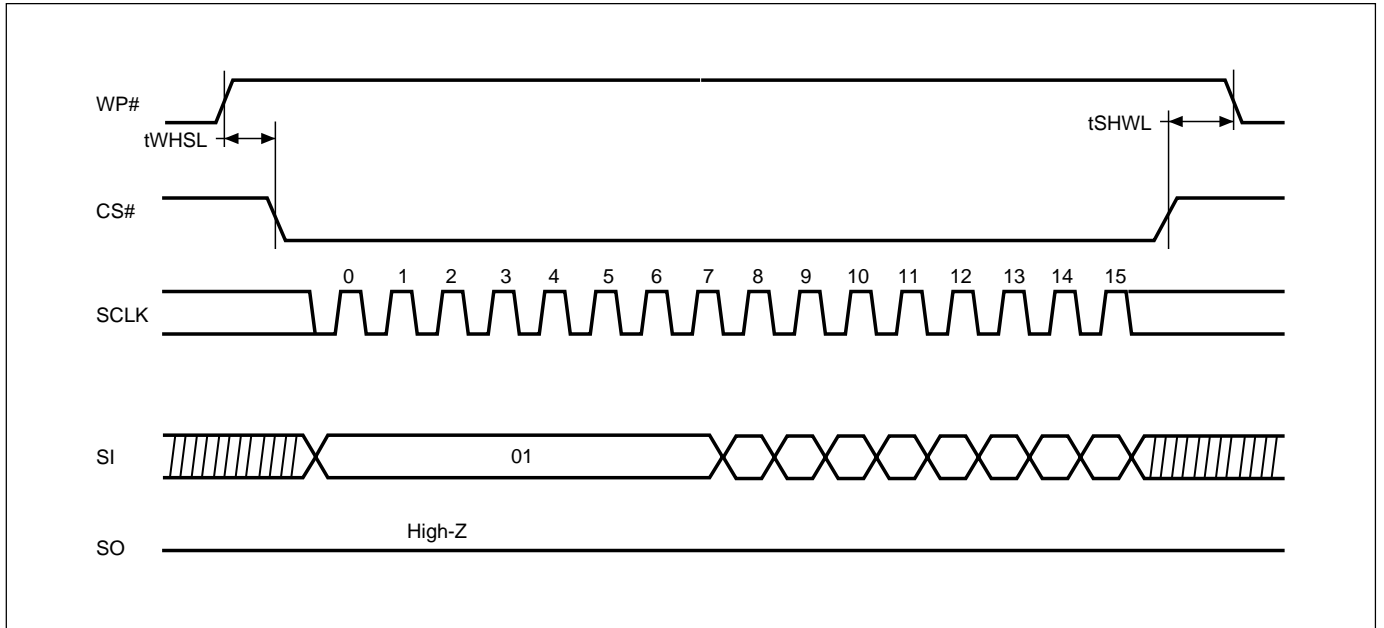


Figure 12. Write Enable (WREN) Sequence (Command 06)

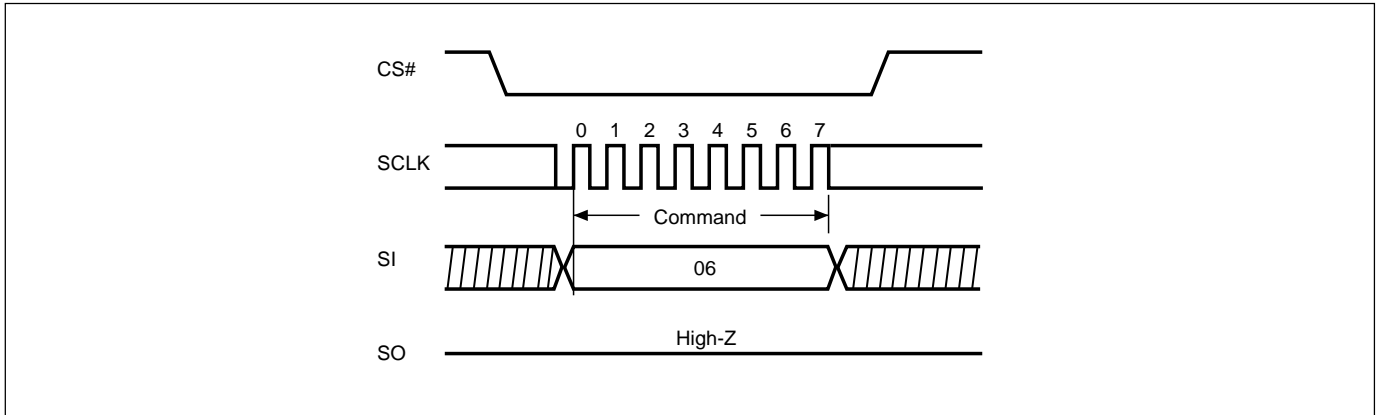


Figure 13. Write Disable (WRDI) Sequence (Command 04)

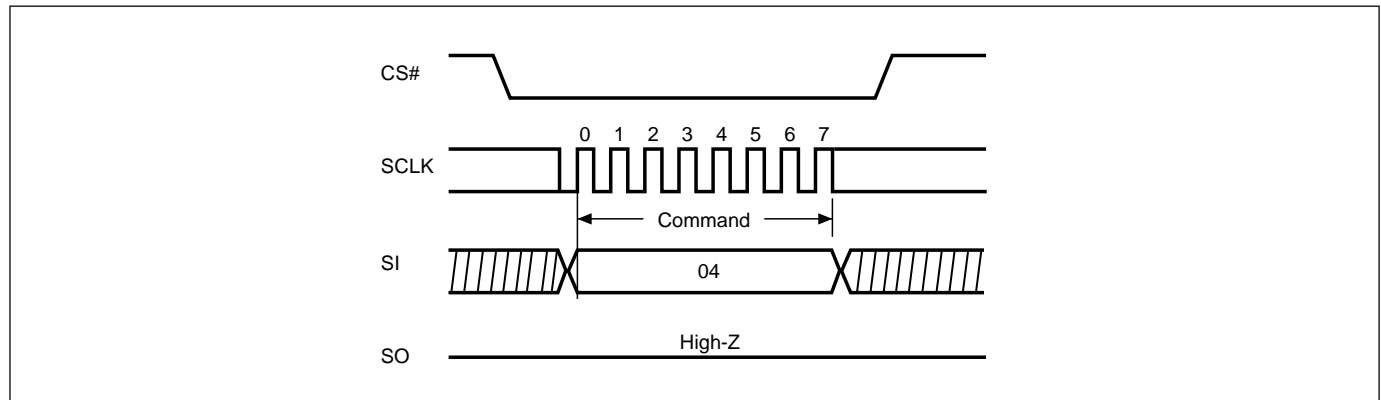


Figure 14. Read Identification (RDID) Sequence (Command 9F)

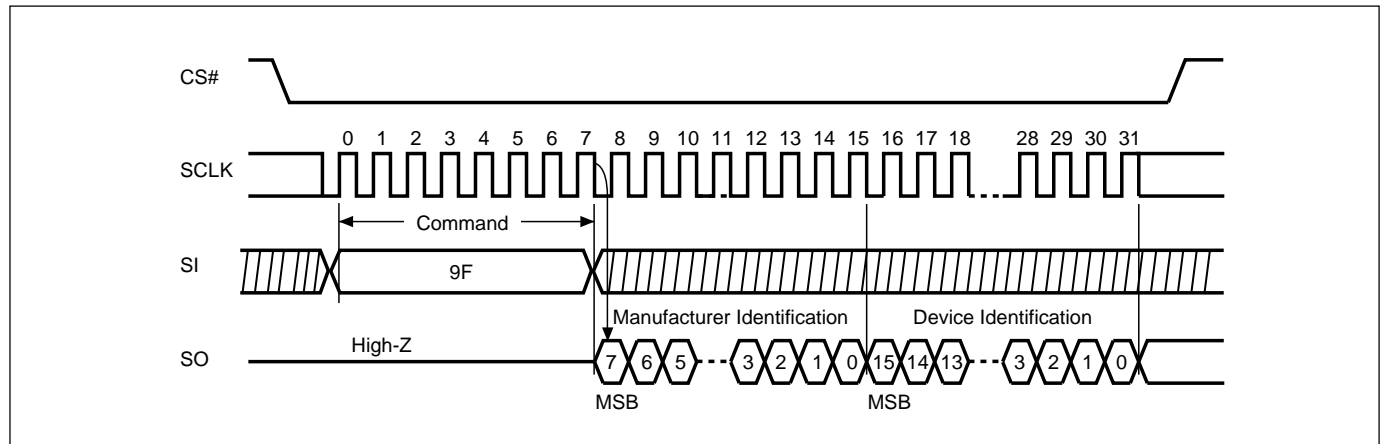


Figure 15. Read Status Register (RDSR) Sequence (Command 05)

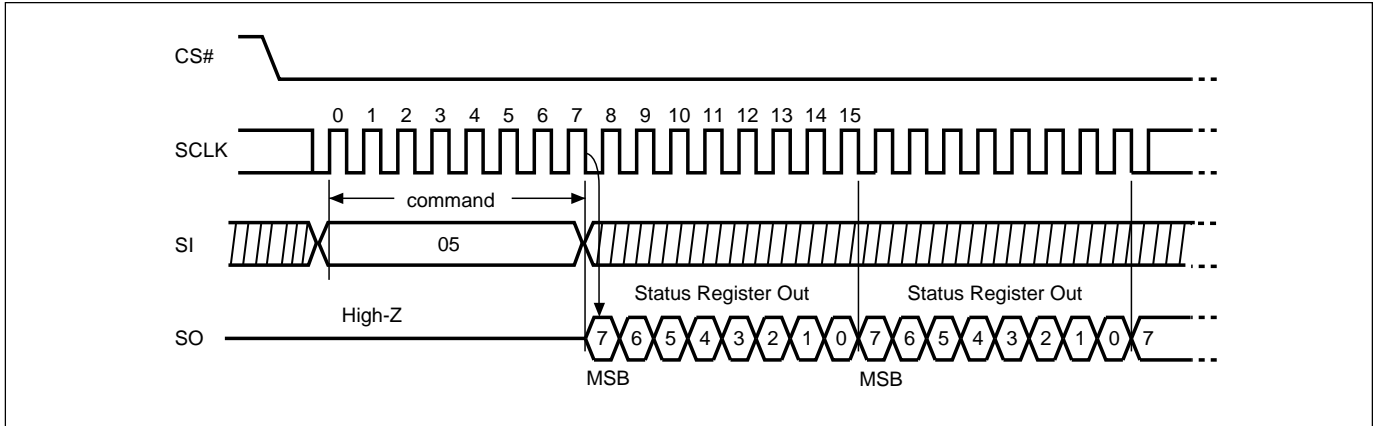


Figure 16. Write Status Register (WRSR) Sequence (Command 01)

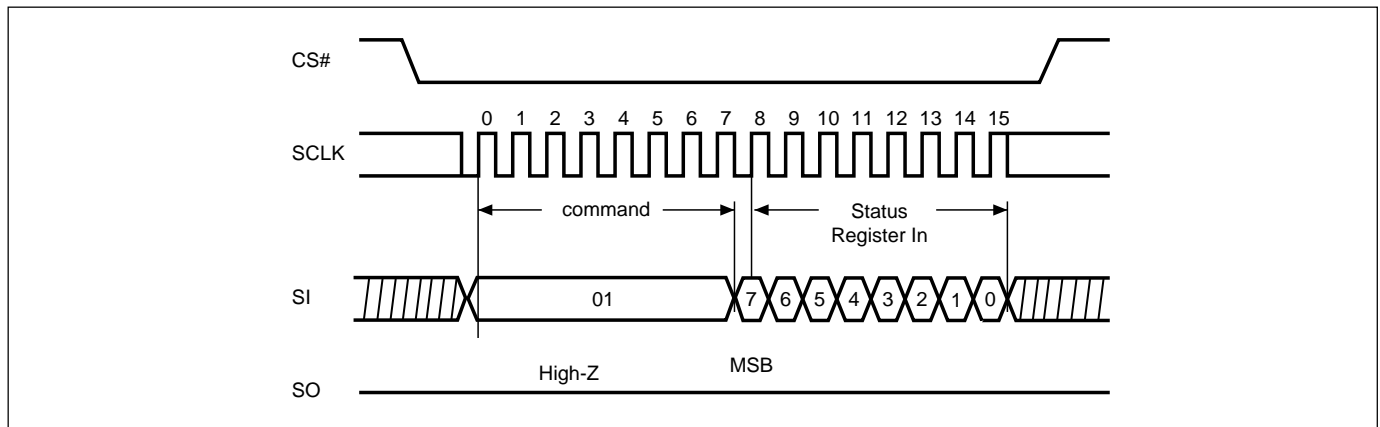


Figure 17. Read Data Bytes (READ) Sequence (Command 03)

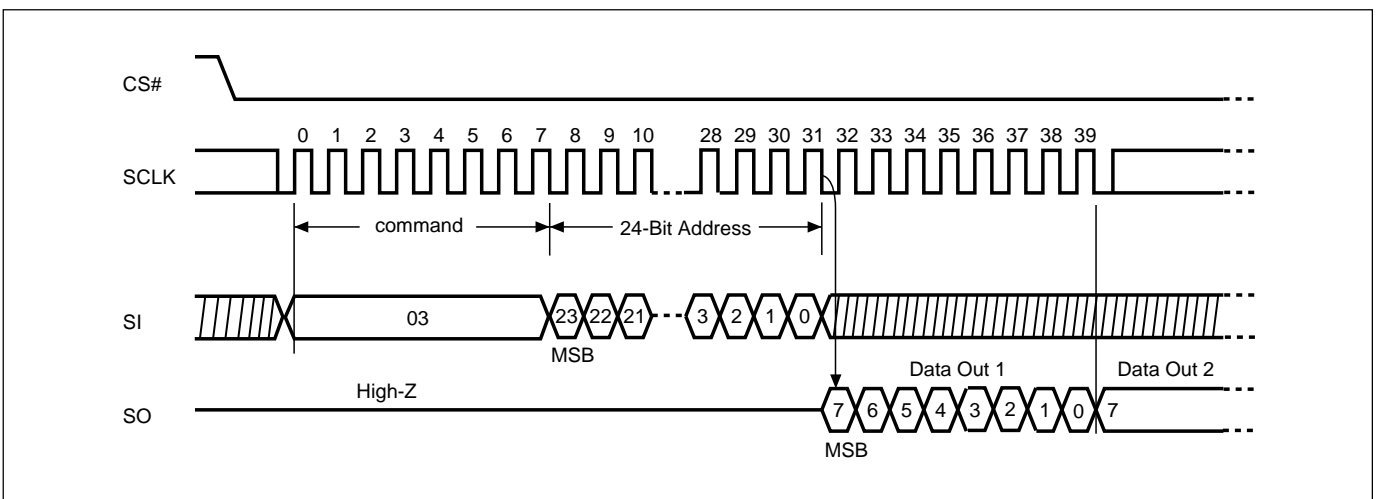


Figure 18. Read Data Bytes at Higher Speed (FAST_READ) Sequence (Command 0B)

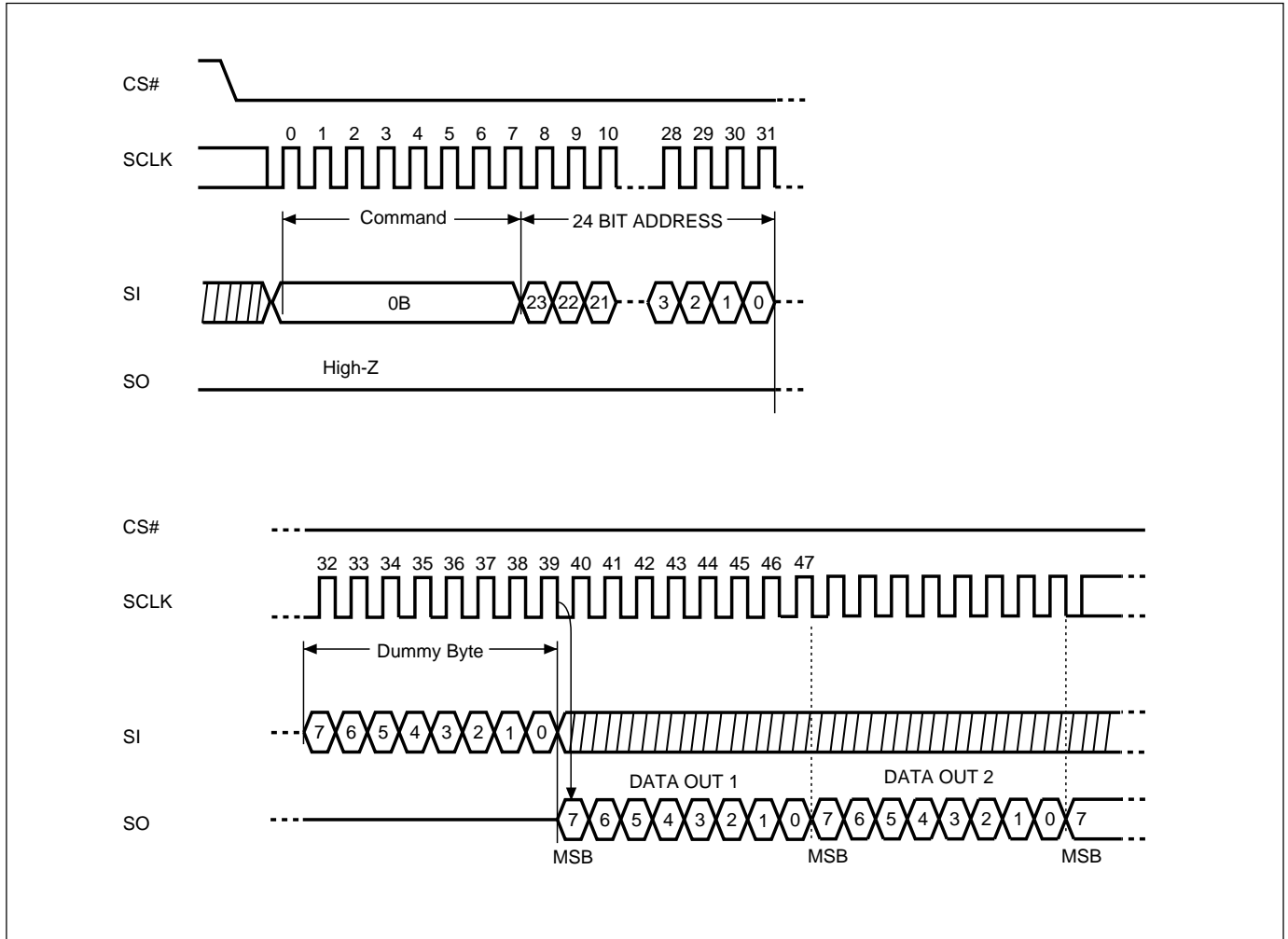


Figure 19. Page Program (PP) Sequence (Command 02)

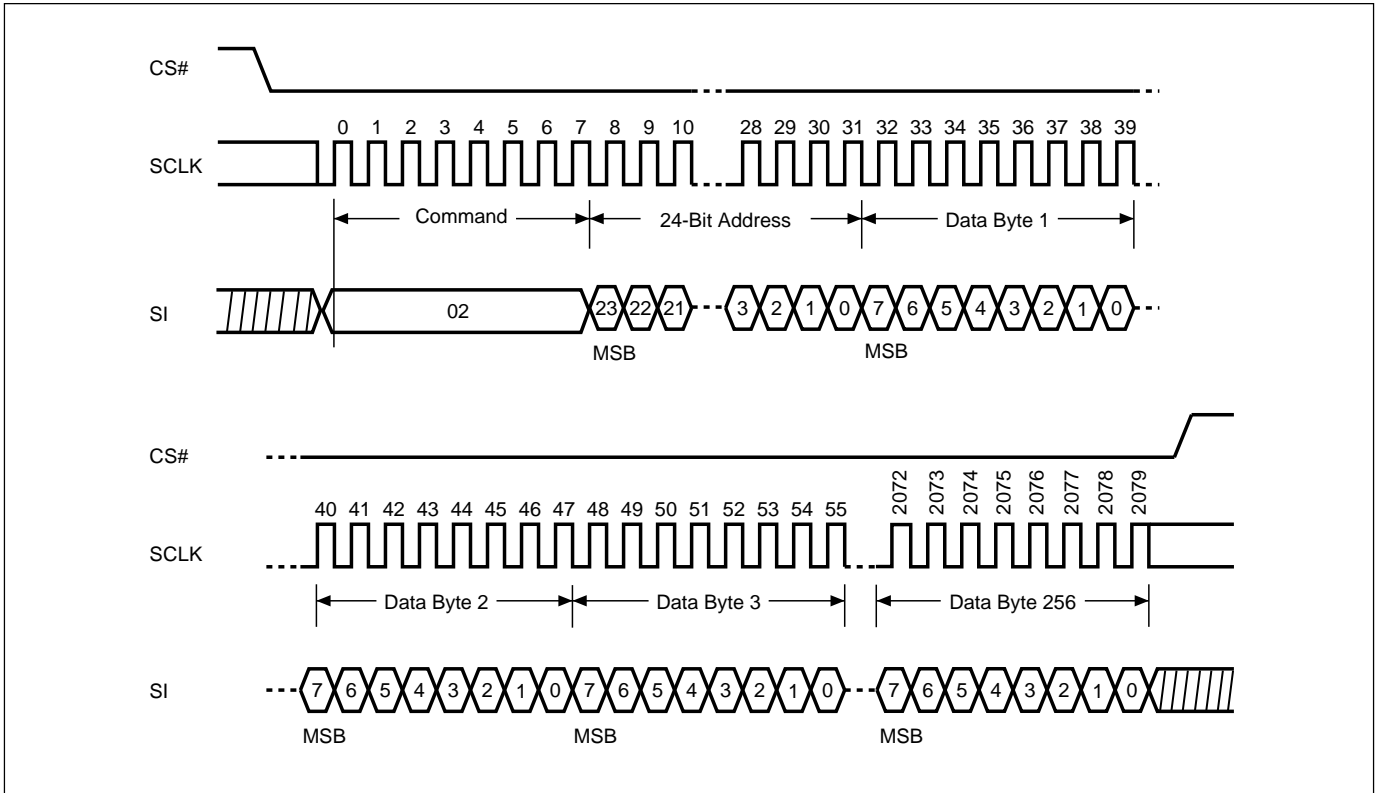
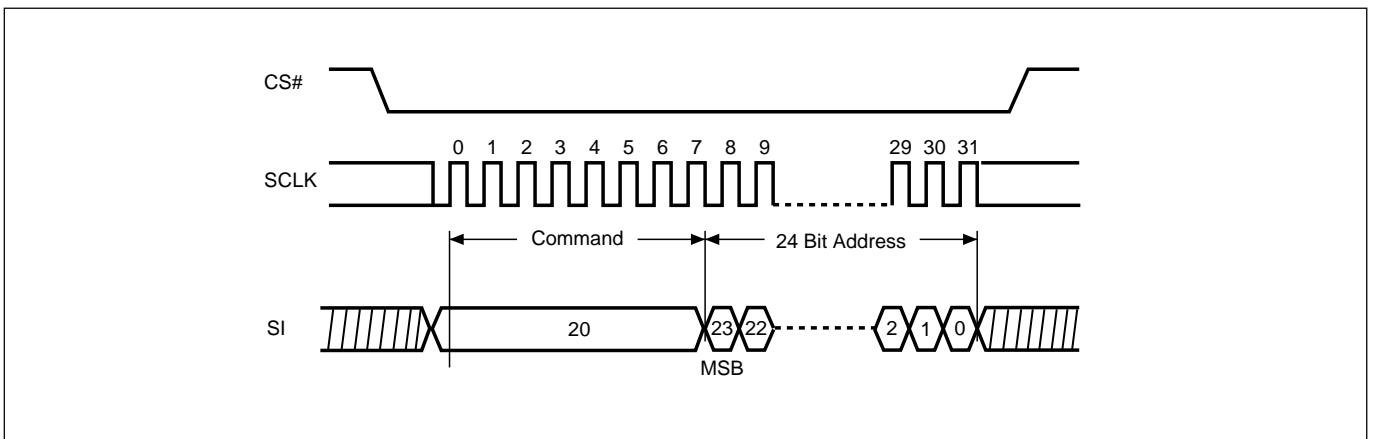
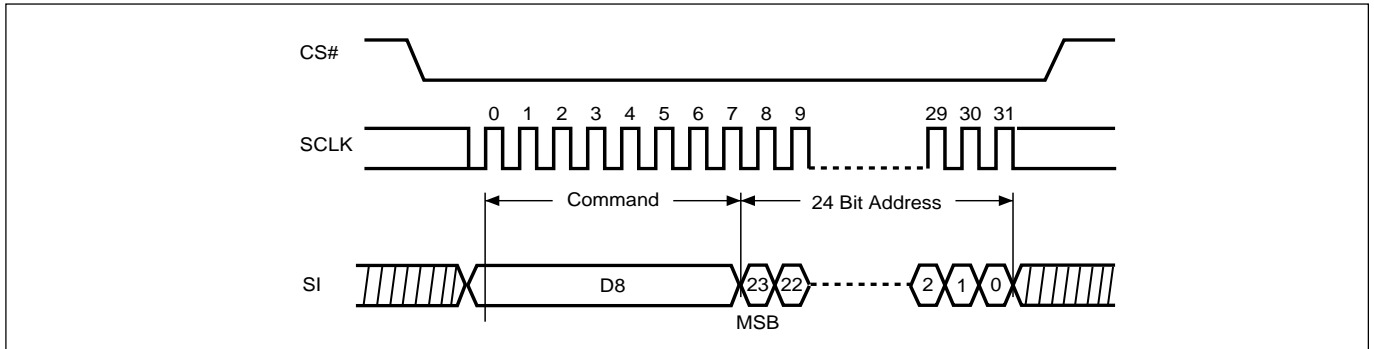


Figure 20. Sector Erase (SE) Sequence (Command 20)



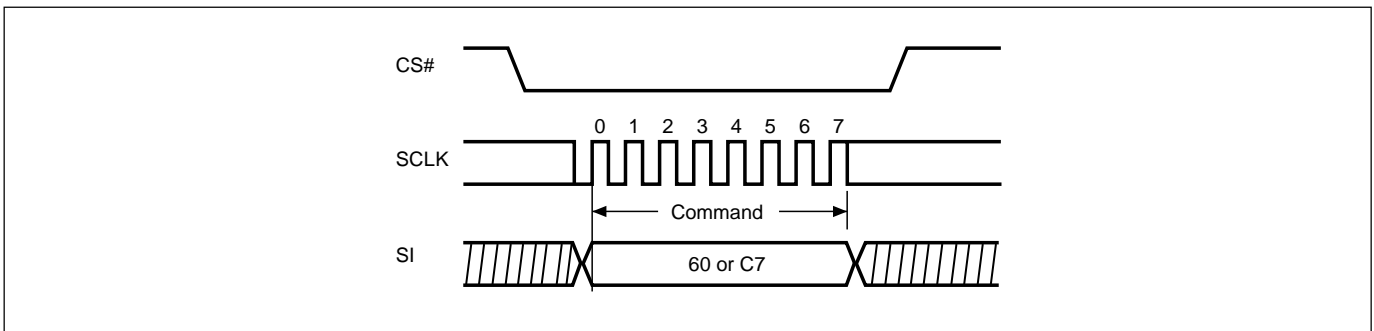
Note: SE command is 20(hex).

Figure 21. Block Erase (BE) Sequence (Command D8)



Note: BE command is D8(hex).

Figure 22. Chip Erase (CE) Sequence (Command 60 or C7)



Note: CE command is 60(hex) or C7(hex).

Figure 23. Deep Power-down (DP) Sequence (Command B9)

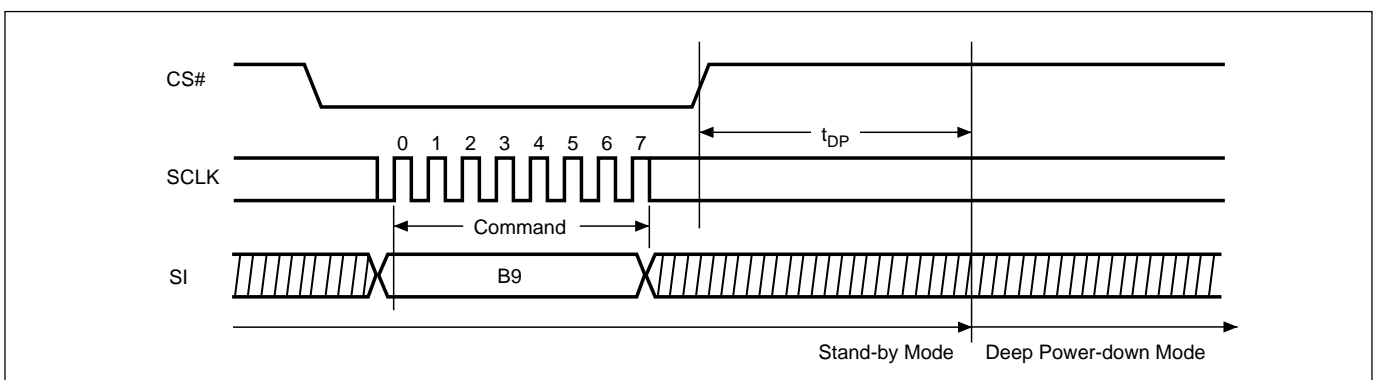


Figure 24. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)

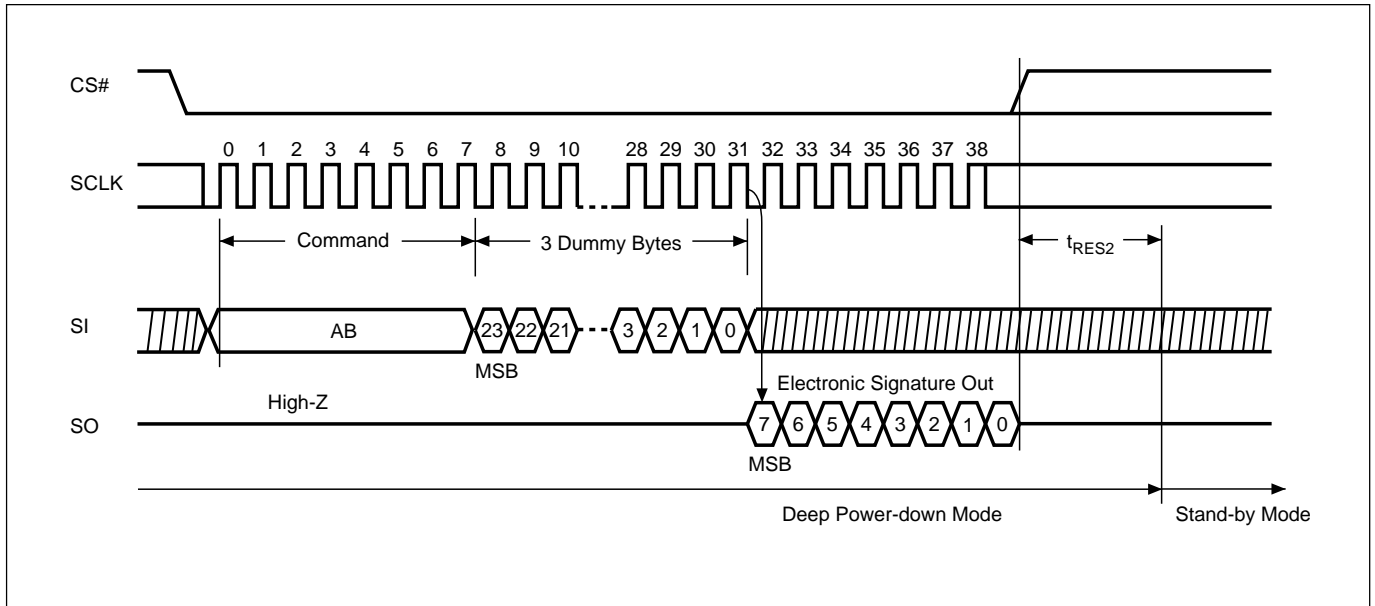


Figure 25. Release from Deep Power-down (RDP) Sequence (Command AB)

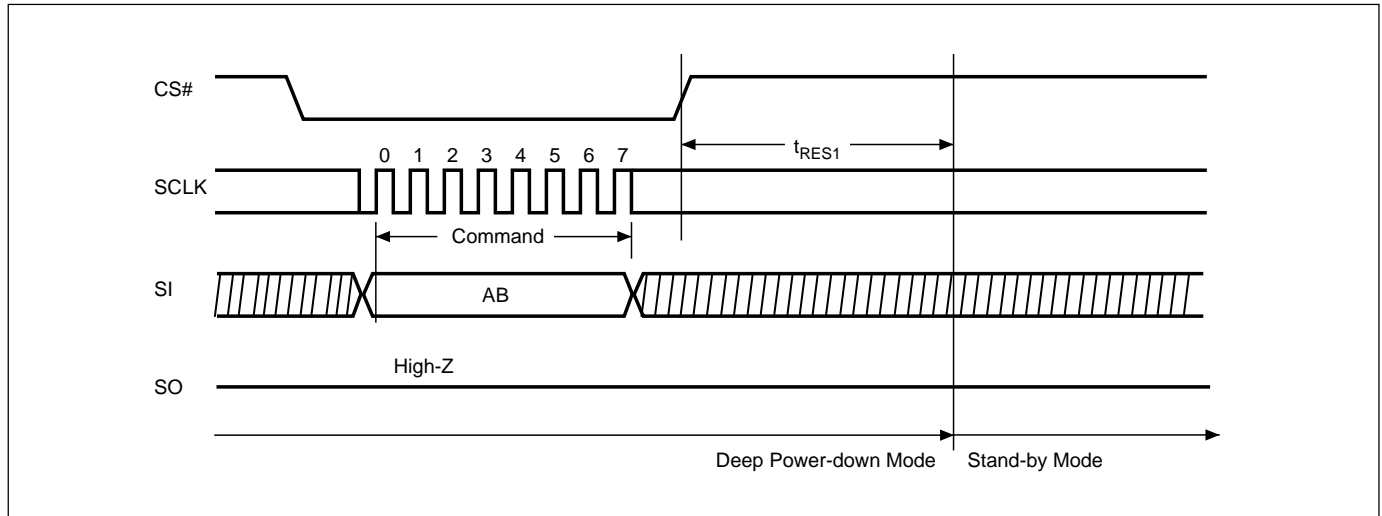
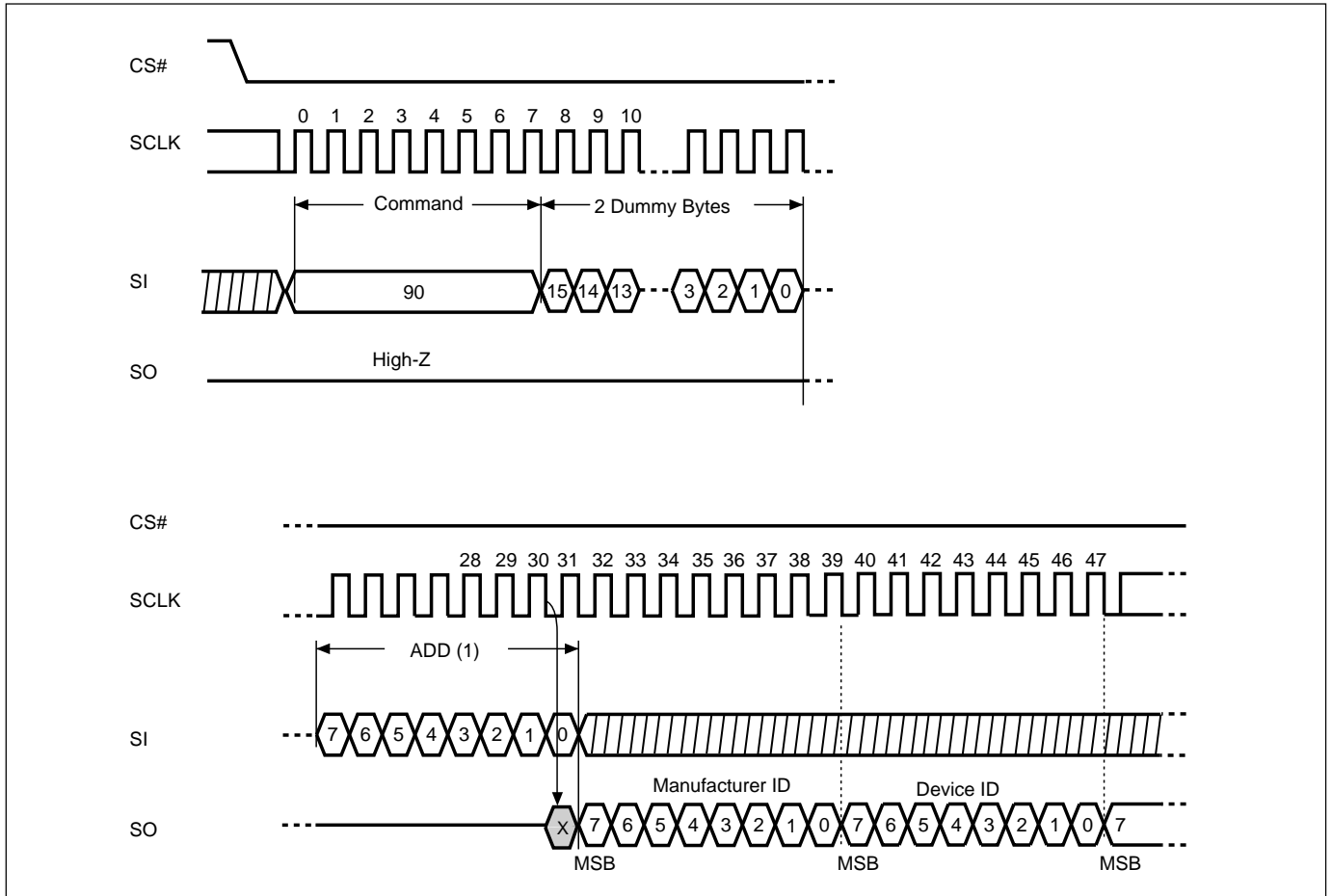


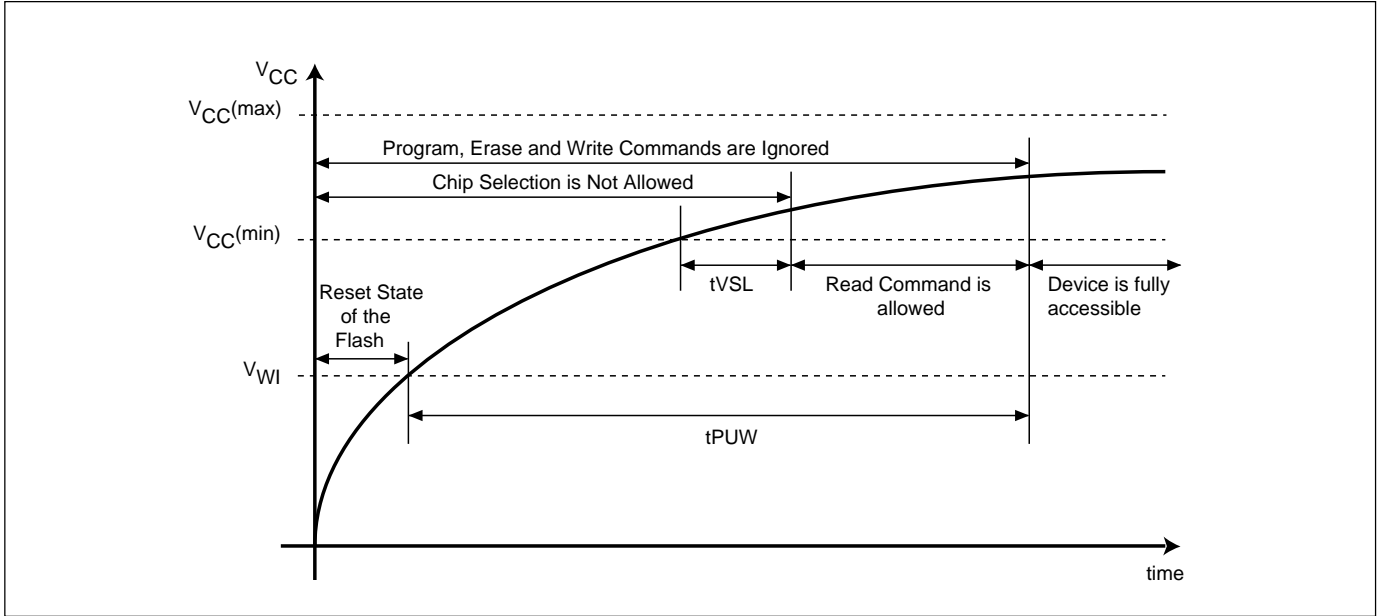
Figure 26. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)



Notes:

- (1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first
- (2) Instruction is 90(hex).

Figure 27. Power-up Timing



RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

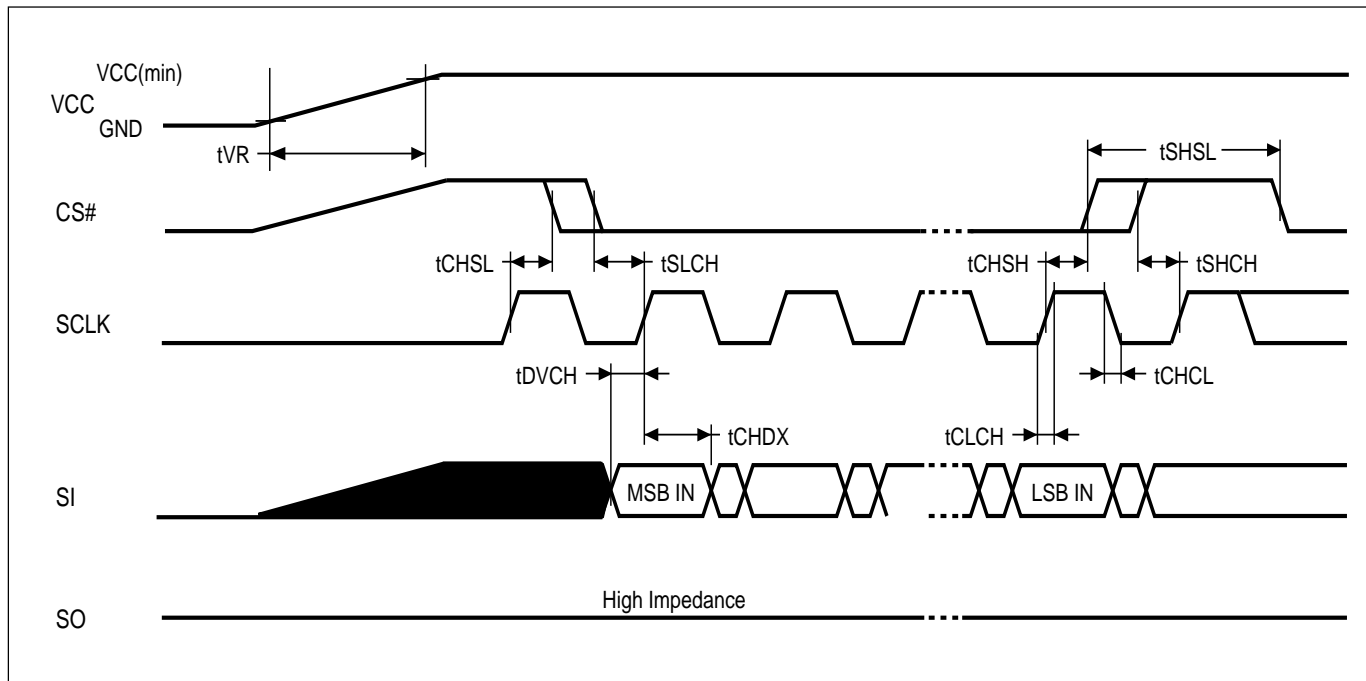


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :

1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	Min.	TYP. (1)	Max. (2)	UNIT
Write Status Register Cycle Time		40	100	ms
Sector Erase Time		60	300	ms
Block Erase Time		0.7	2	s
Chip Erase Time		80	200	s
Chip Erase Time (at ACC mode)		50	125	s
Byte Program Time (via page program command)		9	300	us
Page Program Time		1.4	5	ms
Page Program Time (at ACC mode)		1.4	5	ms
Erase/Program Cycle		100,000		cycles

Note:

1. Typical program and erase time assumes the following conditions: 25° C, 3.3V, and checker board pattern.
2. Under worst conditions of 85° C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0C, VCC=3.0V, and 100K cycle with 90% confidence level.
5. Erase/Program cycles comply with JEDEC JESD-47E & A117A standard.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on ACC	-1.0V	11.5V
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		



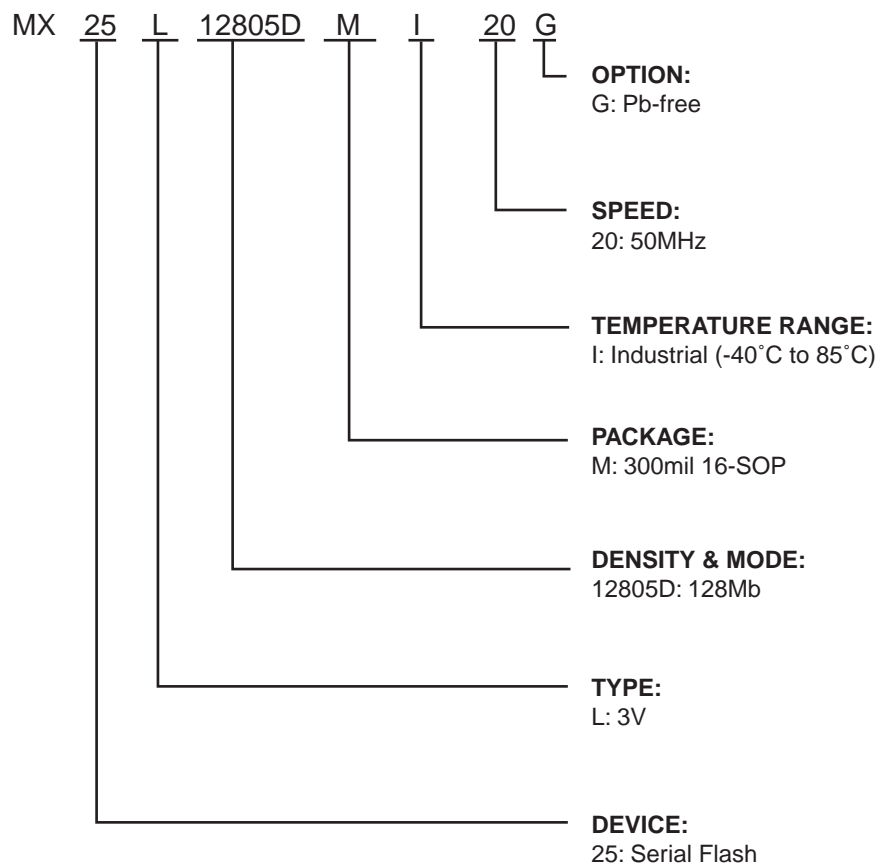
MACRONIX
INTERNATIONAL Co., LTD.

MX25L12805D

ORDERING INFORMATION

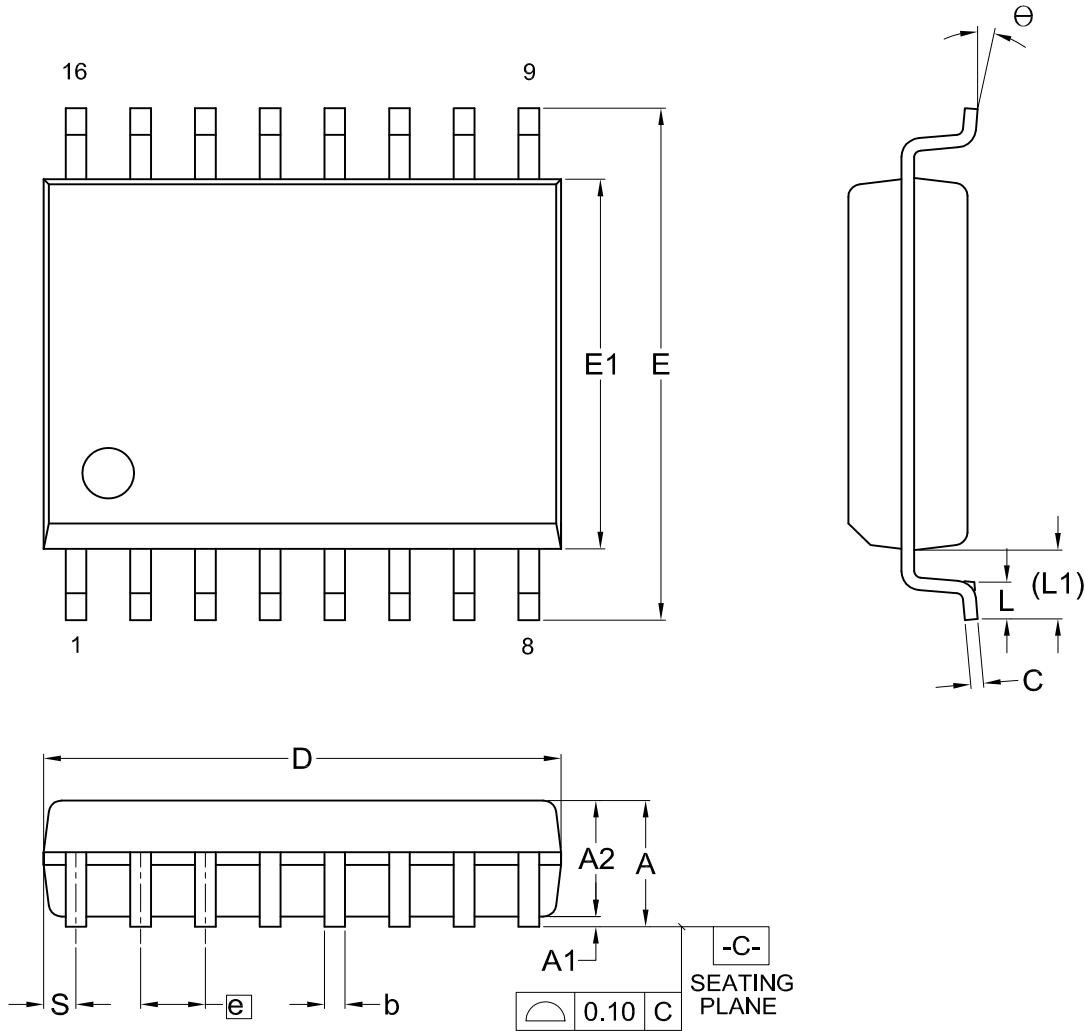
PART NO.	SERIAL CLOCK RATE	READ CURRENT(max.)	STANDBY CURRENT(max.)	Temperature	PACKAGE	Remark
MX25L12805DMI-20G	50MHz	25mA	20uA	-40~85°C	16-SOP	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for SOP 16L (300MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
UNIT														
mm	Min.	---	0.10	2.25	0.36	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0
	Nom.	---	0.20	2.31	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5
	Max.	2.65	0.30	2.40	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8
Inch	Min.	---	0.004	0.089	0.014	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0
	Nom.	---	0.008	0.091	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5
	Max.	0.104	0.012	0.094	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1402	8	MS-013			03-07-'06



REVISION HISTORY

Revision No.	Description	Page	Date
1.0	Removed "Advanced Information" on page 1	P1	FEB/26/2008
1.1	Revised sector erase time spec from 90ms(typ.) to 60ms(typ.)	P24,37	OCT/01/2008

Macronix's products are not designed, manufactured, or intended for use for any high risk applications in which the failure of a single component could cause death, personal injury, severe physical damage, or other substantial harm to persons or property, such as life-support systems, high temperature automotive, medical, aircraft and military application. Macronix and its suppliers will not be liable to you and/or any third party for any claims, injuries or damages that may be incurred due to use of Macronix's products in the prohibited applications.

MACRONIX INTERNATIONAL CO., LTD.

Headquarters

Macronix, Int'l Co., Ltd.
16, Li-Hsin Road, Science Park,
Hsinchu, Taiwan, R.O.C.
Tel: +886-3-5786688
Fax: +886-3-5632888

Macronix America, Inc.

680 North McCarthy Blvd.
Milpitas, CA 95035, U.S.A.
Tel: +1-408-262-8887
Fax: +1-408-262-8810
Email: sales.northamerica@macronix.com

Macronix Asia Limited.

NKF Bldg. 5F, 1-2 Higashida-cho,
Kawasaki-ku Kawasaki-shi,
Kanagawa Pref. 210-0005, Japan
Tel: +81-44-246-9100
Fax: +81-44-246-9105

Macronix (Hong Kong) Co., Limited.

702-703, 7/F, Building 9,
Hong Kong Science Park,
5 Science Park West Avenue, Sha Tin, N.T.
Tel: +86-852-2607-4289
Fax: +86-852-2607-4229

[http : //www.macronix.com](http://www.macronix.com)

Taipei Office

Macronix, Int'l Co., Ltd.
19F, 4, Min-Chuan E. Road, Sec. 3,
Taipei, Taiwan, R.O.C.
Tel: +886-2-2509-3300
Fax: +886-2-2509-2200

Macronix Europe N.V.

Koningin Astridlaan 59, Bus 1
1780 Wemmel Belgium
Tel: +32-2-456-8020
Fax: +32-2-456-8021

Singapore Office

Macronix Pte. Ltd.
1 Marine Parade Central
#11-03 Parkway Centre
Singapore 449408
Tel: +65-6346-5505
Fax: +65-6348-8096