P93U422
HIGH SPEED 256 x 4
STATIC CMOS RAM

FEATURES

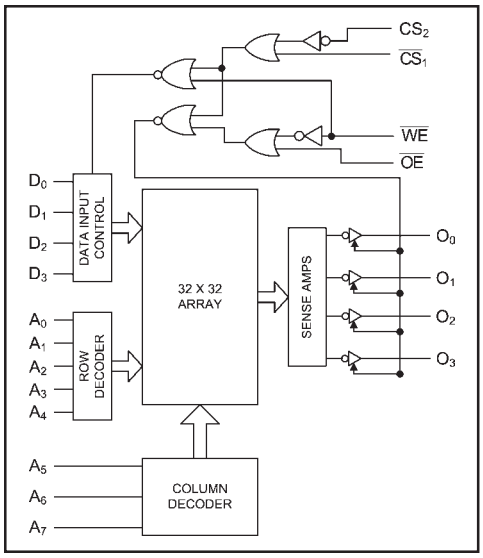
- **Universal 256 x 4 Static RAM**
- **One part, the P93U422, replaces the following bipolar and CMOS parts:**
  - **93422, 93422A**
  - **93L422, 93L422A**
- **Fast Access Time – 35 ns Commercial and Military**
- **Available in the following packages:**
  - **PDIP, CERDIP, Side Brazed DIP**
  - **CERPACK**
  - **LCC**
  - **SOIC**
- **CMOS for Low Power**
  - **440 mW (Commercial)**
  - **495 mW (Military)**
- **5V Power Supply ±10% for both commercial and military temperature ranges**
- **Separate I/O**
- **Fully static operation with equal access and cycle times**
- **Resistant to single event upset and latchup due to advanced process and design improvements**

DESCRIPTION

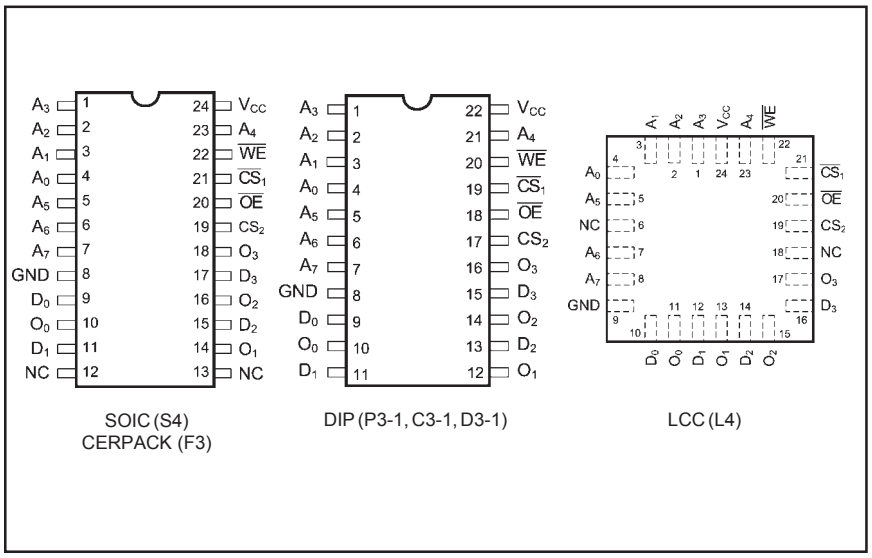
The P93U422 is a 1,024-bit high-speed Static RAM with a 256 x 4 organization. The P93U422 is a universal device designed to replace the entire 93 and 93L 256 x 4 static RAM families. The memory requires no clocks or refreshing and has equal access and cycle times. Inputs and outputs are fully TTL compatible. Operation is from a single 5 Volt supply. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) and active HIGH chip select two (CS_2) as well as 3-state outputs.

In addition to high performance, the device features latch-up protection, single event and upset protection. The P93U422 is offered in several packages: 22-pin 400 mil DIP (plastic and ceramic), 24-pin 300 mil SOIC, 24-pin square LCC and 24-pin CERPACK. Devices are offered in both commercial and military temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	20	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	Gnd	Vcc
Commercial	0°C to 70°C	0V	5.0V ±10%
Military	–55°C to 125°C	0V	5.0V ±10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P93U422 Min.	P93U422 Max.	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = –5.2 mA		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8.0 mA			0.45	V
V_{IH}	Input High Level			2.1		V
V_{IL}	Input Low Level				0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.40 V			–300	µA
I_{IH}	Input High Current	V_{CC} = Max, V_{IN} = 4.5V			40	µA
I_{SC}	Output Short Circuit Current [3]	V_{CC} = Max., V_{OUT} = 0.0V			–70	mA
I_{CC}	Power Supply Current	All Inputs = GND V_{CC} = Max.	T_A = 125°C		70	mA
			T_A = 75°C		70	
			T_A = 0°C		80	
			T_A = –55°C		90	
V_{CL}	Input Clamp Voltage	I_{IN} = –10mA			–1.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4V, V_{CC} = Max.			50	µA
		V_{OUT} = 0.5V, V_{CC} = Max.		–50		

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

An active LOW write enable ($\overline{WE}$) controls the writing/reading operation of the memory. When chip select one ($\overline{CS_1}$) and write enable ($\overline{WE}$) are LOW and chip select two (CS_2) is HIGH, the information on data inputs (D_0 through D_3) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch." Reading is performed with chip selct one ($\overline{CS_1}$) LOW, chip select two (CS_2) HIGH, write enable ($\overline{WE}$) HIGH and output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the noninverting outputs (O_0 through O_3). The outputs of the memory go to an inactive high impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, or during the write operation when write enable ($\overline{WE}$) is LOW.

TRUTH TABLE

Mode	CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	Output
Standby	L	X	X	X	High Z
Standby	X	H	X	X	High Z
D_{OUT} Disabled	H	L	X	H	High Z
Read	H	L	H	L	D_{OUT}
Write	H	L	L	X	High Z

Notes: H = HIGH
L = Low
X = Don't Care
HIGH Z = Implies outputs are disabled or off. This condition is defined as high impedance state for the P93U422.

SWITCHING CHARACTERISTICS (5,6)

Over Operating Range (Commercial and Military)

Parameters	Description	P93U422		Unit
		Min.	Max.	
$t_{PLH(A)}$ (7) $t_{PLH(A)}$ (7)	Delay from Address to Output (Address Access Time) (See Fig. 2)		35	ns
t_{PZH} ($\overline{CS_1}$, CS_2) (8) t_{PZL} ($\overline{CS_1}$, CS_2) (8)	Delay from Chip Select to Active Output and Correct Data (See Fig. 2)		25	ns
t_{PZH} ($\overline{WE}$) (8) t_{PZL} ($\overline{WE}$) (8)	Delay from Write Enable to Active Output and Correct Data (Write Recovery) (See Fig. 1)		25	ns
t_{PZH} ($\overline{OE}$) (8) t_{PZL} ($\overline{OE}$) (8)	Delay from Output Enable to Active Output and Correct Data (See Fig. 2)		25	ns
t_S(A)	Setup Time Address (Prior to Initiation of Write) (See Fig. 1)	5		ns
t_h(A)	Hold Time Address (After Termination of Write) (See Fig. 1)	5		ns
t_S(DI)	Setup Time Data Input (Prior to Initiation of Write) (See Fig. 1)	5		ns
t_h(DI)	Hold Time Data Input (After Termination of Write) (See Fig. 1)	5		ns
t_S ($\overline{CS_1}$, CS_2)	Setup Time Chip Select (Prior to Initiation of Write) (See Fig. 1)	5		ns
t_h ($\overline{CS_1}$, CS_2)	Hold Time Chip Select (After Termination of Write) (See Fig. 1)	5		ns
t_{pw}($\overline{WE}$)	Minimum Write Enable Pulse Width (to Insure Write) (See Fig. 1)	20		ns
t_{PHZ} ($\overline{CS_1}$, CS_2) (8) t_{PLZ} ($\overline{CS_1}$, CS_2) (8)	Delay from Chip Select to Inactive Output (HIGH Z) (See Fig. 2)		30	ns
t_{PHZ} ($\overline{WE}$) (8) t_{PLZ} ($\overline{WE}$) (8)	Delay from Write Enable to Inactive Output (HIGH Z) (See Fig. 1)		30	ns
t_{PHZ} ($\overline{OE}$) (8) t_{PLZ} ($\overline{OE}$) (8)	Delay from Output Enable to Inactive Output (HIGH Z) (See Fig. 2)		30	ns

Notes:

5) Test conditions assume signal transition times of 10 ns or less.

6) Extended temperature operation guaranteed with 400 linear feet per minute of air flow.

7) $t_{PLH}^{(A)}$ and $t_{PHL}^{(A)}$ are tested with S_1 closed and C_L = 15 pF with both input and output timing referenced to 1.5V

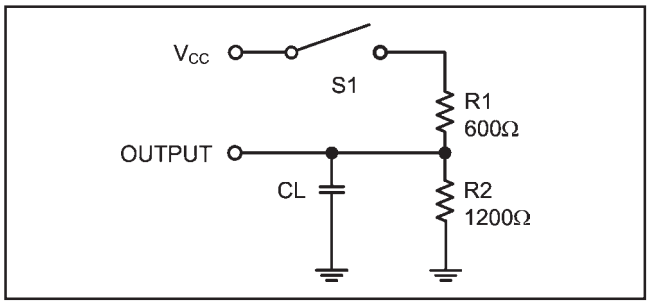
8) $t_{PZH}(\overline{WE})$, $t_{PZH}(\overline{CS_1}, CS_2)$ and $t_{PZH}(\overline{OE})$ are measured with S_1 open, C_L = 15 pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}, CS_2)$ and $t_{PZL}(\overline{OE})$ are measured with S_1 closed, C_L = 15pF and with both the input and output timing referenced to 1.5V.

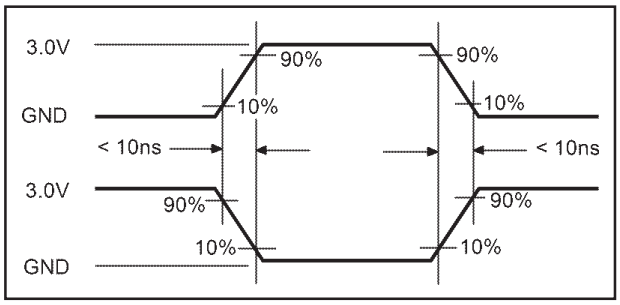
$t_{PHZ}(\overline{WE})$, $t_{PHZ}(\overline{CS_1}, CS_2)$ and $t_{PHZ}(\overline{OE})$ are measured with S_1 open, C_L < 5pF and are measured between the 1.5V level on the input to the V_{OH} -500mV level on the output.

$t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$ and $t_{PLZ}(\overline{OE})$ are measured with S_1 closed, C_L < 5pF and are measured between the 1.5V level on the input to the V_{OL} +500mV level on the output.

SWITCHING TEST

Test Circuits (7, 8)





KEY TO DIAGRAM

Waveform	Inputs	Outputs
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H

Waveform	Inputs	Outputs
	Don't care; any change permitted	Changing; state unknown
	Does not apply	Center line is high impedence "off" state

SWITCHING WAVEFORMS

Write Mode (with $\overline{OE}$ = LOW)

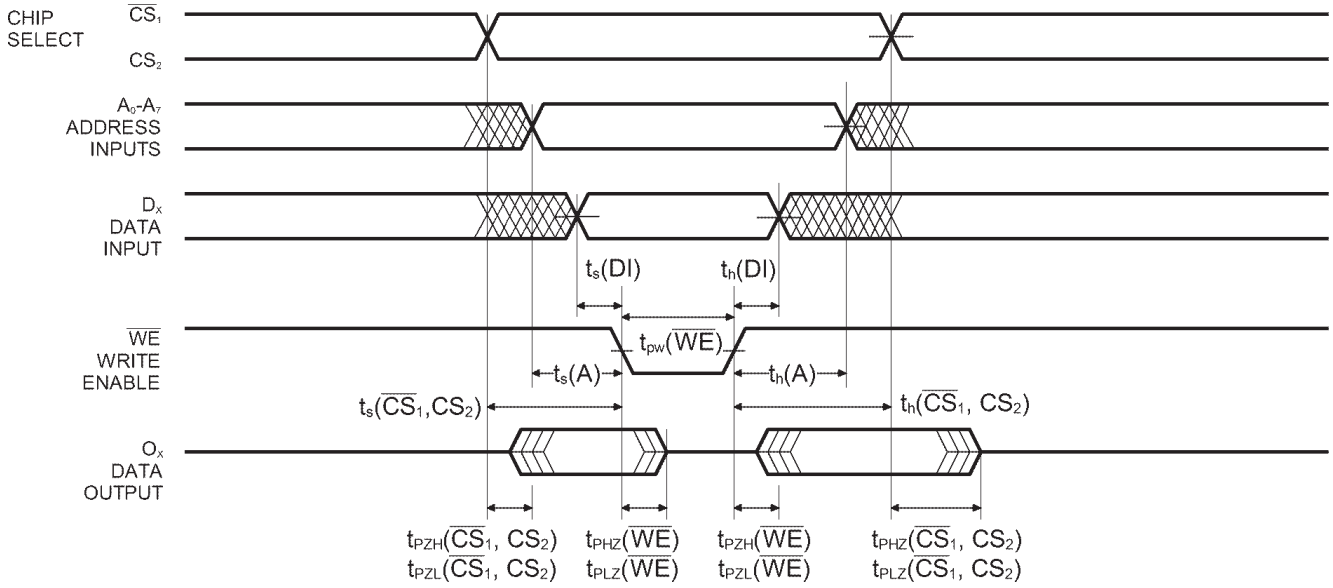


Figure 1.

Read Mode

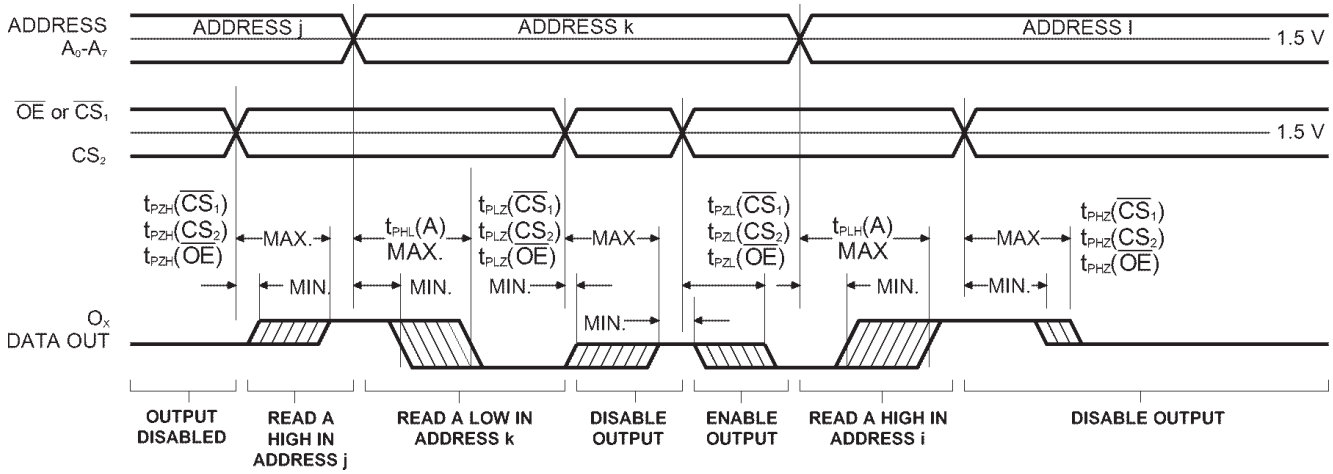
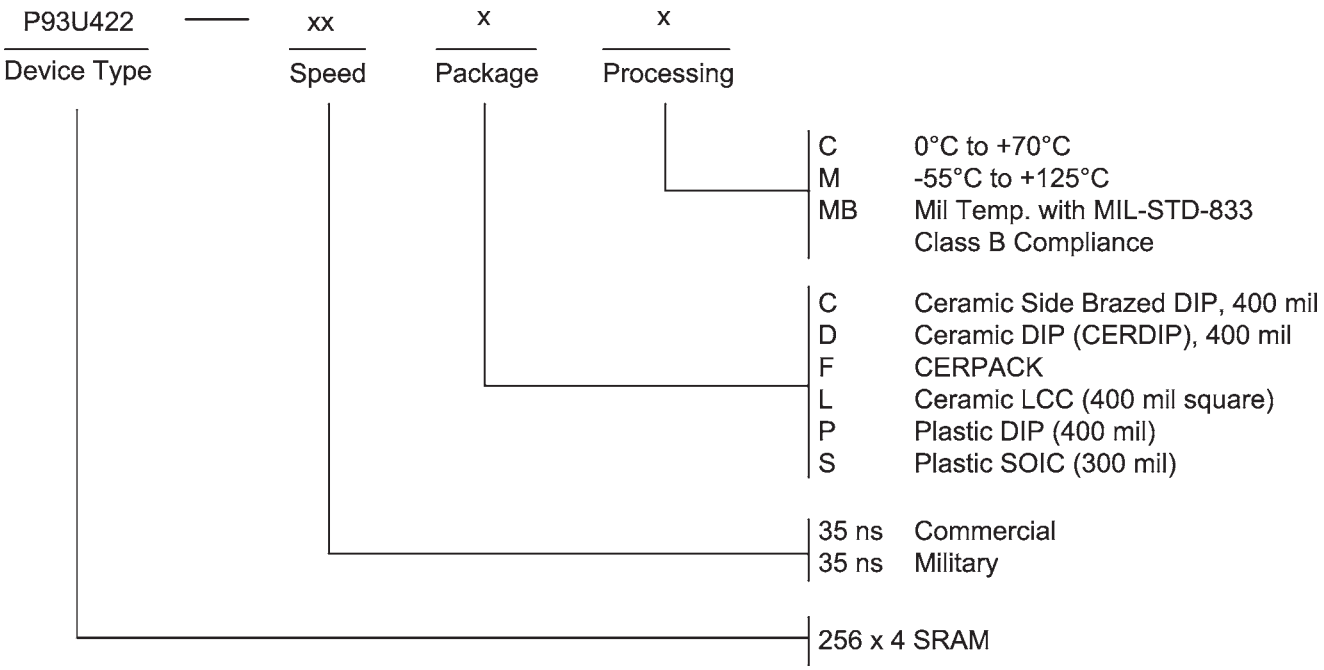


Figure 2.

ORDERING INFORMATION



SELECTION GUIDE

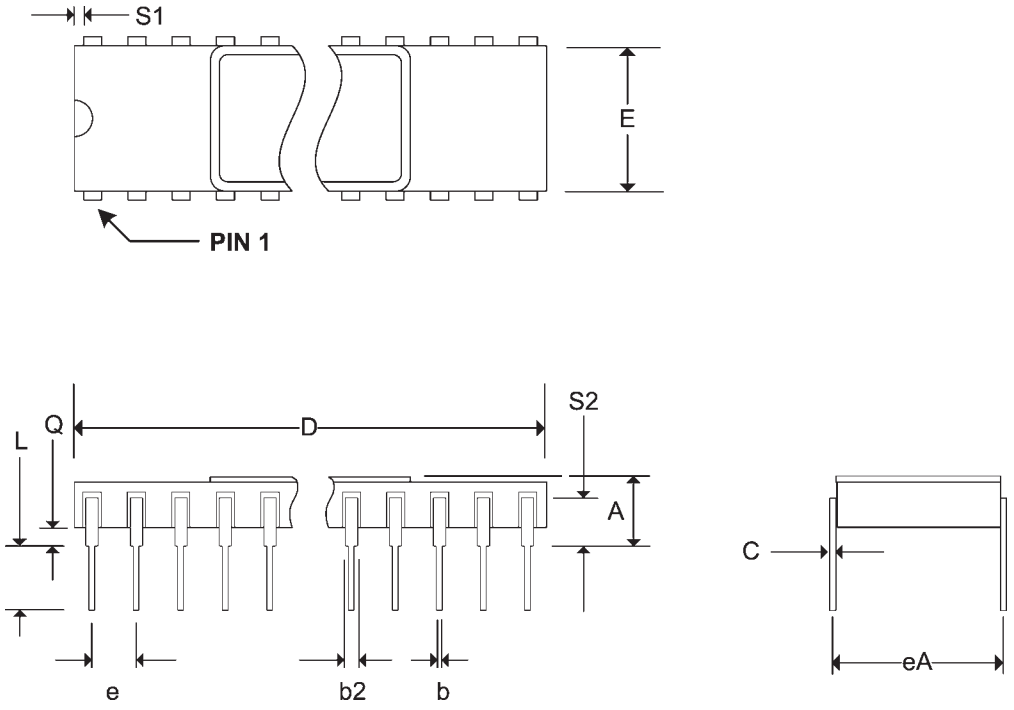
The P93U422 is available in the following temperature range, speed, and package options.

Temperature Range	Package	Speed (ns)
		35
Commercial Temperature	Plastic DIP	-35PC
	Plastic SOIC	-35SC
Military Temperature	Side Brazed DIP	-35CM
	CERDIP	-35DM
	CERPACK	-35FM
	LCC	-35LM
Military Processed*	Side Brazed DIP	-35CMB
	CERDIP	-35DMB
	CERPACK	-35FMB
	LCC	-35LMB

*Military temperature range with MIL-STD-883, Class B processing.

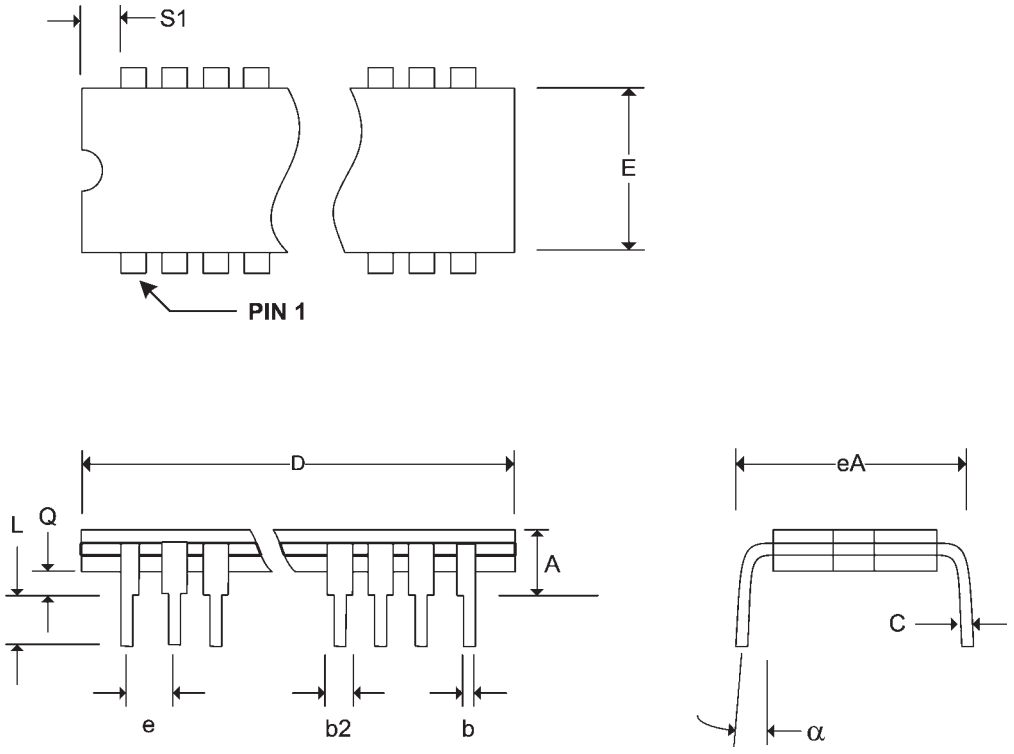
Pkg #	C3-1	
# Pins	22 (400 Mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.035	0.060
C	0.008	0.015
D	-	1.100
E	0.360	0.410
eA	0.400 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDE BRAZED DUAL IN-LINE PACKAGE



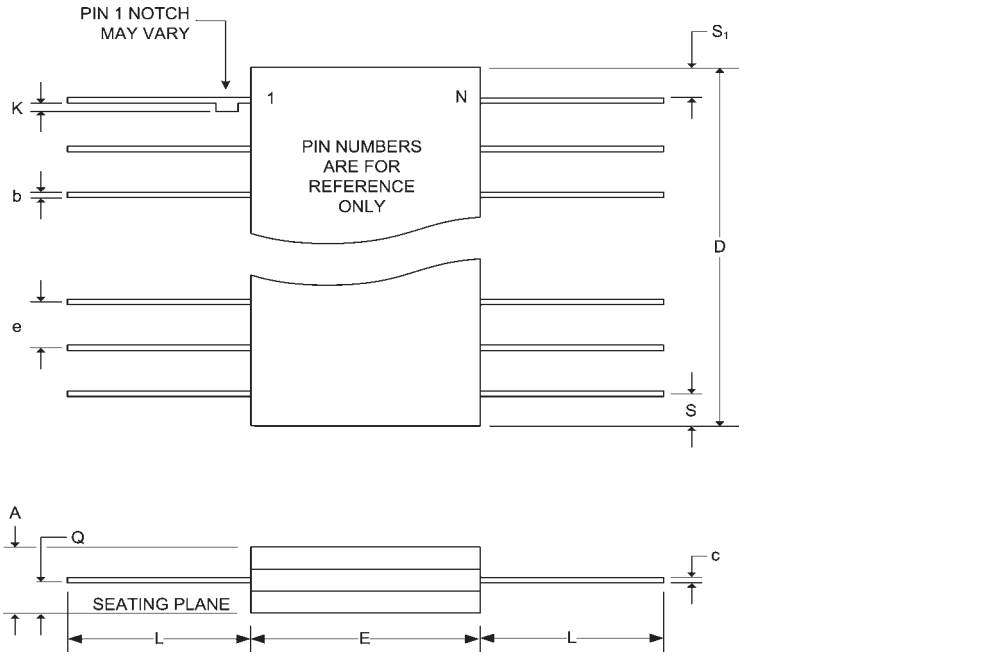
Pkg #	D3-1	
# Pins	22 (400 Mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.111
E	0.350	0.410
eA	0.400 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
α	0°	15°

CERDIP DUAL IN-LINE PACKAGE



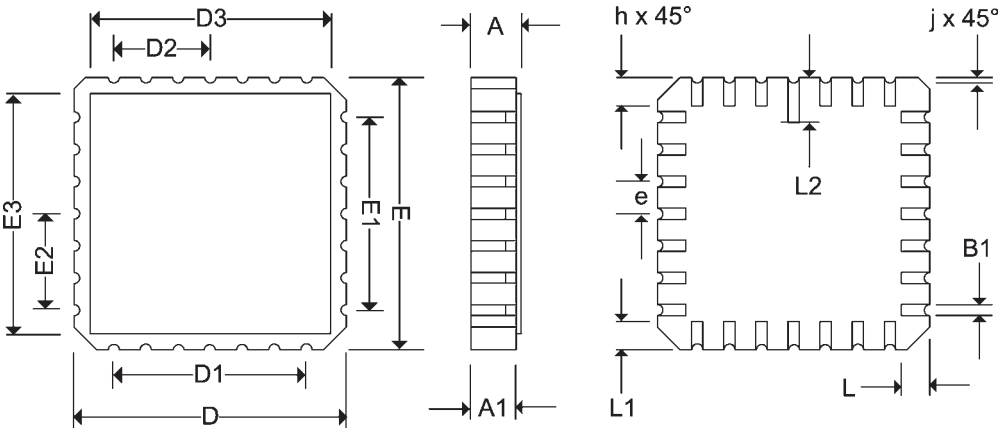
Pkg #	F3	
# Pins	24	
Symbol	**Min**	**Max**
A	0.060	0.090
b	0.015	0.022
c	0.004	0.009
D	-	0.630
E	0.330	0.380
e	0.050 BSC	
k	0.008	0.015
L	0.250	0.370
Q	0.026	0.045
S	-	0.085
S1	0.005	-

CERPACK CERAMIC FLAT PACKAGE



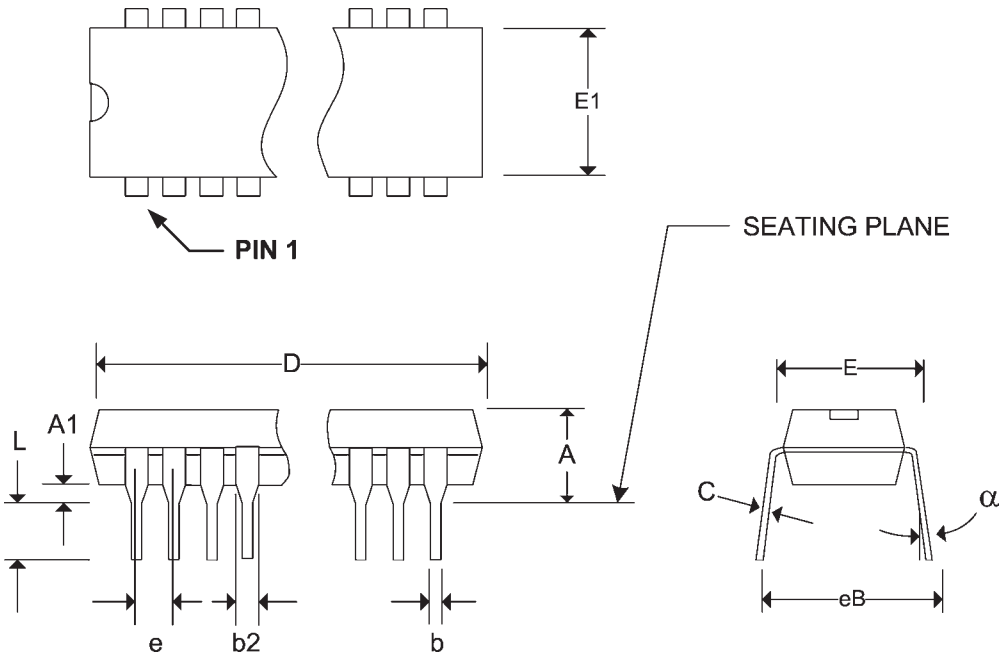
Pkg #	L4	
# Pins	24	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D/E	0.395	0.410
D1/E1	0.250 BSC	
D2/E2	0.125 BSC	
D3/E3	-	0.410
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	6	
NE	6	

SQUARE LEADLESS CHIP CARRIER



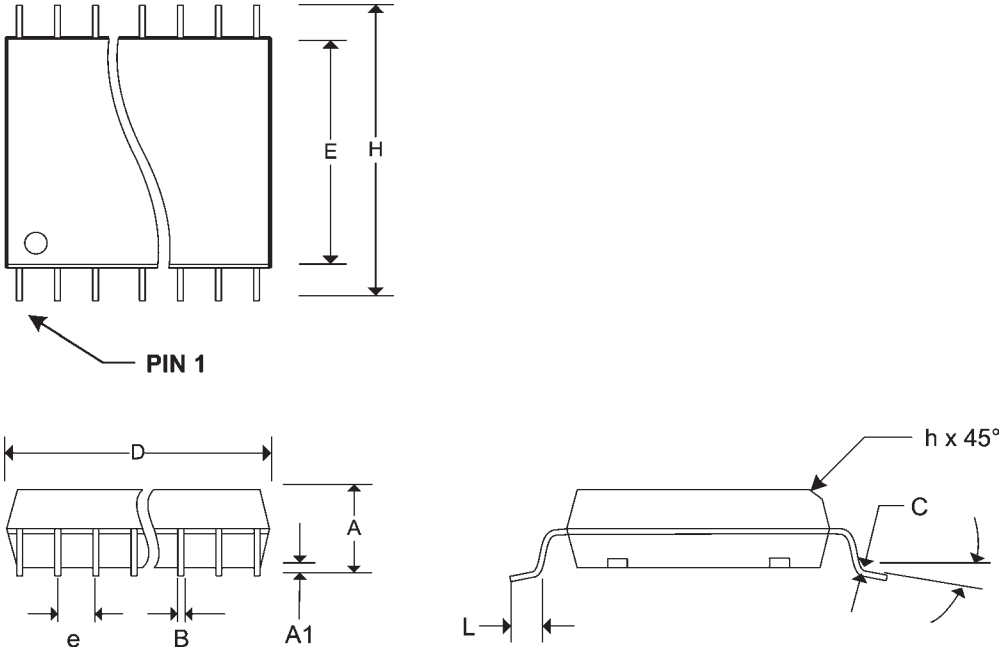
Pkg #	P3-1	
# Pins	22 (400 Mil)	
Symbol	**Min**	**Max**
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.065
C	0.009	0.015
D	1.065	1.120
E1	0.330	0.390
E	0.390	0.425
e	0.100 BSC	
eB	-	0.500
L	0.115	0.160
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE



Pkg #	S4	
# Pins	24 (300 Mil)	
Symbol	**Min**	**Max**
A	0.093	0.104
A1	0.004	0.012
b2	0.013	0.020
C	0.009	0.012
D	0.598	0.614
e	0.050 BSC	
E	0.291	0.299
H	0.394	0.419
h	0.010	0.029
L	0.016	0.050
α	0°	8°

SMALL OUTLINE IC PLASTIC PACKAGE



REVISIONS

DOCUMENT NUMBER:	SRAM102
DOCUMENT TITLE:	P93U422 HIGH SPEED 256 x 4 STATIC CMOS RAM

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
ORIG	1997	DAB	New Data Sheet
A	Oct-05	JDB	Change logo to Pyramid