AKD5381-B
AK5381 Evaluation Board Rev.1

GENERAL DESCRIPTION

AKD5381-B is an evaluation board for the digital audio 24bit 96kHz A/D converter, AK5381. AKD5381-B has analog input circuits and a digital interface transmitter,and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD5381-B --- AK5381 Evaluation Board

FUNCTION

- **DIT (AK4114) with optical output**

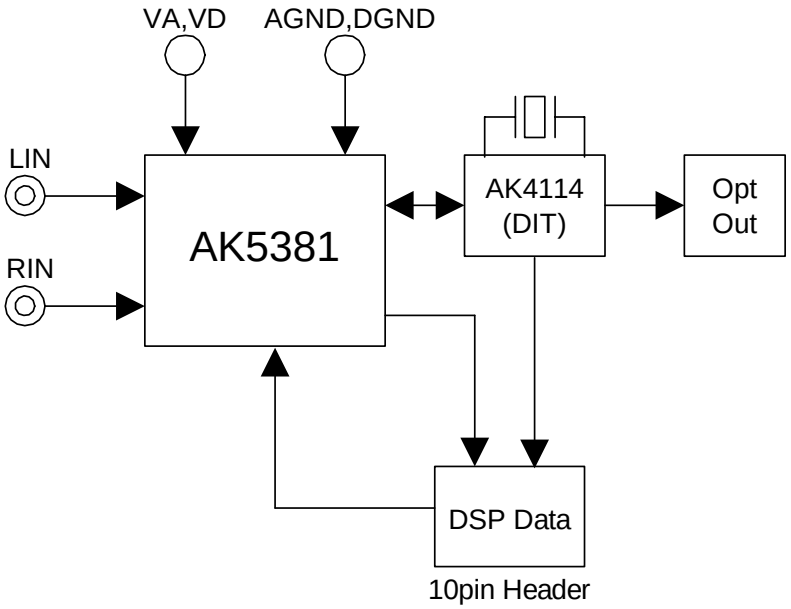


Figure 1. AKD5381-B Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

1. Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

[VA]	(red)	= 2.7 ~ 5.5V or +15V	: for VA of AK5381 (typ. 5.0V)
[VD]	(orange)	= 2.7 ~ 5.5V	: for VD of AK5381, 74HC14 (typ. 5.0V)
[VCC]	(red)	= 3.3V	: for AK4114
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.

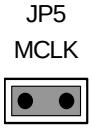
The AK5381 and AK4114 should be reset once bringing SW2 = "L" upon power-up.

■ Evaluation mode

(1) Slave Mode

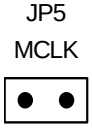
(1-1) A/D evaluation using DIT function of AK4114

PORT2 (DIT) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX141). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier, which equips DIR input. Nothing should be connected to PORT1 (DSP).



(1-2) All interface signals including master clock are fed externally.

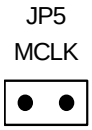
PORT1 (DSP) is used. All interface signals (MCLK, SCLK, LRCK) are provided to the AK5381 through PORT1. JP5 (MCLK) should be open. The DIF1 of SW1 (MODE) should be set to "H".



(2) Master Mode

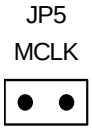
(2-1) A/D evaluation using DIT function of AK4114

PORT2 (DIT) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX141). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier, which equips DIR input. Nothing should be connected to PORT1 (DSP). The DIF1 of SW1 (MODE) should be set to "H".



(2-2) Master clock is fed externally.

PORT1 (DSP) is used. MCLK is provided to the AK5381 through PORT1. JP5 (MCLK) should be open. The DIF1 of SW1 (MODE) should be set to "H".



■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
   OPEN : Separated.
   SHORT : Common. (The connector "DGND" can be open.) <Default>

2. JP2 (CKS1) : Setting of CKS1 pin for AK5381
   H : Master mode
   L : Slave mode <Default>

3. JP3 (VA) : Select VA for AK5381
   VA : Supply from VA connector <Default>
   REG : Supply from regulator. VA connector should be supplied +15V.

4. JP4 (VD) : Select VD for AK5381
   VA : Supply from VA connector
   VD : Supply from VD connector <Default>

■ DIP Switch set up

[SW1] (MODE1): Setting the evaluation mode for AK5381 and AK4114
ON is "H", OFF is "L". CKS1 should be set by JP2.

No.	Name	OFF ("L")	ON ("H")
1	CKS0	See Table 2	
2	CKS2		
3	DIF	MSB justified	I^2S Compatible
4	DIF1	AK4114 Master mode	AK4114 Slave mode

Table 1. Mode Setting

CKS2	CKS1	CKS0	Input Level	HPF	Master/Slave	MCLK	SCLK
L	L	L	CMOS	ON	Slave	256/384/512/768fs	≥ 48fs or 32fs
L	L	H	CMOS	OFF	Slave	256/384/512/768fs	≥ 48fs or 32fs
L	H	L	CMOS	ON	Master	256fs (~ 96kHz)	64fs
L	H	H	CMOS	ON	Master	512fs (~ 48kHz)	64fs
H	L	L	TTL	ON	Slave	256/384/512/768fs	≥ 48fs or 32fs
H	L	H	Reserved				
H	H	L	CMOS	ON	Master	384fs (~ 96kHz)	64fs
H	H	H	CMOS	ON	Master	768fs (~ 48kHz)	64fs

Table 2. Mode Setting of AK5381

Note: AK4114 does not support MCLK=384fs/512fs/768fs.
PORT1 (DSP) should be used when MCLK=384fs/512fs/768fs.

■ The function of the toggle SW

Upper-side is "H" and lower-side is "L".

[SW2] (PDN): Resets the AK5381 and AK4114. Keep "H" during normal operation.

■ Analog Input Circuits

Analog signal is input via J1(RIN) and J2(LIN) of RCA connectors.

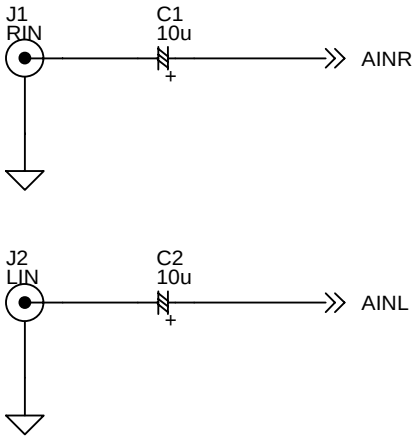


Figure 2. Analog Input circuits

* AKM assumes no responsibility for the trouble when using the circuit examples.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit: Audio Precision, System Two Cascade
- MCLK : 256fs
- SCLK : 64fs
- fs : 48kHz, 96kHz
- Bit : 24bit
- Power Supply : VA = VD = 5.0V (Using regulator)
- Interface : DIT
- Temperature : Room

Parameter		Result (Lch / Rch)	Unit
ADC Analog Input Characteristics:			
S/(N+D) (–1dB Input)	fs=48kHz	89.0 / 88.4	dB
	fs=96kHz	86.9 / 86.2	dB
D-Range (–60dB Input)	fs=48kHz, A-weighted	102.7 / 102.4	dB
	fs=96kHz	99.2 / 99.2	dB
S/N	fs=48kHz, A-weighted	102.8 / 102.8	dB
	fs=96kHz	99.4 / 99.4	dB
Interchannel Isolation		123.6 / 123.8	dB

[ADC Plot : fs=48kHz]

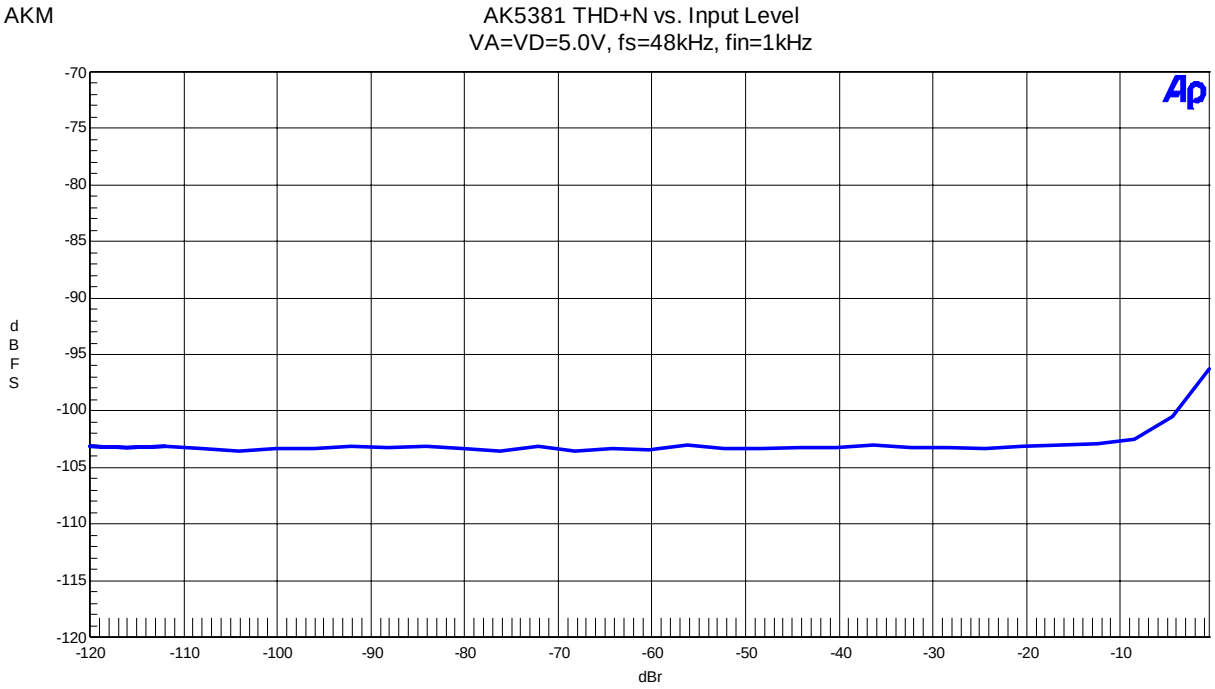


Figure 1. THD+N vs. Input Level

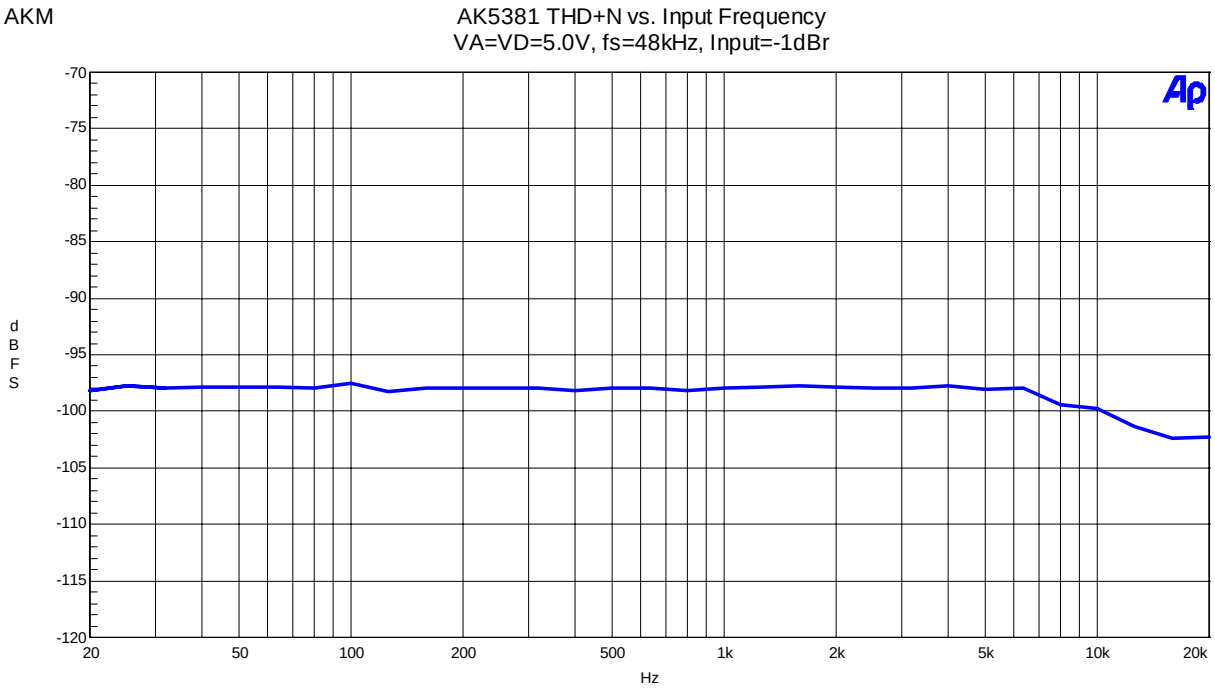


Figure 2. THD+N vs. Input Frequency

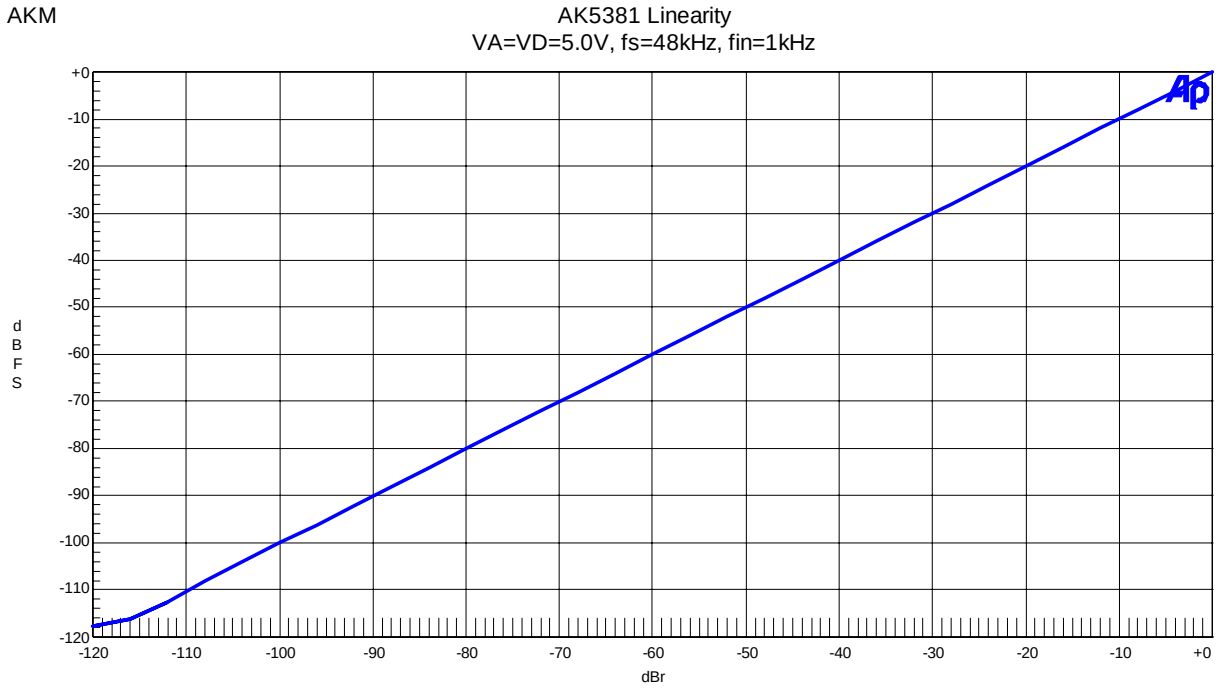


Figure 3. Linearity

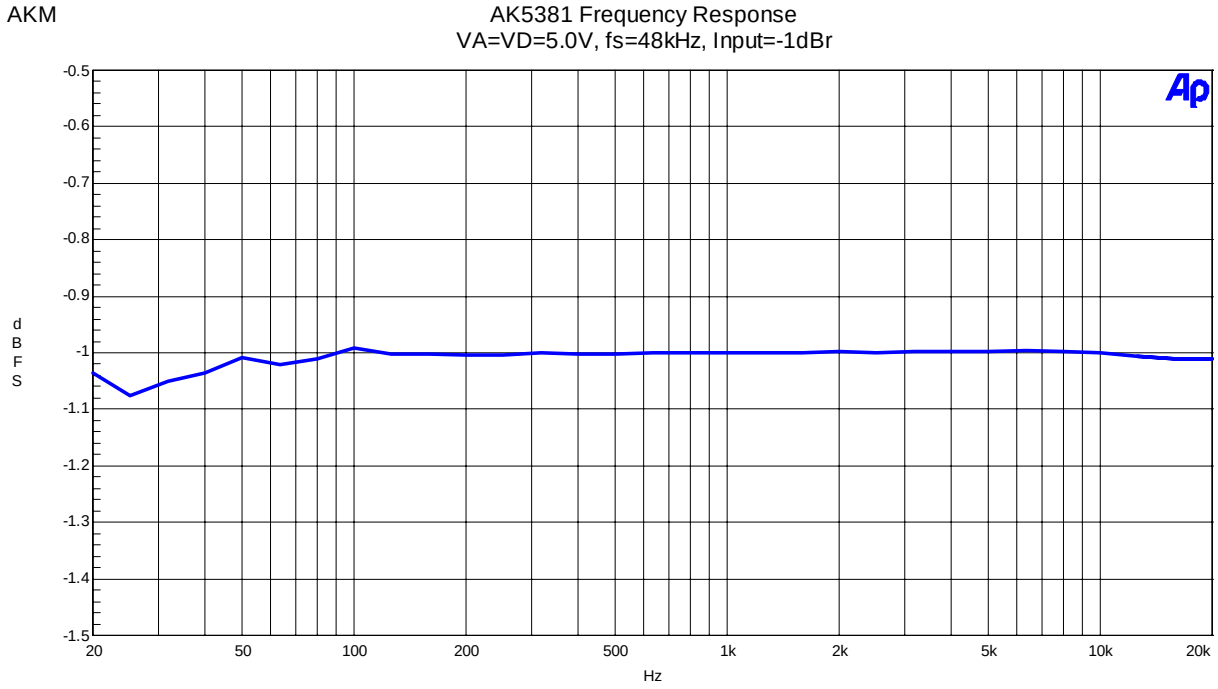


Figure 4. Frequency Response

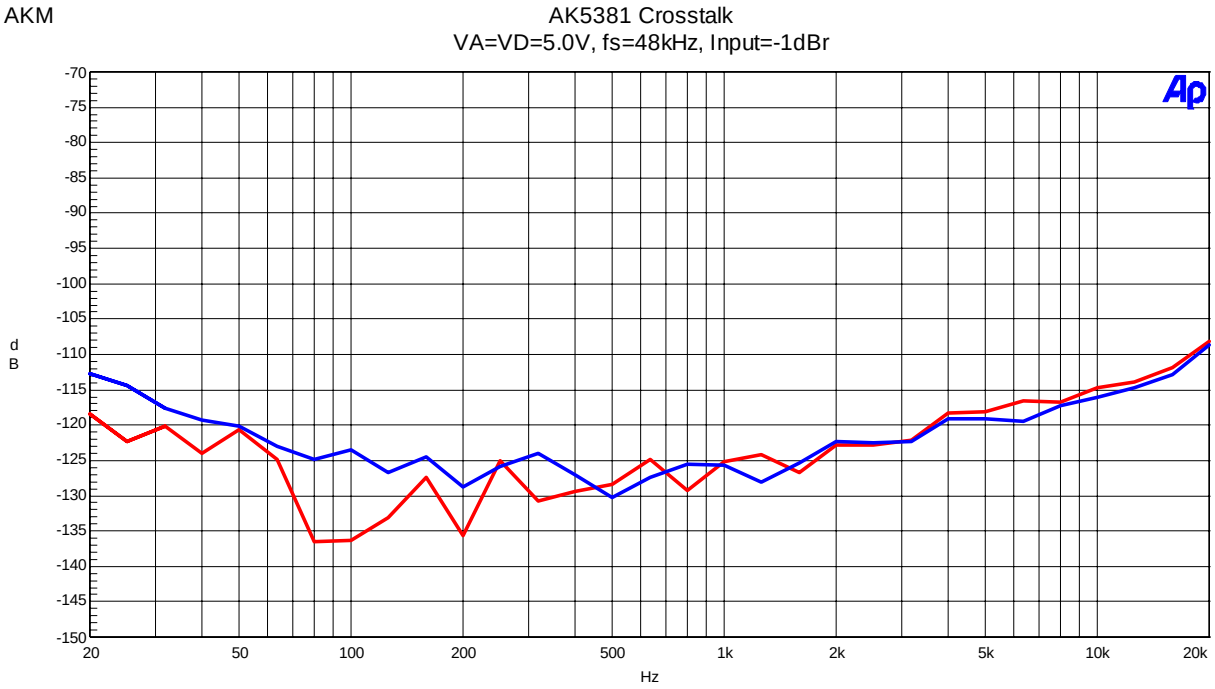


Figure 5. Crosstalk

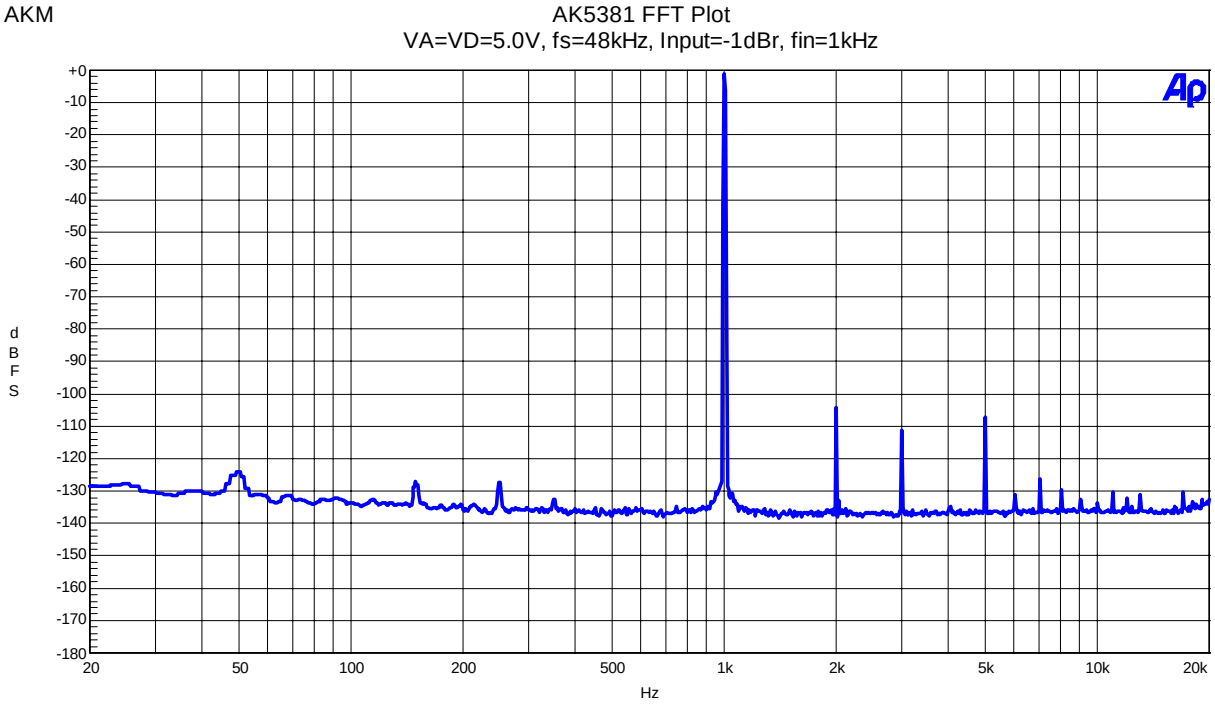


Figure 6. FFT Plot

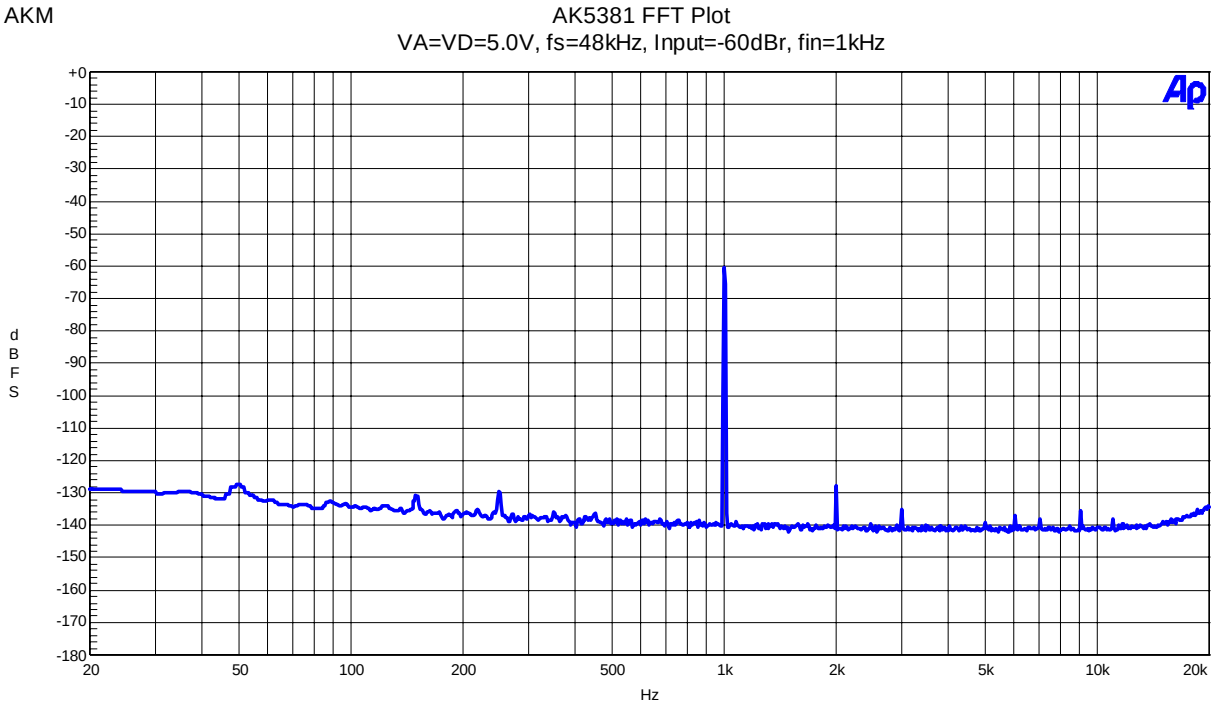


Figure 7. FFT Plot

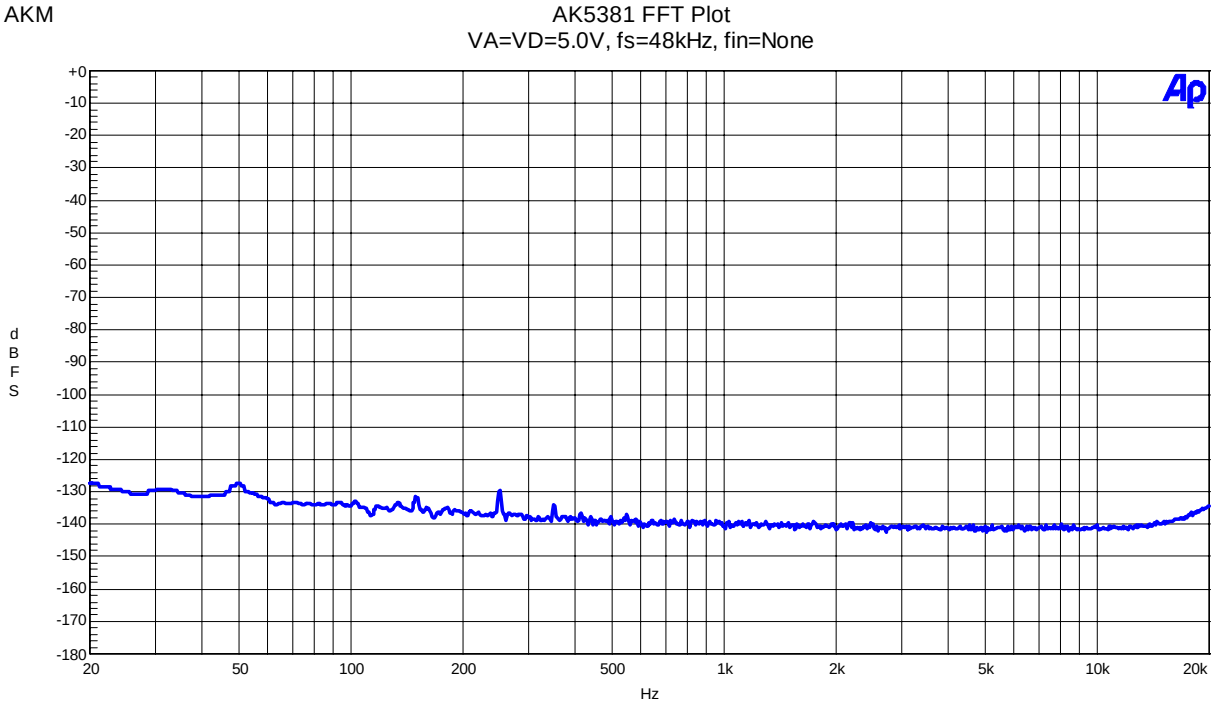


Figure 8. FFT Plot

[ADC Plot : fs=96kHz]

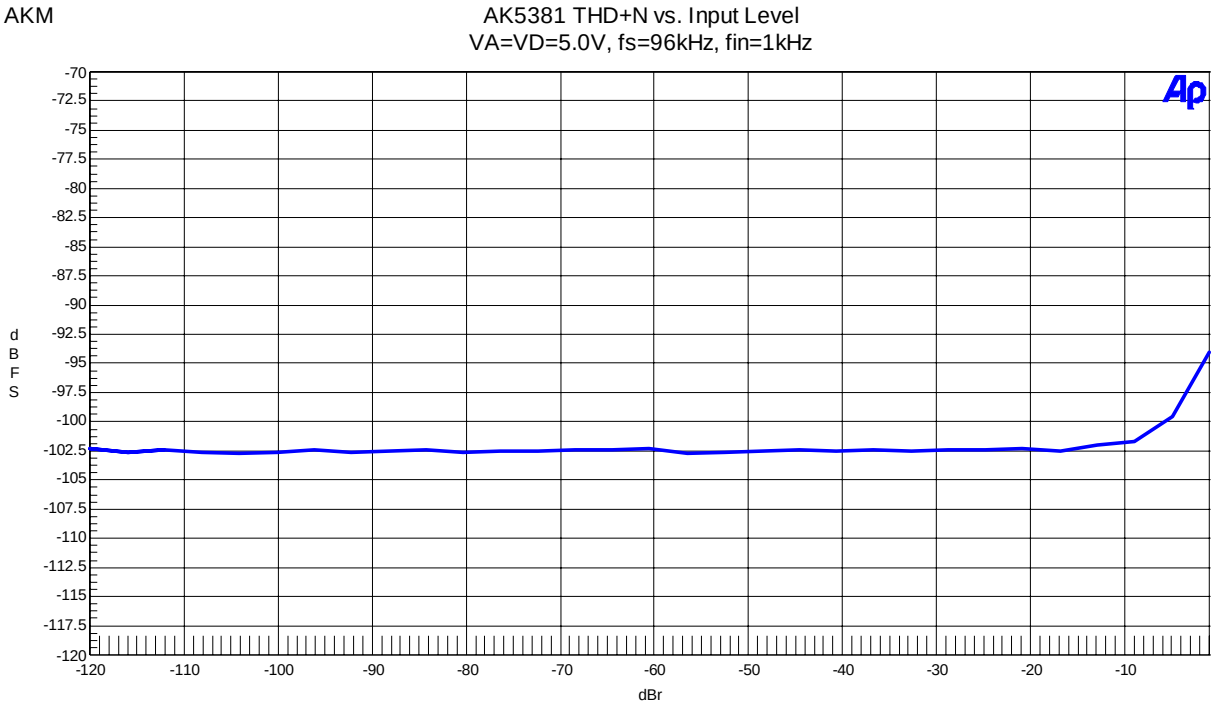


Figure 9. THD+N vs. Input Level

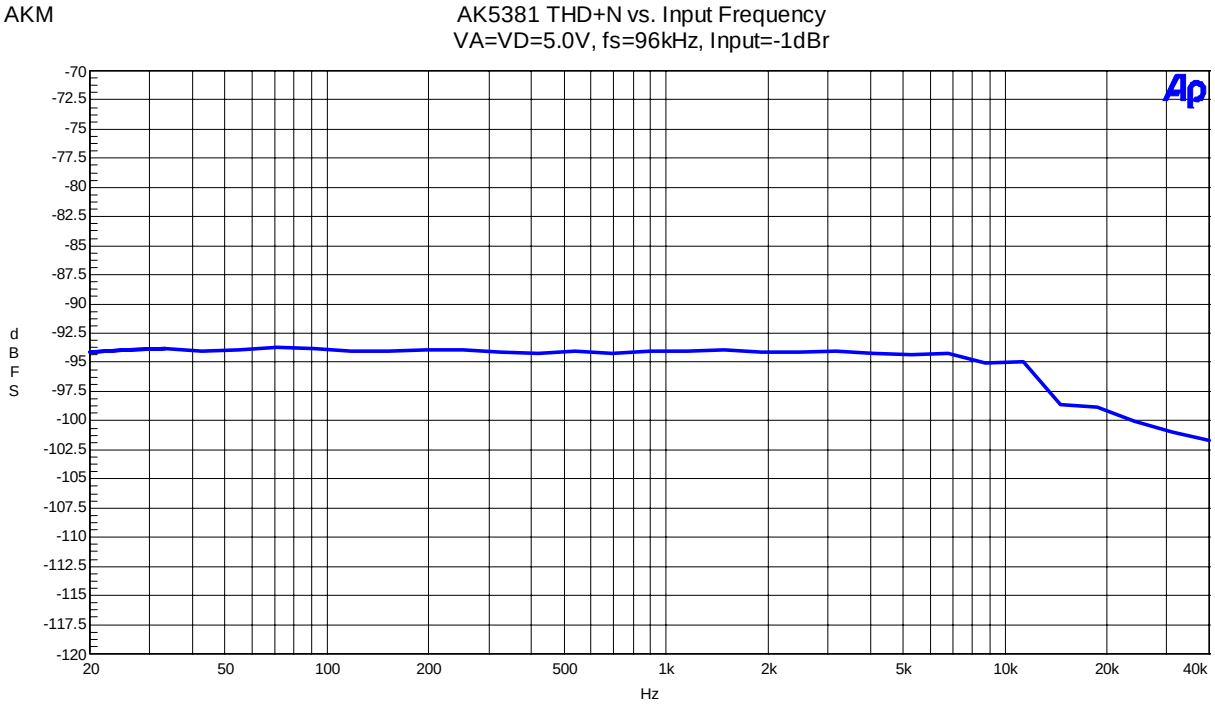


Figure 10. THD+N vs. Input Frequency

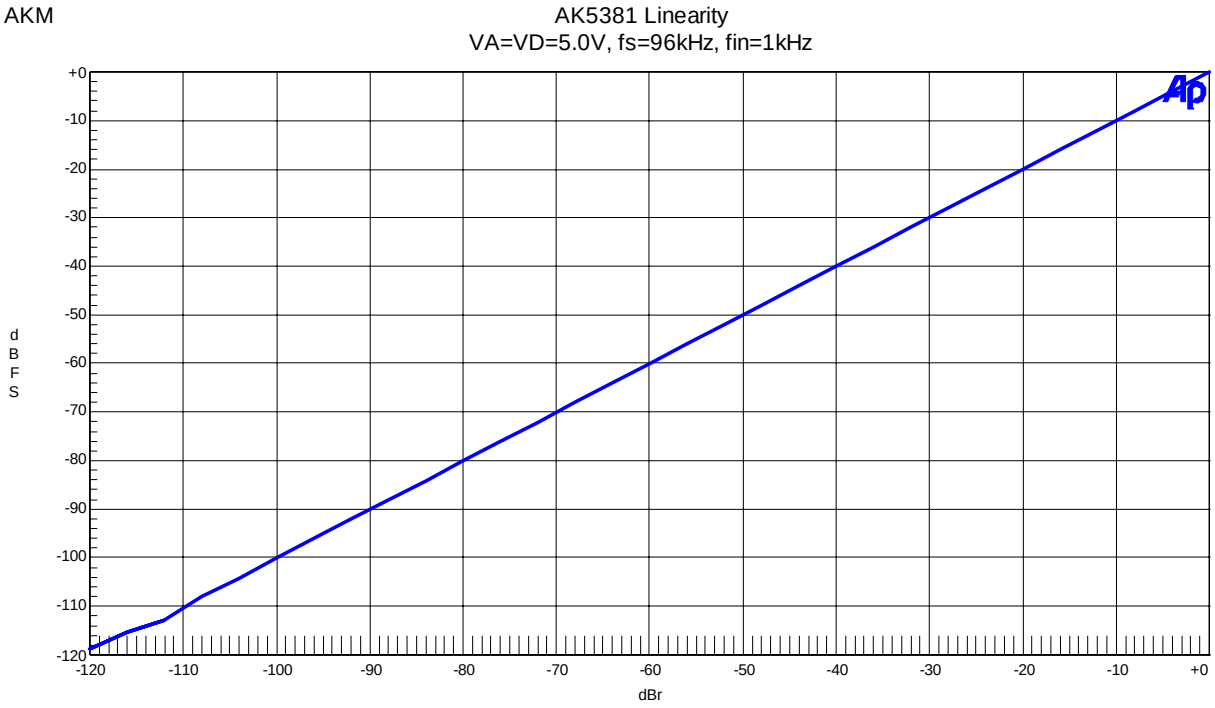


Figure 11. Linearity

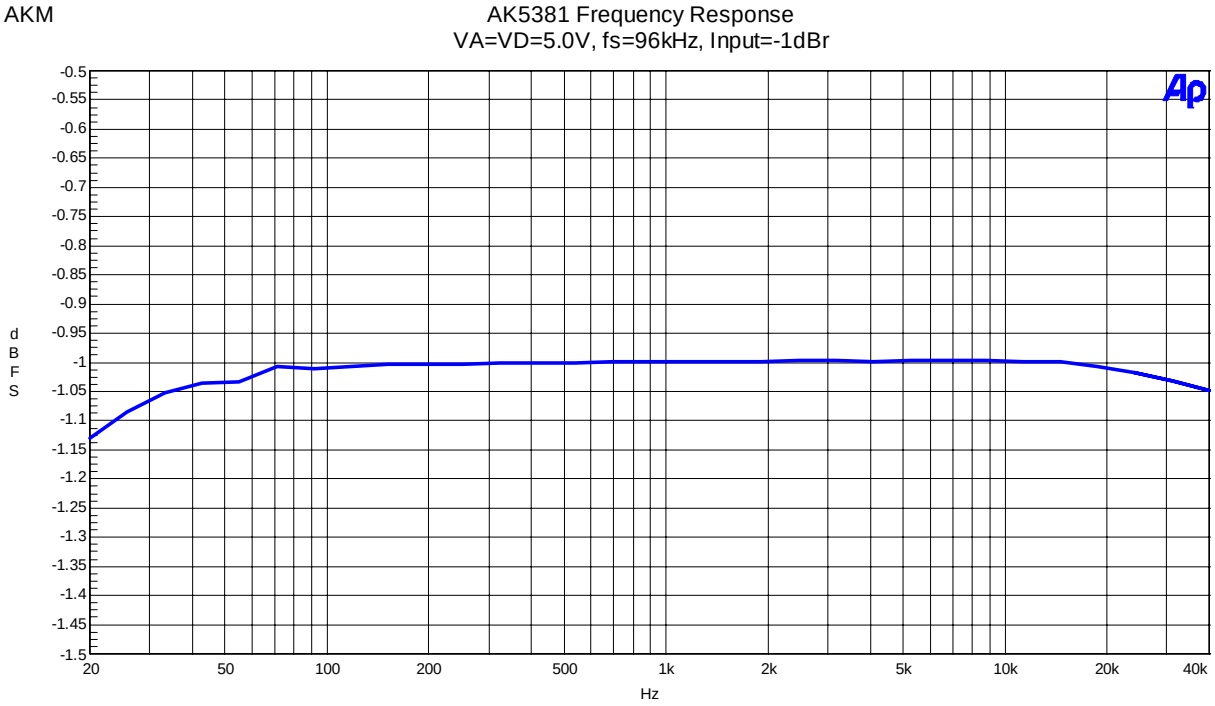


Figure 12. Frequency Response

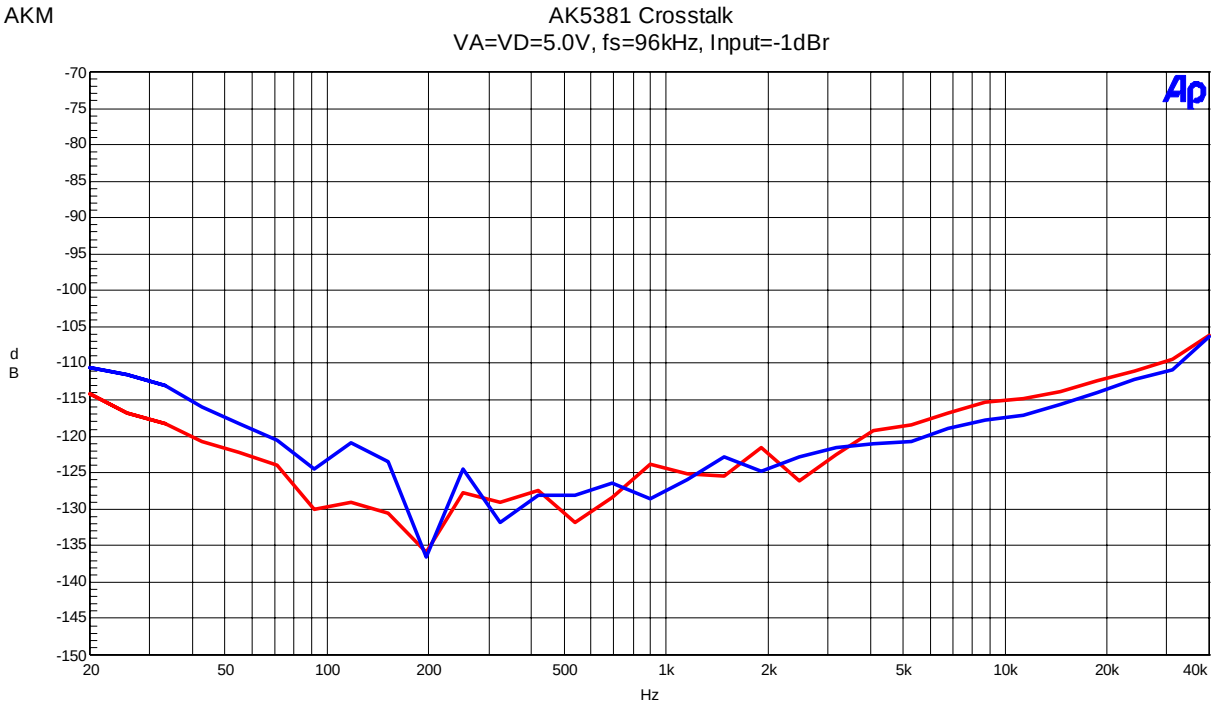


Figure 13. Crosstalk

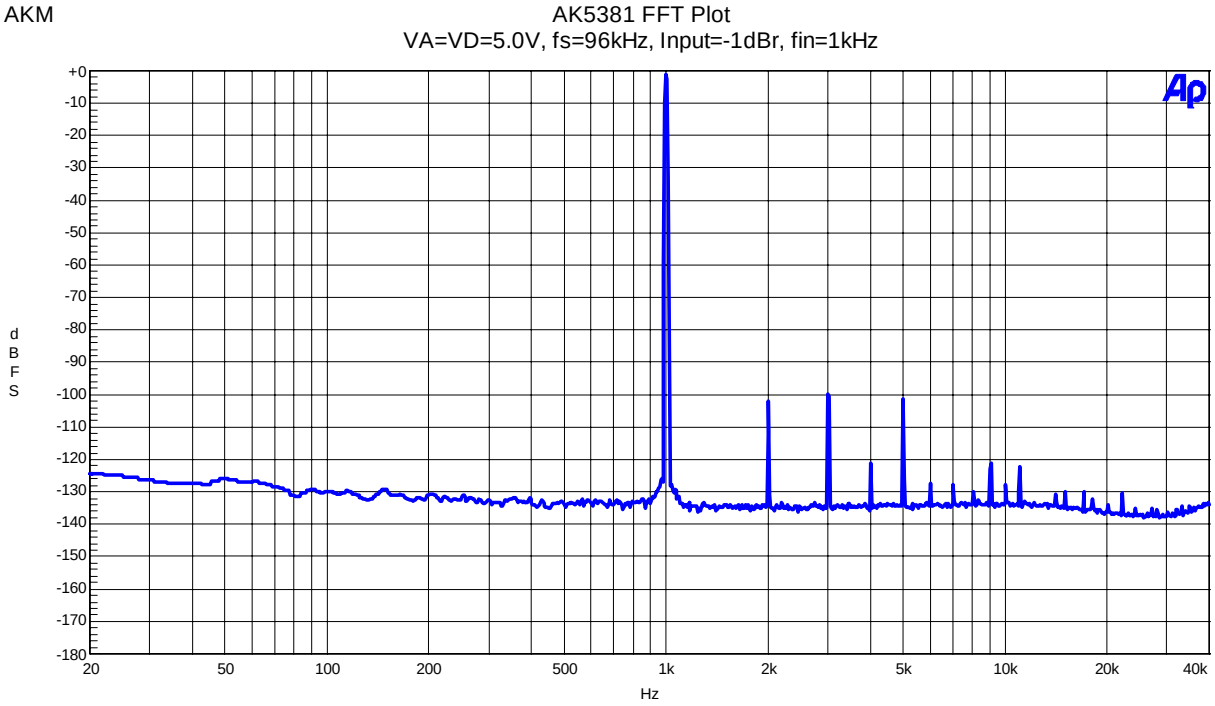


Figure 14. FFT Plot

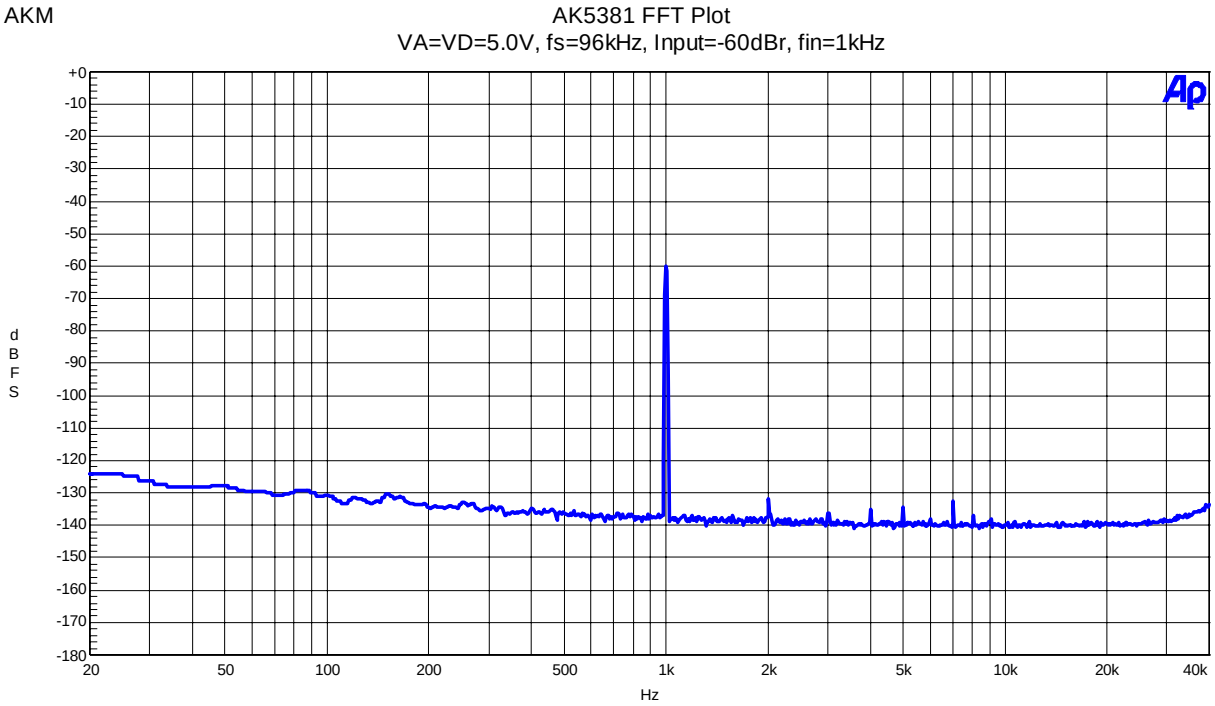


Figure 15. FFT Plot

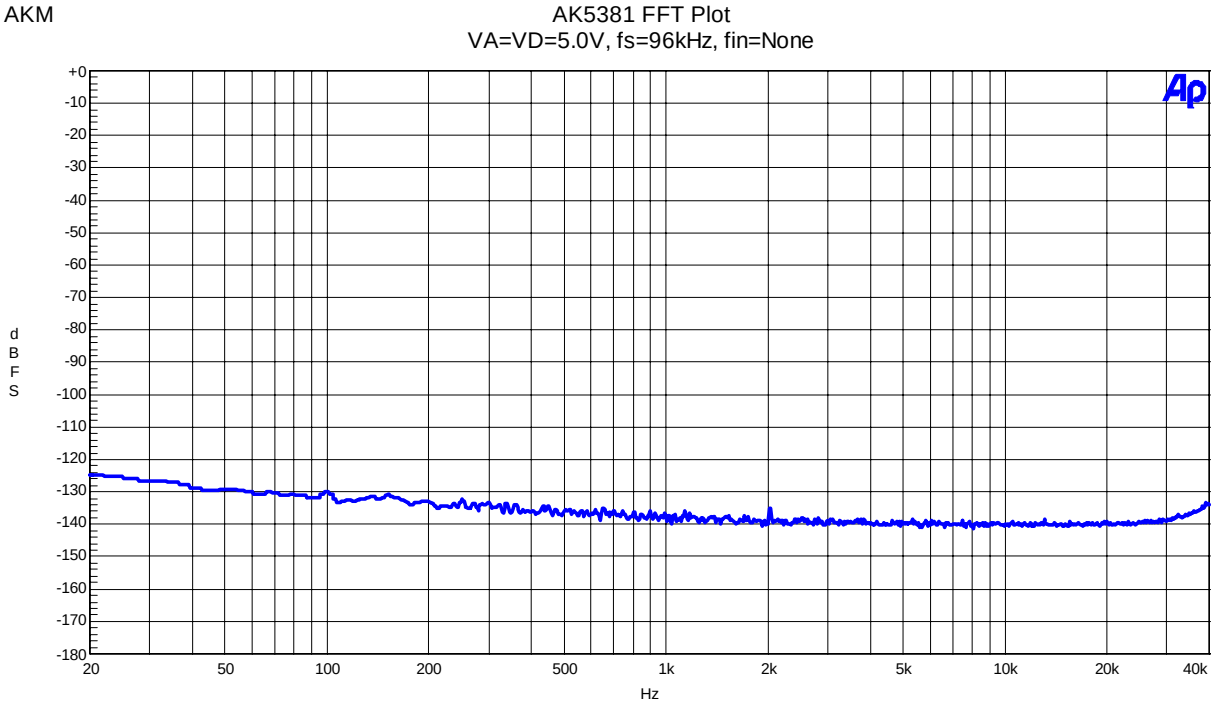


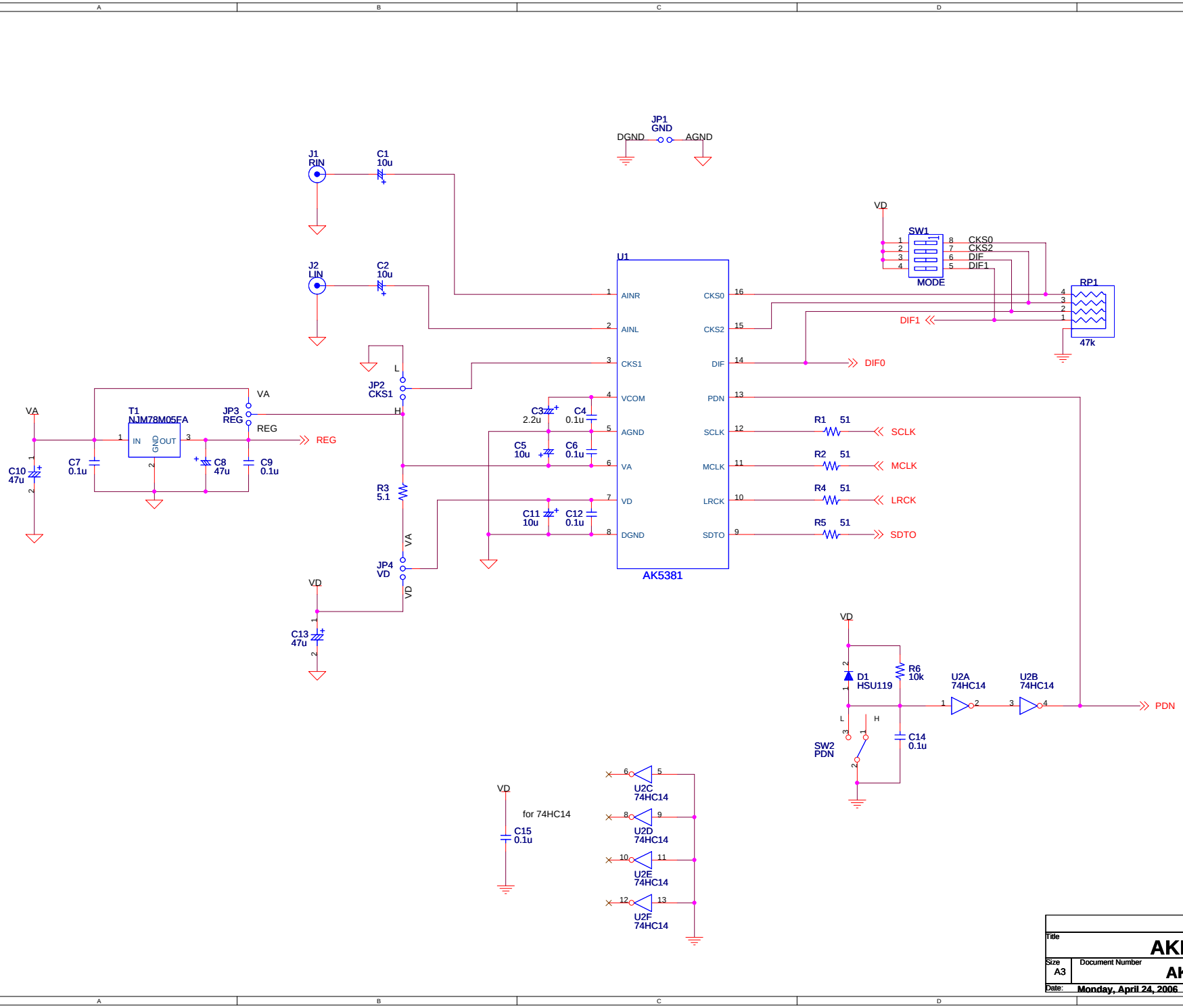
Figure 16. FFT Plot

Revision History

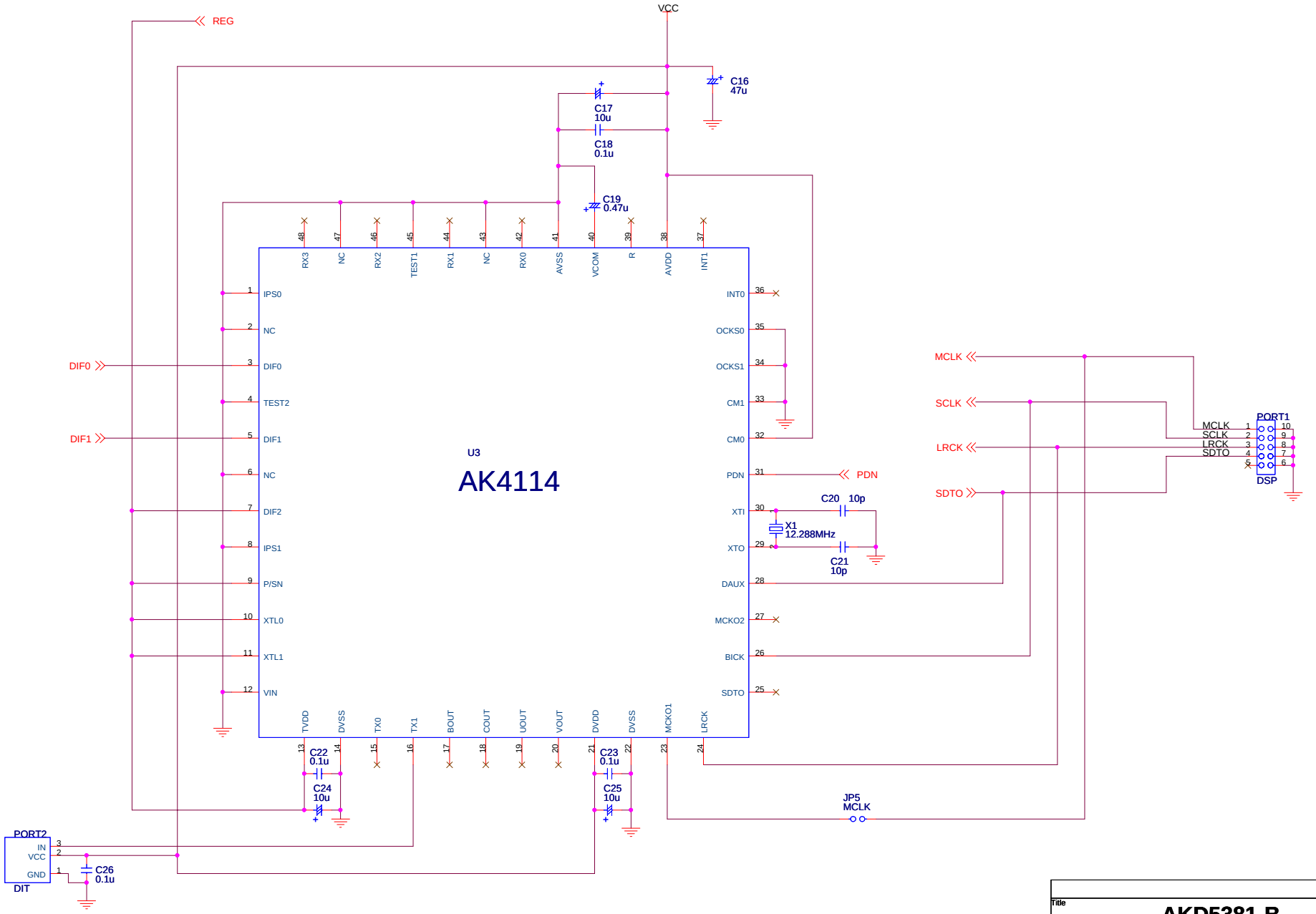
Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
04/05/14	KM074700		First Edition	
05/01/14	KM074701	0	Board Name Change	AKD5381 Rev.B→AKD5381-B Rev.0
			Circuit Change	The information on AK5357 was removed.
06/04/24	KM074702	1	Error Correction	Board Rev: 0→1

IMPORTANT NOTICE

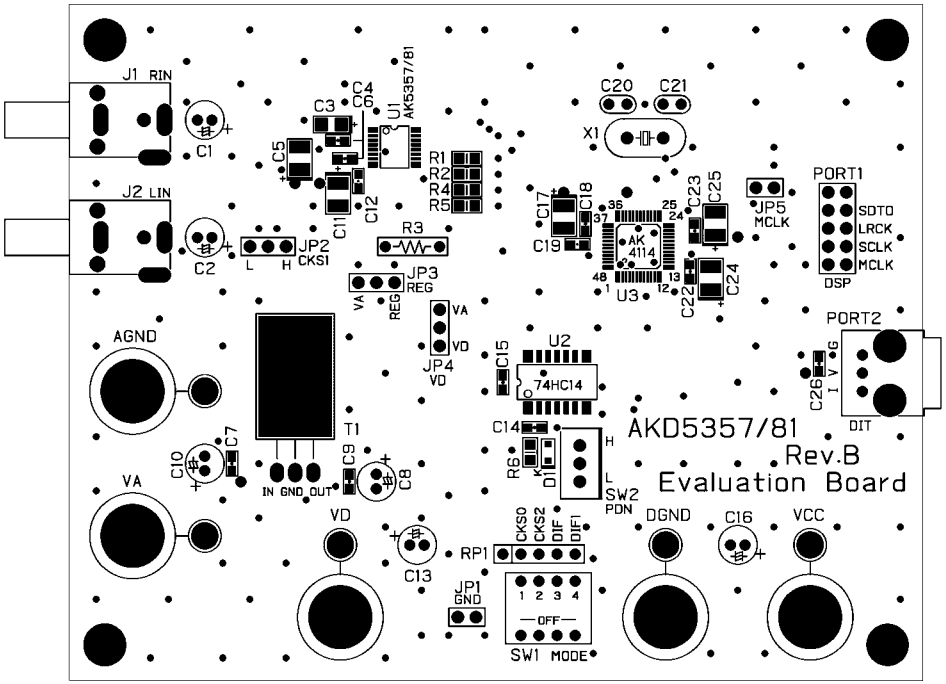
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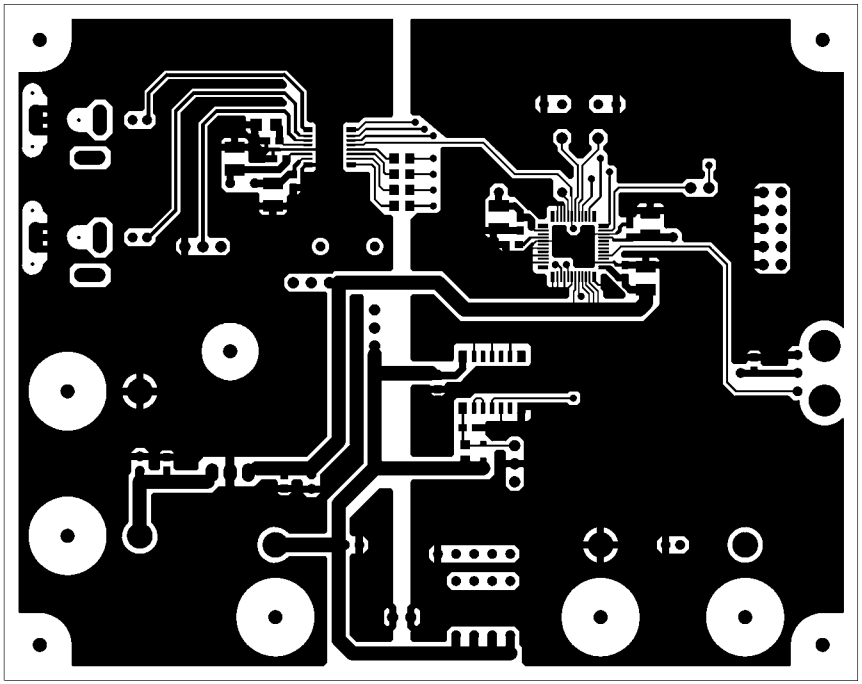
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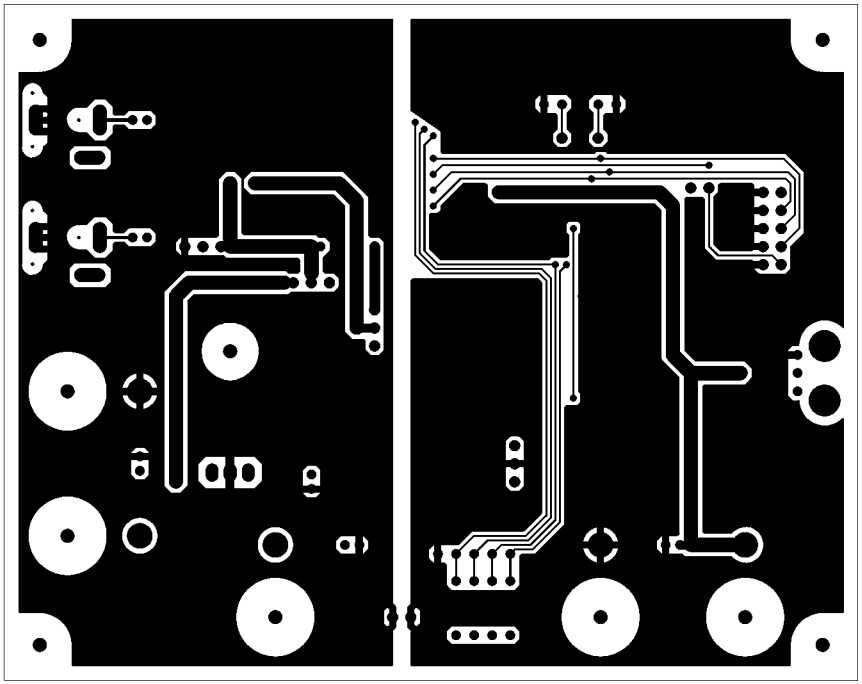
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AKD5357/81 Rev.B L1 SR SILK



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