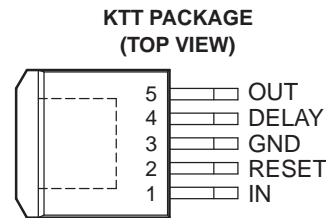


FEATURES

- Qualified for Automotive Applications
- Output Voltage 5 V \pm 2%
- Very Low Current Consumption
- Power-On and Undervoltage Reset
- Reset Low-Level Output Voltage < 1 V
- Very Low Dropout Voltage
- Short-Circuit Proof
- Reverse-Polarity Proof
- ESD Protection > 6 kV



DESCRIPTION/ORDERING INFORMATION

The TLE4275 is a monolithic integrated low-dropout voltage regulator offered in a 5-pin TO package. An input voltage up to 45 V is regulated to $V_{OUT} = 5$ V (typ). The device can drive loads up to 450 mA and is short-circuit proof. At overtemperature, the TLE4275 is turned off by the incorporated temperature protection. A reset signal is generated for an output voltage, $V_{OUT,rt}$, of 4.65 V (typ). The reset delay time can be programmed by the external delay capacitor.

The input capacitor, C_{IN} , compensates for line fluctuation. Using a resistor of approximately 1 Ω , in series with C_{IN} , dampens the oscillation of input inductivity and input capacitance. The output capacitor, C_{OUT} , stabilizes the regulation circuit. Stability is specified at $C_{OUT} \geq 22$ μ F and $ESR \leq 5$ Ω , within the operating temperature range.

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The device also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

ORDERING INFORMATION

T_J	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 150°C	TO-263 – KTT Reel of 500	TLE4275QKTTRQ1	TLE4275Q1

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

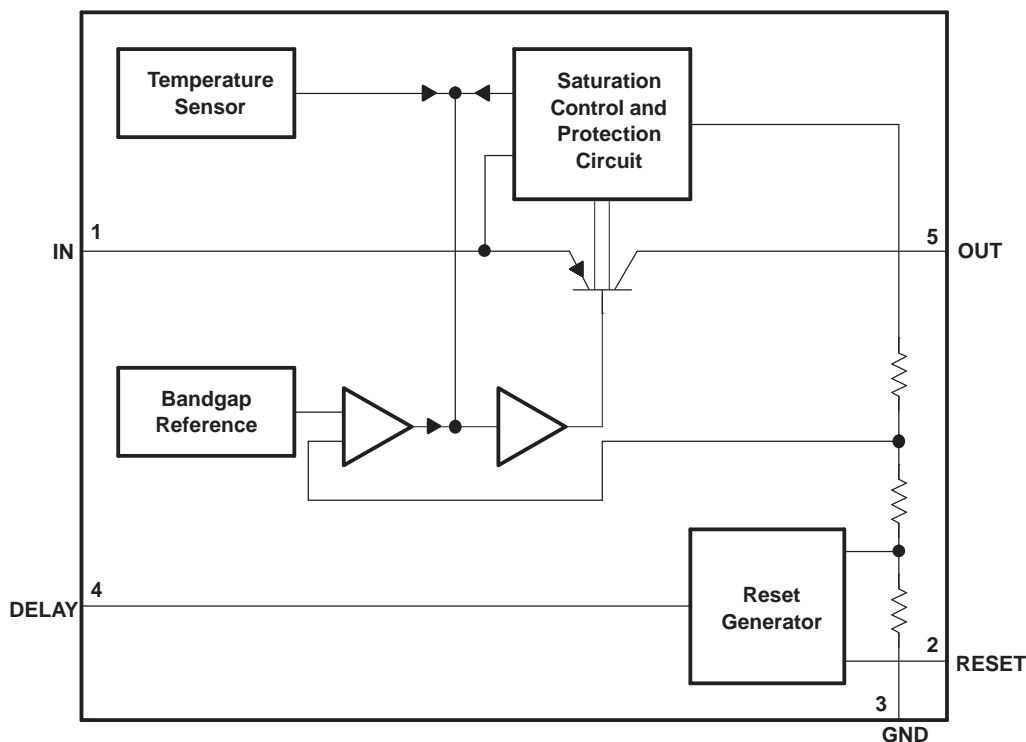
TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	IN	Input. Connect to ground as close to device as possible, through a ceramic capacitor.
2	RESET	Reset output. Open-collector output.
3	GND	Ground. Internally connected to heatsink.
4	DELAY	Reset delay. Connect to ground with a capacitor to set delay time.
5	OUT	Output. Connect to ground with ≥ 22 - μ F capacitor, $ESR < 5$ Ω at 10 kHz.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _I	Input voltage range ⁽²⁾	IN	-42	45	V
		DELAY	-0.3	7	
V _O	Output voltage range	OUT	-1	16	V
		RESET	-0.3	25	
I _I	Input current	DELAY		±2	mA
I _O	Output current	RESET		±5	mA
θ _{JA}	Package thermal impedance, junction to free air ⁽³⁾⁽⁴⁾			21.5	°C/W
T _J	Operating junction temperature range		-40	150	°C
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal.

(3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _I	Input voltage	5.5	42	V
T _J	Junction temperature	-40	150	°C

Electrical Characteristics

over recommended operating free-air temperature range, $V_I = 13.5\text{ V}$, $T_J = -40^\circ\text{C}$ to 150°C (unless otherwise noted) (see [Figure 1](#))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	$I_O = 5\text{ mA}$ to 400 mA , $V_I = 6\text{ V}$ to 28 V	4.9	5	5.1	V
		$I_O = 5\text{ mA}$ to 200 mA , $V_I = 6\text{ V}$ to 40 V	4.9	5	5.1	
I_O	Output current limit		450	700		mA
I_q	Current consumption $I_q = I_I - I_O$	$I_O = 1\text{ mA}$	$T_J = 25^\circ\text{C}$	150	200	μA
			$T_J \leq 85^\circ\text{C}$	150	220	
		$I_O = 250\text{ mA}$		5	10	mA
		$I_O = 400\text{ mA}$		12	22	
V_{do}	Dropout voltage ⁽¹⁾	$I_O = 300\text{ mA}$, $V_{do} = V_I - V_O$		250	500	mV
	Load regulation	$I_O = 5\text{ mA}$ to 400 mA		15	30	mV
	Line regulation	$\Delta V_I = 8\text{ V}$ to 32 V , $I_O = 5\text{ mA}$	-15	5	15	mV
PSSR	Power-supply ripple rejection	$f_r = 100\text{ Hz}$, $V_r = 0.5\text{ V}_{pp}$		60		dB
$\frac{\Delta V_O}{\Delta T}$	Temperature output-voltage drift			0.5		mV/K
$V_{O,rt}$	RESET switching threshold		4.5	4.65	4.8	V
V_{ROL}	RESET output low voltage	$R_{ext} \geq 5\text{ k}\Omega$, $V_O > 1\text{ V}$		0.2	0.4	V
I_{ROH}	RESET output leakage current	$V_{ROH} = 5\text{ V}$		0	10	μA
$I_{D,c}$	RESET charging current	$V_D = 1\text{ V}$	3	5.5	9	μA
V_{DU}	RESET upper timing threshold		1.5	1.8	2.2	V
V_{DRL}	RESET lower timing threshold		0.2	0.4	0.7	V

(1) Measured when the output voltage V_O has dropped 100 mV from the nominal value obtained at $V_I = 13.5\text{ V}$

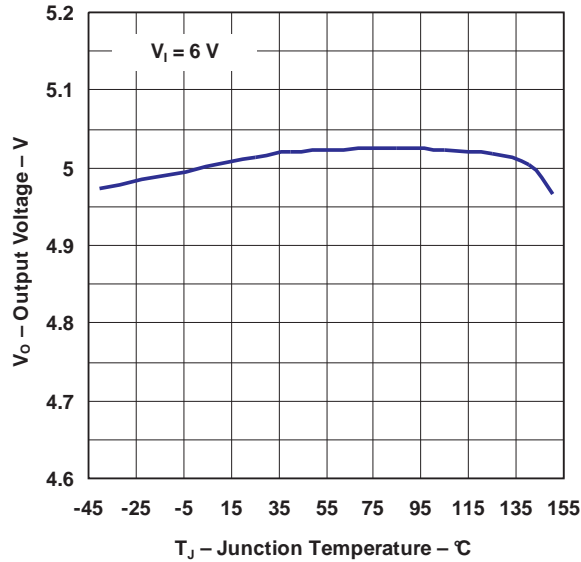
Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

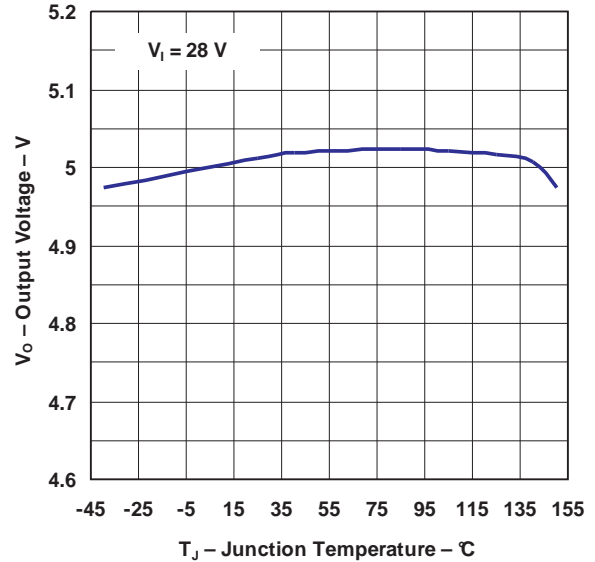
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rd}	RESET delay time	$C_D = 47\text{ nF}$	10	16	22	ms
t_{rr}	RESET reaction time	$C_D = 47\text{ nF}$		0.5	2	μs

TYPICAL CHARACTERISTICS

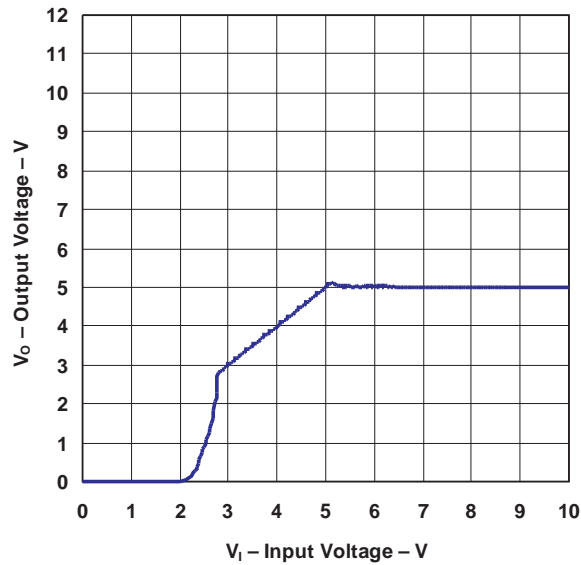
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE



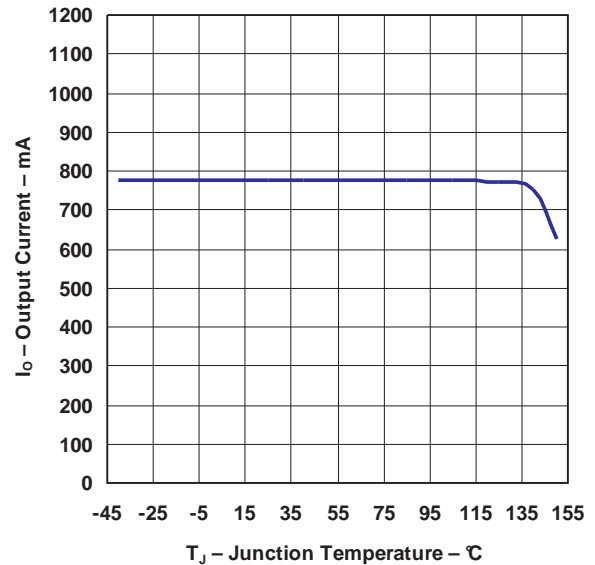
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE



OUTPUT VOLTAGE
VS
INPUT VOLTAGE

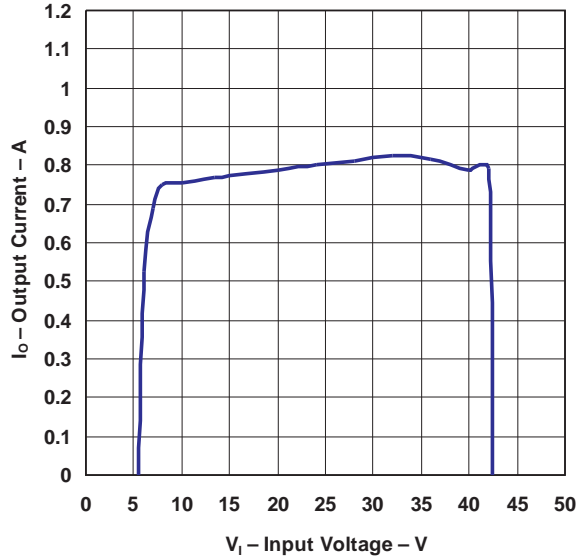


OUTPUT CURRENT
VS
JUNCTION TEMPERATURE

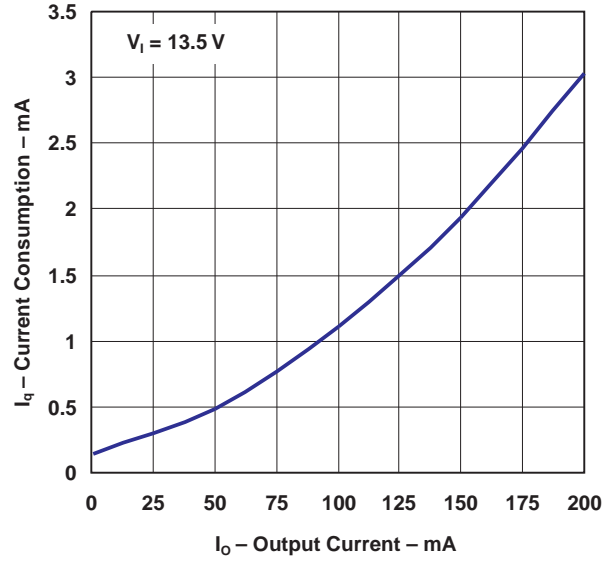


TYPICAL CHARACTERISTICS (continued)

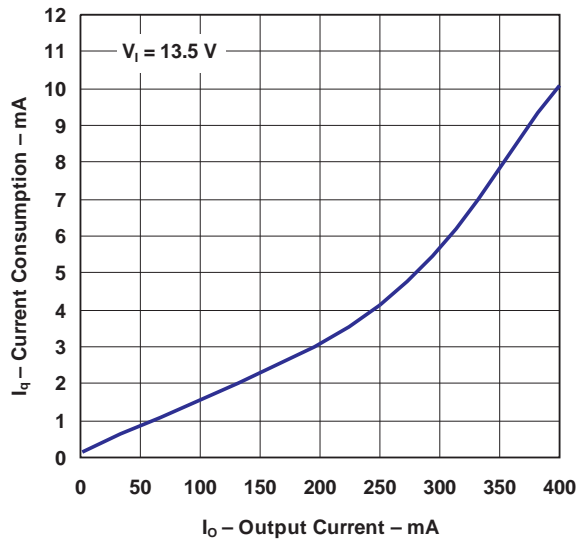
OUTPUT CURRENT
VS
INPUT VOLTAGE



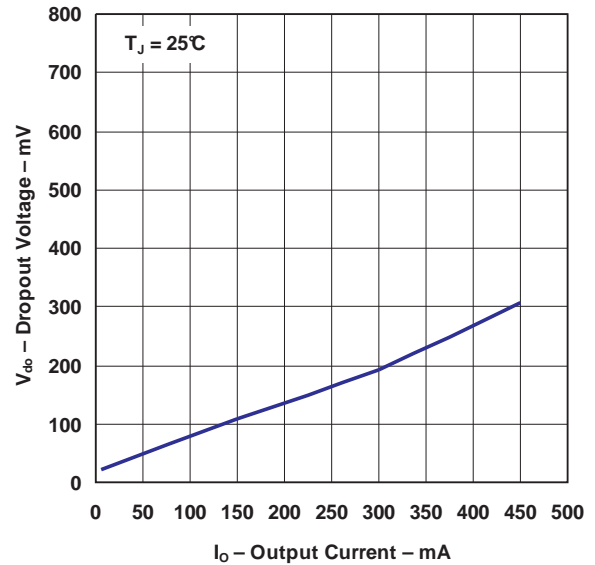
CURRENT CONSUMPTION
VS
OUTPUT CURRENT



CURRENT CONSUMPTION
VS
OUTPUT CURRENT

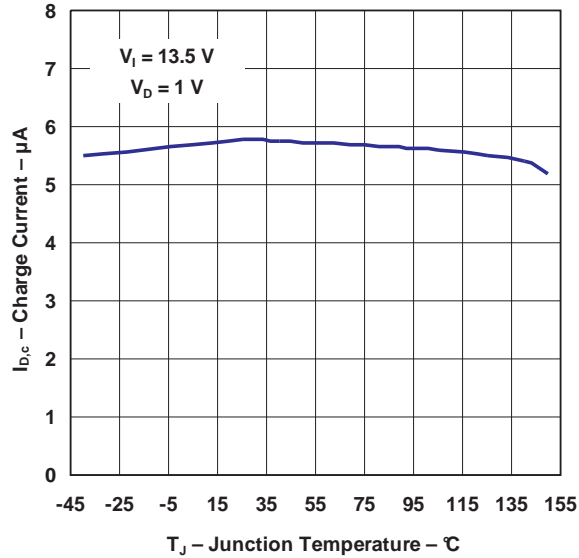


DROPOUT VOLTAGE
VS
OUTPUT CURRENT

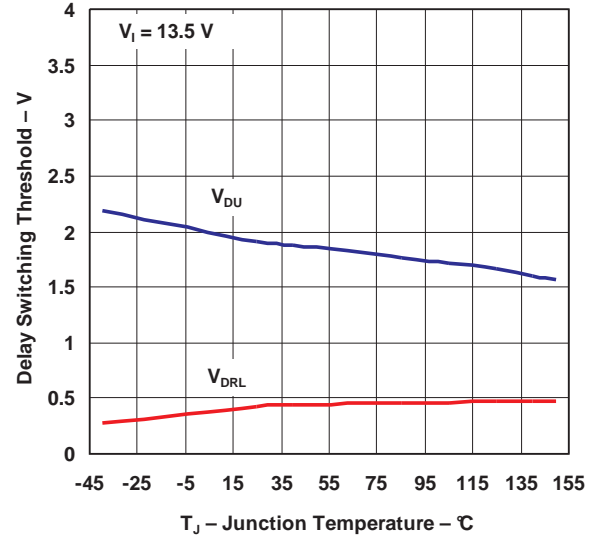


TYPICAL CHARACTERISTICS (continued)

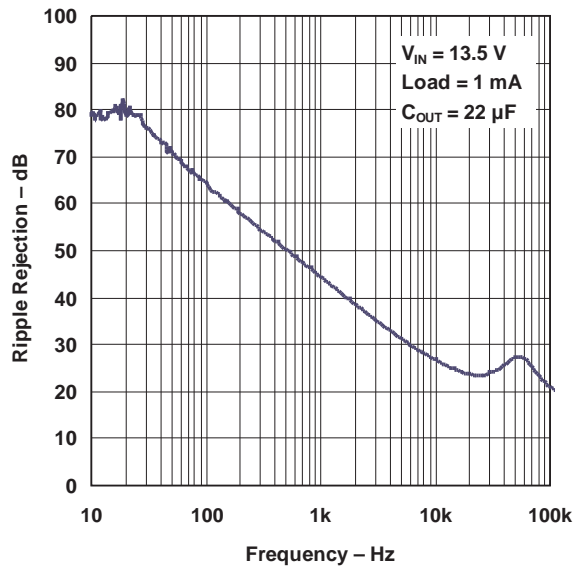
CHARGE CURRENT
VS
JUNCTION TEMPERATURE



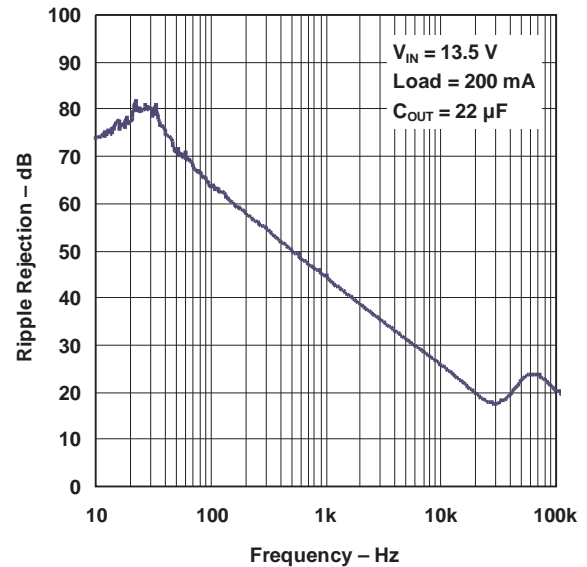
DELAY SWITCHING THRESHOLD
VS
JUNCTION TEMPERATURE



POWER-SUPPLY RIPPLE REJECTION
VS
FREQUENCY

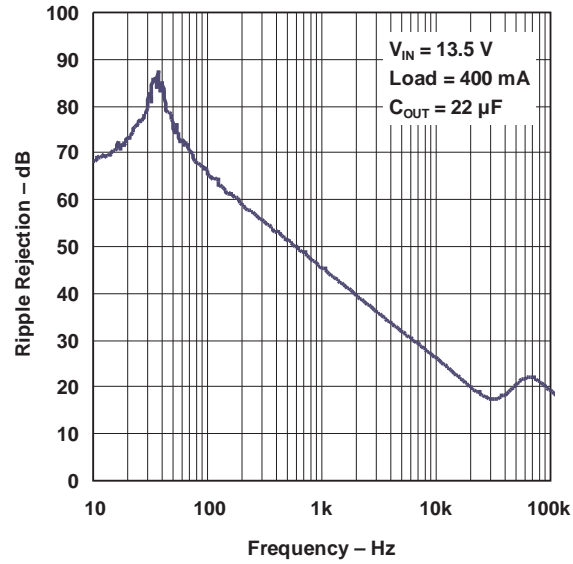


POWER-SUPPLY RIPPLE REJECTION
VS
FREQUENCY



TYPICAL CHARACTERISTICS (continued)

POWER-SUPPLY RIPPLE REJECTION
VS
FREQUENCY



PARAMETER MEASUREMENT INFORMATION

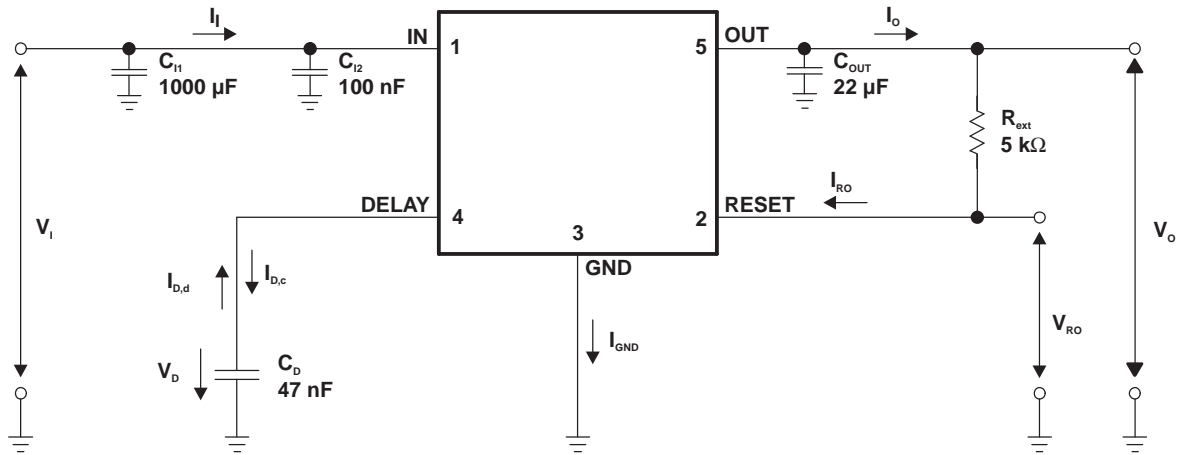


Figure 1. Test Circuit

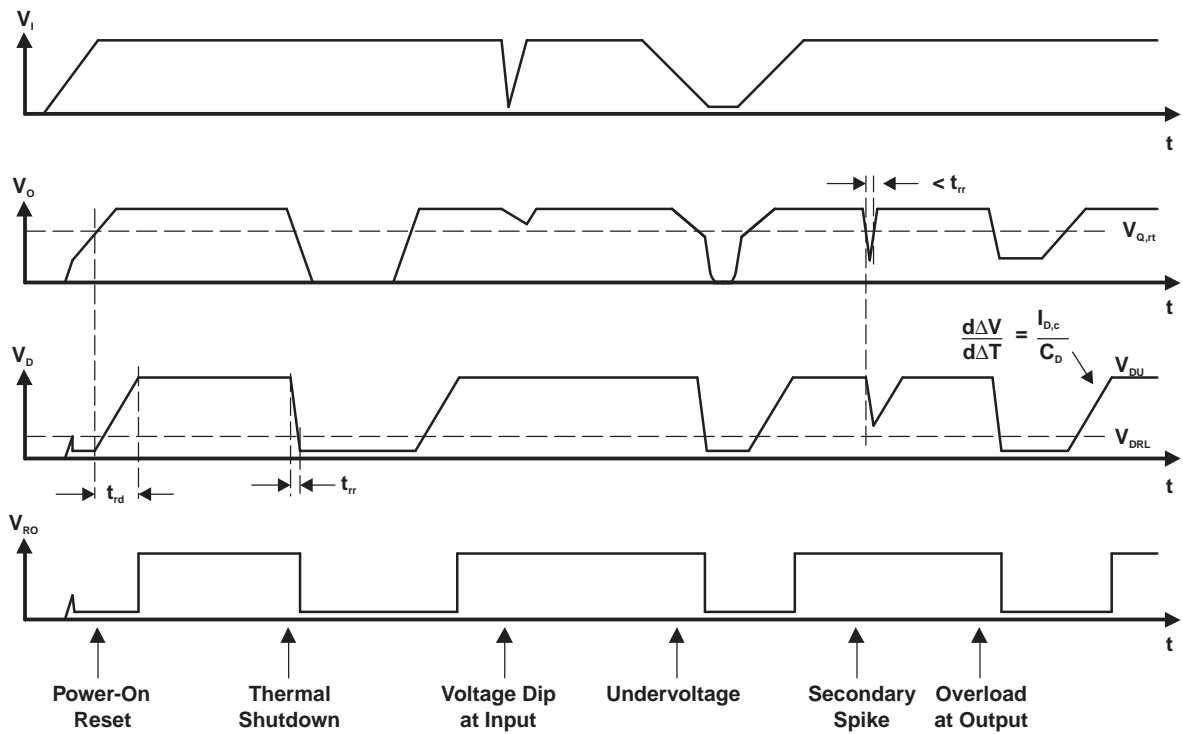


Figure 2. Reset Timing

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLE4275QKTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-1 WEEK

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

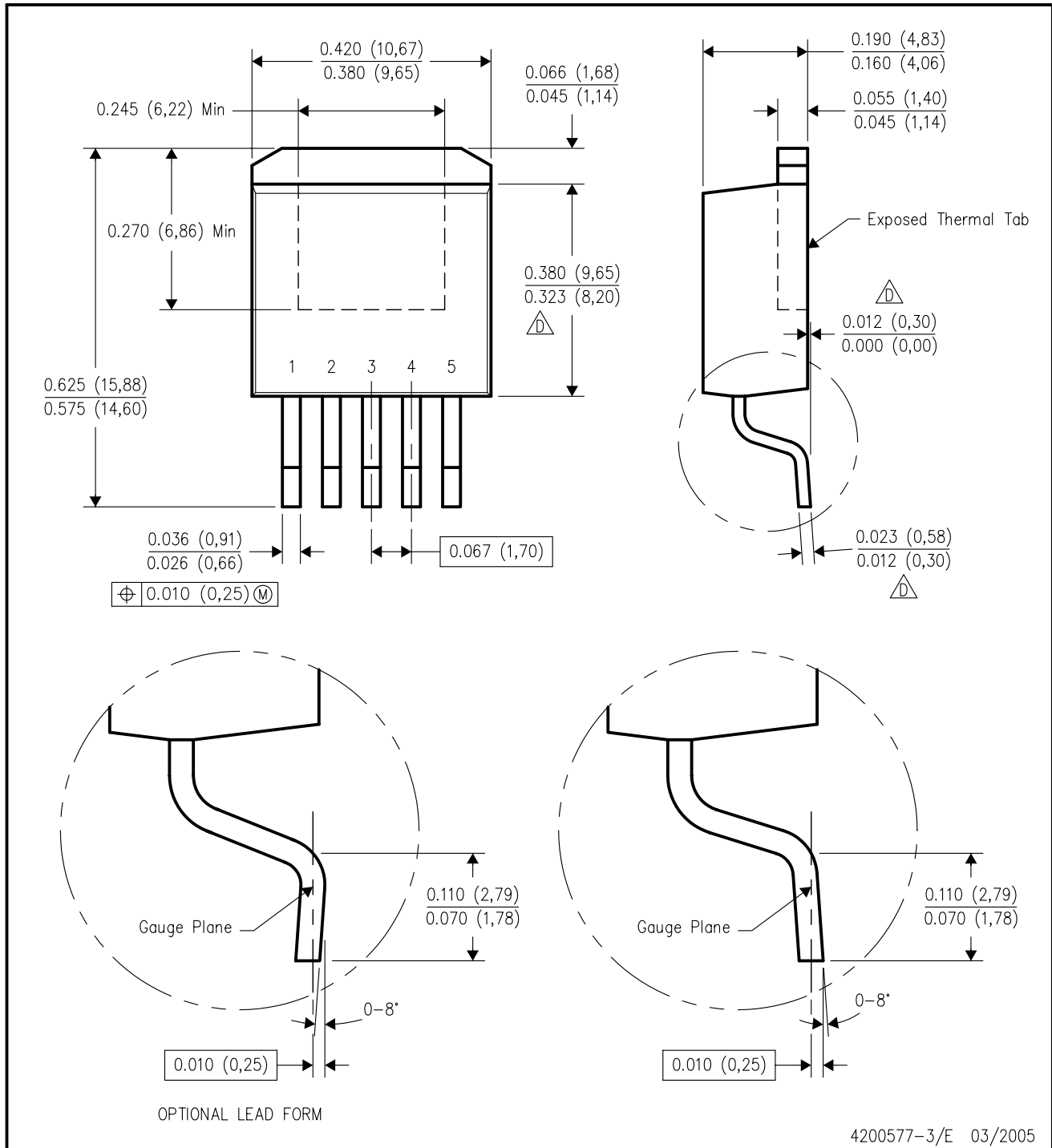
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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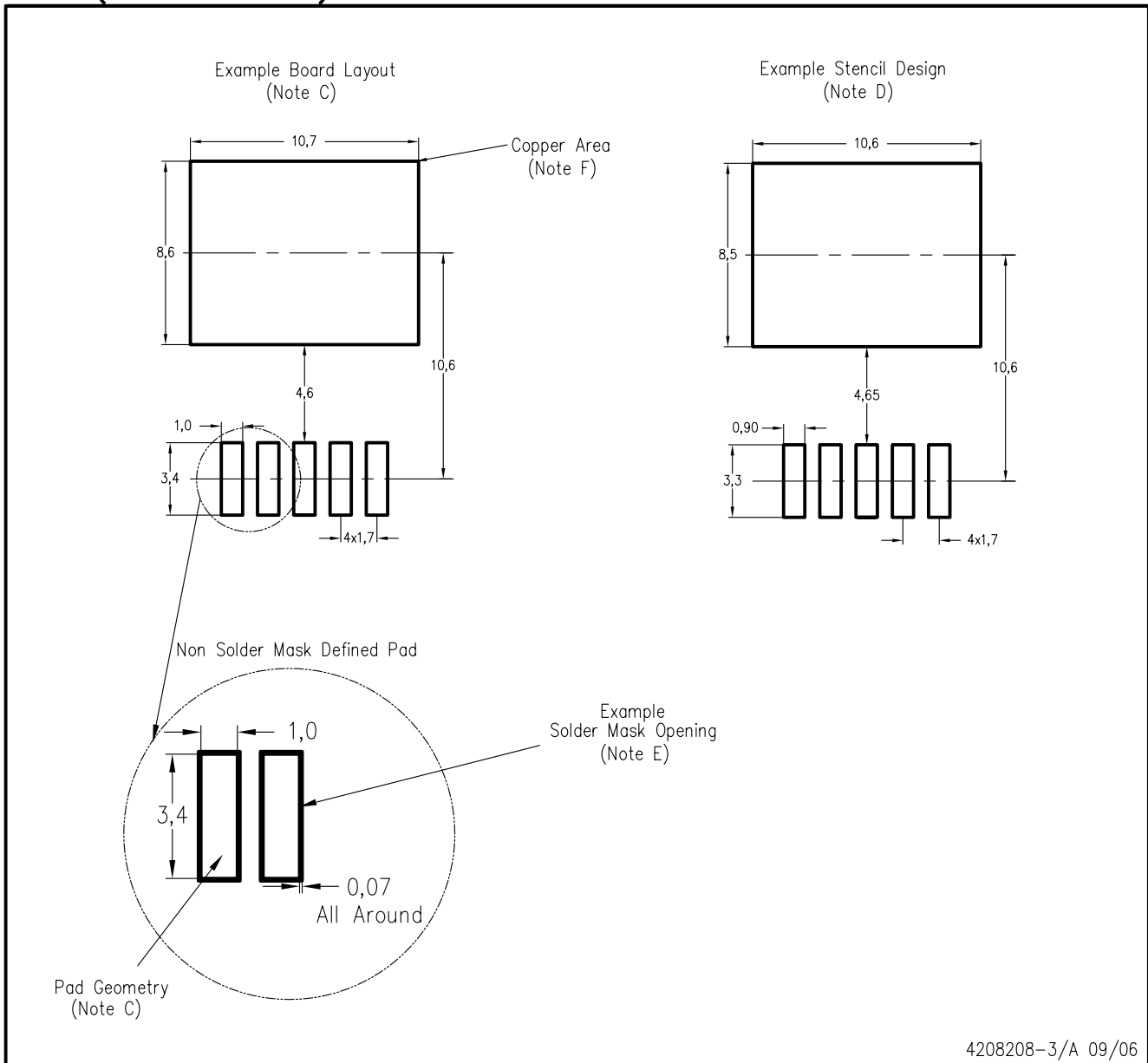
KTT (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- ⊕ Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R-PSFM-G5)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-SM-782 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
 - F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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