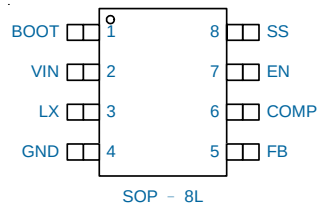
2A, 18V, High-Efficiency Synchronous-Rectified Buck Converter

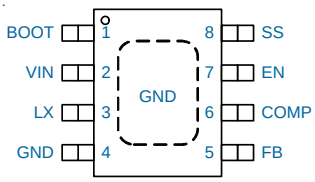
General Description

The uP1723 is a high-efficiency synchronous-rectified buck converter with internal power switch. With internal low $R_{DS(ON)}$ switches, the high-efficiency buck converter is capable of delivering 2A output current over a wide input voltage range from 4.5V to 18V. The output voltage is adjustable from 0.8V to 15V by a voltage divider. Other features for the buck converter include adjust soft-start, chip enable, over-voltage, under-voltage, over-temperature and over-current protections. It is available in a space saving SOP-8L, PSOP-8L, PMSOP-8L and PMSOP-10L packages.

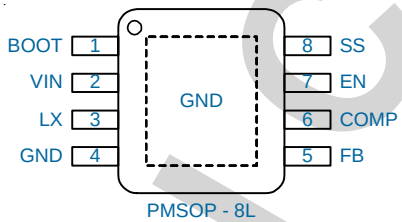
Pin Configuration



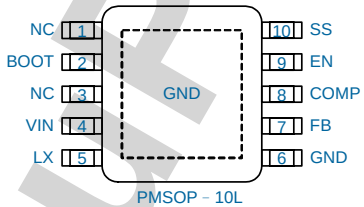
SOP – 8L



PSOP – 8L



PMSOP - 8L



PMSOP – 10L

Features

- 4.5V to 18V Input Voltage Range
- 2A Output Current
- Accurate Reference: 0.925V (+/- 1.5%)
- Up to 93% Conversion Efficiency
- Integrated Low $R_{DS(ON)}$ Upper and Lower MOSFET Switches: 130mΩ
- Current Mode PWM Operation
- 340kHz Fixed-Frequency Operation
- Programmable Soft-Start
- Integrated Boot Diode
- Over Voltage and Under Voltage Protection
- Over Current and Over Temperature Protection
- Frequency Decay Mode During UVP
- SOP-8L, PSOP-8L, PMSOP-8L and PMSOP-10L Package
- RoHS Compliant and Halogen Free

Applications

- Battery-Powered Portable Devices
  - MP3 Players
  - Digital Still Cameras
  - Wireless and DSL Modems
  - Personal Information Appliances
- 802.11 WLAN Power Supplies
- FPGA/ASIC Power Supplies
- Laptop, Palmtops, Notebook Computers
- Portable Information Appliances

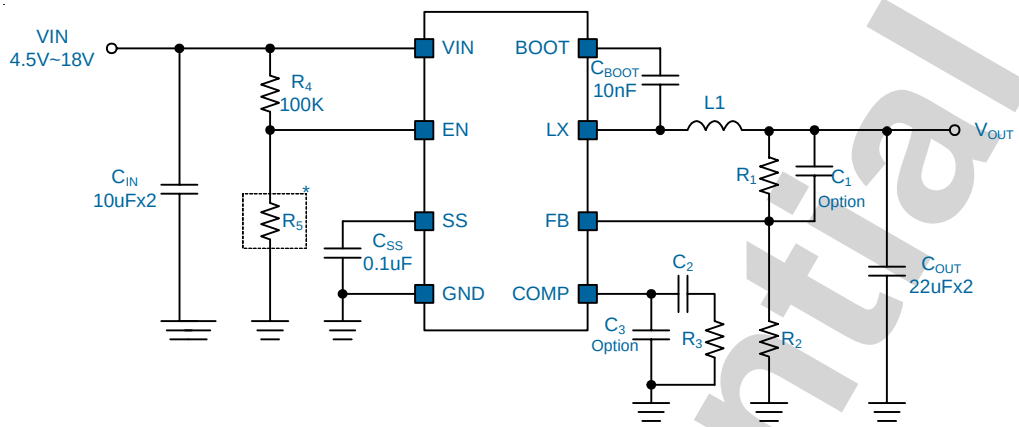
Ordering Information

Order Number	Package Type	Top Marking
uP1723PSA8	SOP-8L	uP1723P
uP1723PSU8	PSOP-8L	uP1723P
uP1723PRU8	PMSOP-8L	uP1723P
uP1723PRUA	PMSOP-10L	uP1723P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

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Typical Application Circuit



Note: * check BOM List for EN Pin Application table below.

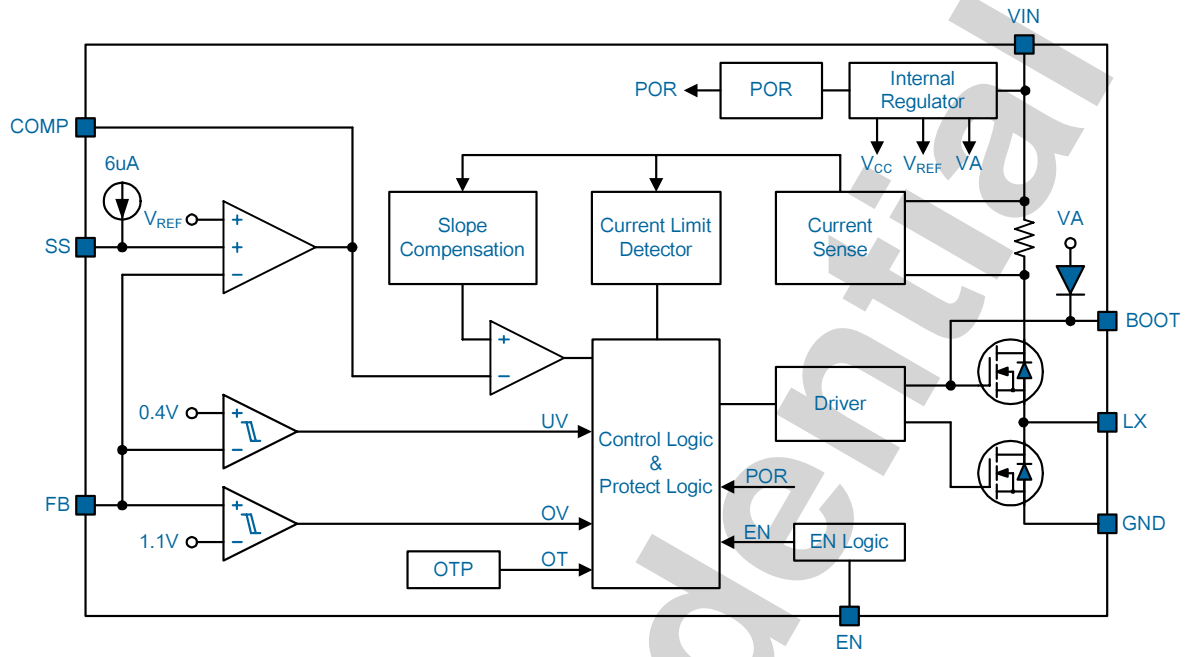
V_{IN}	V_{OUT}	C_{IN}	L1	C_{OUT}	C_1	C_2	R_1	R_2	R_3
12V	1.2V	10uFx2	2.2uH	22uFx2	22pF	1.5nF	3K	10K	4.7K
12V	1.8V	10uFx2	2.2uH	22uFx2	22pF	1.5nF	9.53K	10K	6.2K
12V	2.5V	10uFx2	6.8uH	22uFx2	22pF	1.5nF	16.9K	10K	8.2K
12V	3.3V	10uFx2	10uH	22uFx2	22pF	1.5nF	26.1K	10K	10K
12V	5V	10uFx2	15uH	22uFx2	22pF	1.5nF	44.2K	10K	13K

BOM List for EN Pin Application:

	Power Saving Mode			Full Power Mode		
V_{IN}	R4	R5	VEN	R4	R5	VEN
4.5V	100k	NC	4.40V	100k	180k	2.89V
5.0V	100k	NC	4.80V	100k	130k	2.82V
9.0V	100k	110k	4.71V	100k	47k	2.87V
12V	100k	62k	4.59V	100k	30k	2.76V
15V	100k	43k	4.51V	100k	22k	2.70V

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Functional Block Diagram



Functional Pin Description

Pin No.		Pin Name	Pin Function
PSA8/ PSU8/ PRU8	PRUA		
--	1,3	NC	**Not Internal Connected.**
1	2	BOOT	**Bootstrap Supply for the Floating Upper Gate Driver.** Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the LX pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical value for C_{BOOT} is 10nF or greater. Ensure that C_{BOOT} is placed near the IC.
2	4	VIN	**Power Supply Input**. Input voltage that supplies current to the output voltage and powers the internal control circuit. Bypass the input voltage with a minimum 10uFx2 X5R or X7R ceramic capacitor.
3	5	LX	**Internal Switches Output.** Connect this pin to the output inductor.
4	6	GND	**Ground.** Ground of the buck converter.
5	7	FB	**Switcher Feedback Voltage.** This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network.
6	8	COMP	**Compensation.** This pin is output of the error amplifier. The current comparator threshold increases with this control voltage. Connect an RC network to ground for control loop compensation.
7	9	EN	**Buck Converter Enable (Active High).** Logic low shuts down the converter.
8	10	SS	**Soft-Start Control Pin.** Connect a softstart capacitor C_{SS} to this pin. Leave open for no soft-start application. The softstart capacitor is discharged to ground when EN pin is low.
Exposed Pad			**Ground.** Ground of the buck converter.

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Functional Description

The uP1723 is a high efficiency synchronous-rectified buck converter with internal power switches. With internal low $R_{DS(ON)}$ switches, it is capable of delivering 2A output current over a wide input voltage range from 4.5V to 18V. The output voltage is adjustable from 0.925V to 15V by a voltage divider. Other features include Programmable soft-start, chip enable, overvoltage, under-voltage, over-temperature and over-current protections.

Input Supply Voltage

VIN supplies current to internal control circuits and output voltages. The supply voltage range is from 4.5V to 18V. A power on reset (POR) continuously monitors the input supply voltage. The POR level is typically 4.0V at VIN rising. The buck converter draws pulsed current with sharp edges each time the upper switch turns on, resulting in voltage ripples and spikes at supply input. A minimum 10uFx2 ceramic capacitor with shortest PCB trace is highly recommended for bypassing the supply input.

Enable Control with Operation Mode Setting

Pulling EN pin lower than 1.2V shuts down the buck converter and reduces its quiescent current lower than 1uA. In the shutdown mode, both upper and lower switches are turned off.

As shown in Table 1, to set the buck converter in the full power mode by pulling EN pin between 2.4V and 3V.

Pulling EN pin higher than 3.8V to set the buck converter in the power saving mode.

Table 1. Mode Table Selection

EN Rising	Mode
2.4V < EN < 3V	Full Power Mode
3.8V < EN < 5.5V	Power Saving Mode

Soft Start

The uP1723 features programmable soft start function to limit the inrush current from supply input by a soft start

capacitor C_{SS} connected to SS pin as shown in Figure 1.The C_{SS} is charged to VIN by a 6uA current source when EN pin is taken high.

The error amplifier is a tri-input device. V_{SS} or V_{REF} whichever is smaller dominates the non-inverting inputs of the error amplifier. The V_{FB} voltage will follow the V_{SS} and ramp up linearly. When V_{SS} is higher than V_{REF}, the uP1723 asserts soft start end and the V_{FB} voltage is regulated to V_{REF}. Soft start end also initiates the output under voltage protection.

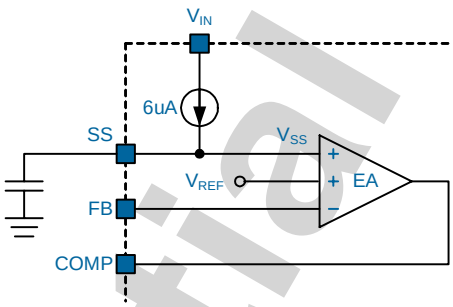


Figure 1. uP1723 Soft Start

Main Control Loop

The uP1723 adopts slope-compensated, current mode PWM control. During normal operation, the uP1723 operates at PWM mode to regulate output voltage by transferring the power to the output voltage cycle by cycle at a constant frequency. The uP1723 turns on the upper switch at each rising edge of the internal oscillator allowing the inductor current to ramp up linearly. The switch remains on until either the current limit is tripped or the PWM comparator turns off the switch for regulating output voltage.

The lower switch turns on with optimal dead time and picks up the inductor current after the upper switch turns off allowing the inductor current to ramp down linearly. The switch remains on until the next rising edge of oscillator turns on the upper switch. The uP1723 regulates the output voltage by controlling the ramp up/down duty cycle of inductor current. The high frequency switching ripple is easily smoothed by the output filter.

The upper switch current is sensed, slope compensated and compared with the error amplifier output COMP to determine the adequate duty cycle. The feedback voltage VFB is sensed through a resistive voltage divider and regulated to internal 0.925V reference voltage. The error amplifier amplifies and compensates voltage variation to get appropriate COMP pin voltage.

When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.925V reference, which in turn, causes the error amplifier output voltage to increase until the average inductor current matches the new load current.

The uP1723 also adopts power saving technology for improving efficiency at light load. When output load is lower than an internal power saving threshold, the uP1723 automatically enters power saving mode which adaptively controls the switching behavior to reduce switching loss, therefore enhances total efficiency of the buck converter.

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Functional Description

Output Voltage Setting and Feedback Network

For the adjustable output version, the output voltage can be set from VREF to VIN by a voltage divider as:

$$V_{OUT} = \frac{0.925 \times (R1 + R2)}{R2}$$

The internal VREF is 0.925V with 1.5% accuracy. In real applications, a 22pF feed-forward ceramic capacitor is recommended in parallel with R1 for better transient response.

Over Temperature Protection

The OTP is triggered and shuts down the uP1723 if the junction temperature is higher than 150°C. The OTP is a non-latch type protection. The uP1723 automatically initiates another soft start cycle if the junction temperature drops below 120°C.

Current Limit Function

The uP1723 continuously monitors the inductor current for current limit by sensing the voltage drop across the upper switch when it turns on. When the inductor current is higher than current limit threshold (4A typical), the current limit function activates and forces the upper switch turning off to limit inductor current cycle by cycle. If the load continuously demands more current than what uP1723 could provide, uP1723 will not be able to regulate the output voltage, and the output voltage will drop accordingly. Eventually, under voltage protection will be triggered if V_{FB} is lower than UVP threshold.

When the output is shorted to ground, the current limit function activates immediately, and VOUT will be pulled down very fast. Eventually the under voltage protection will be triggered, and the IC will shut down to protect external components. The IC will restart after the UVP retry delay, and the above behavior may repeat if the output short condition is not released. This is the so-called Short Circuit Protection (SCP).

Under Voltage Protection

The uP1723 continuously monitors FB voltage for under voltage protection. When V_{FB} < 0.4V (typical), the uP1723 triggers under voltage protection and enters frequency decay mode which the switching frequency of the uP1723 will decrease linearly according to the FB voltage drop. Eventually when V_{FB} = 0V, the switching frequency of the uP1723 will be clamped at 100kHz. After triggering UVP, the SS voltage is also discharged to 0V. After V_{SS} = 0V, the uP1723 will try to re-soft-start to establish the output voltage once again. In the end of re-soft-start (V_{SS} = 1.2V), if the UVP condition is still not relieved, the uP1723 will turn-off all high-side and low-side MOSFETs and re-try to soft start every 8ms.

Over Voltage Protection

The uP1723 continuously monitors FB voltage for over voltage protection. When V_{FB} > 1.1V (typical), the uP1723 triggers over voltage protection and the low-side MOSFET is turned on while high-side MOSFET is turned off to discharge the output voltage. At any time if the OVP condition is relieved, the uP1723 will restart the soft start sequence.

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Absolute Maximum Rating

(Note 1)

Supply Input Voltage, V_{IN} ---------- -0.3V to +20V

LX Pin Voltage

DC ---------- -0.3V to +(V_{IN} +0.3V)

<50ns ---------- -3.5V to +25V

BOOT Pin Voltage ---------- -0.3V to (V_{IN} +6.0V)

Other Pins ---------- -0.3V to +6.0V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3/4)

SOP - 8L θ_{JA} ---------- 160°C/W

SOP - 8L θ_{JC} ---------- 39°C/W

PSOP - 8L θ_{JA} ---------- 47°C/W

PSOP - 8L θ_{JC} ---------- 17.9°C/W

PMSOP - 8L θ_{JA} ---------- 86°C/W

PMSOP - 8L θ_{JC} ---------- 30°C/W

PMSOP - 10L θ_{JA} ---------- 160°C/W

PMPSOP - 10L θ_{JC} ---------- 40°C/W

Power Dissipation, P_D @ T_A = 25°C

SOP - 8L ---------- 0.63W

PSOP - 8L ---------- 2.13W

PMSOP - 8L ---------- 1.16W

PMSOP - 10L ---------- 0.63W

Recommended Operation Conditions

(Note 5)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
VIN POR Threshold	V_{INRTH}		3.8	4.2	4.5	V
VIN POR Hysteresis	V_{INHYS}		--	0.32	--	V
Quiescent Current		V_{EN} = 5V, V_{FB} = 1V, no switching	--	0.8	1.2	mA
Shutdown Current	I_{SD}	V_{EN} = 0	--	0.5	3	uA

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Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Feedback Voltage						
Feedback Voltage	V_{FB}	4.5V < V_{IN} < 18V	0.911	0.925	0.939	V
Error Amplifier Transconductance	GEA	ΔIC = +/- 10uA	--	940	--	uA/V
COMP to Current Sense Transconductance	GCS		--	4	--	A/V
Power Switches						
Hide-Side Switch On Resistance	$R_{DS(ON)}$		--	130	--	mΩ
Low-Side Switch On Resistance	$R_{DS(ON)}$		--	130	--	mΩ
High Side Switch Leakage Current	I_{EN}	V_{EN} = 0, V_{SW} = 0	--	0	10	uA
Upper Side Switch Current Limit			--	4	--	A
Oscillator						
Oscillation Frequency	f_{OSC1}		300	340	380	kHz
Short Circuit Oscillation Frequency	f_{OSC2}		--	100	--	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	--	93	--	%
Minimum On Time	T_{ON}		--	130	--	ns
Enable						
EN Logic High		V_{EN} rising	2.4	--	5.5	V
EN Logic Low		V_{EN} falling	--	--	1.2	V
Full Power Entry Threshold		V_{EN} rising	2.4	--	3	V
Power Saving Entry Threshold		V_{EN} rising	3.8	--	5.5	V
Soft Start						
Soft Start Current	I_{SS}	V_{SS} = 0V	5.5	6	6.5	uA
Protect						
Under Voltage Protect		FB falling	--	0.4	--	V
Over Voltage Protect		FB rising	--	1.1	--	V
Thermal Shutdown Temperature	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		--	30	--	°C

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. q_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

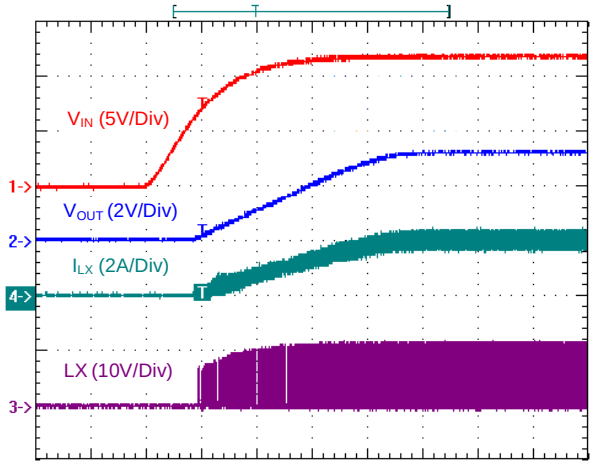
Note 4. The "case temperature" location for measuring θ_{JC} is on the top of the package.

Note 5. The device is not guaranteed to function outside its operating conditions.

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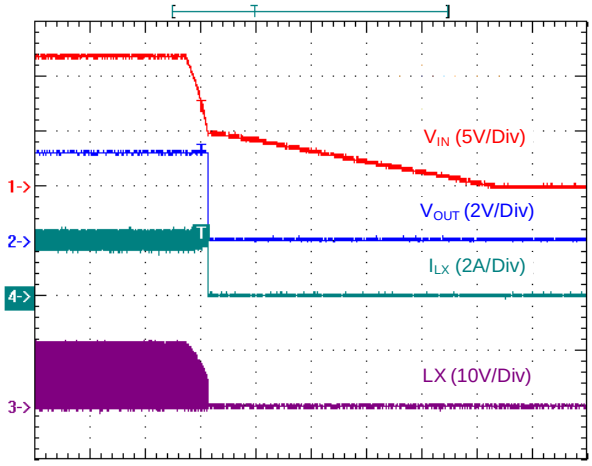
Typical Operation Characteristics

Power On Waveforms



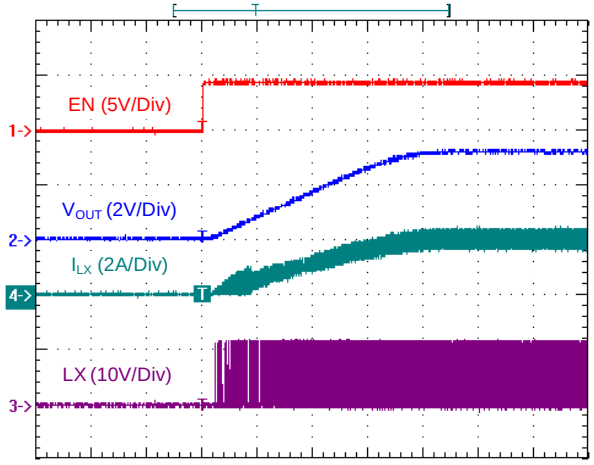
4ms/Div
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A

Power Off Waveforms



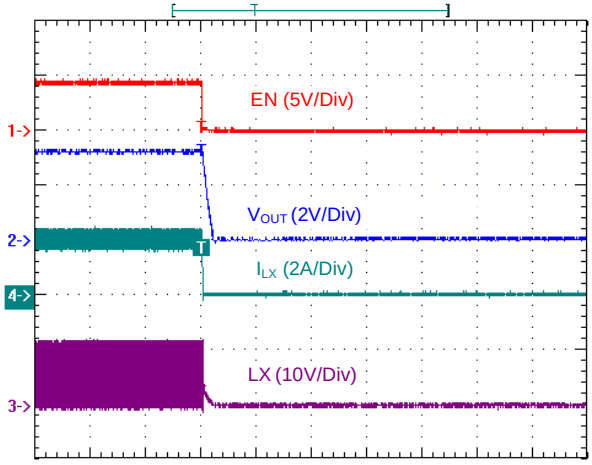
20ms/Div
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A

Turn On Waveforms



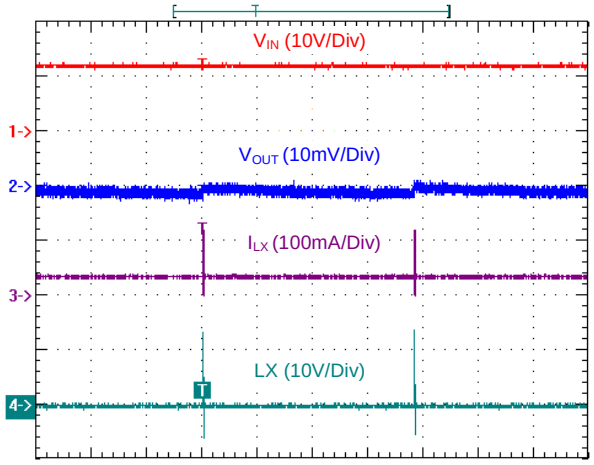
4ms/Div
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A

Turn Off Waveforms



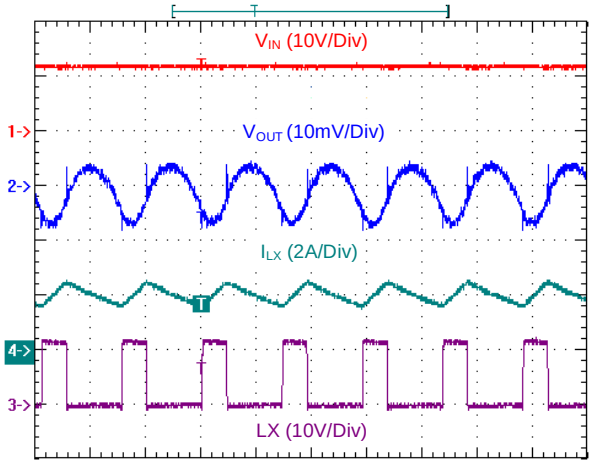
400us/Div
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A

Steady State Waveforms



100us/Div
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A at PSM

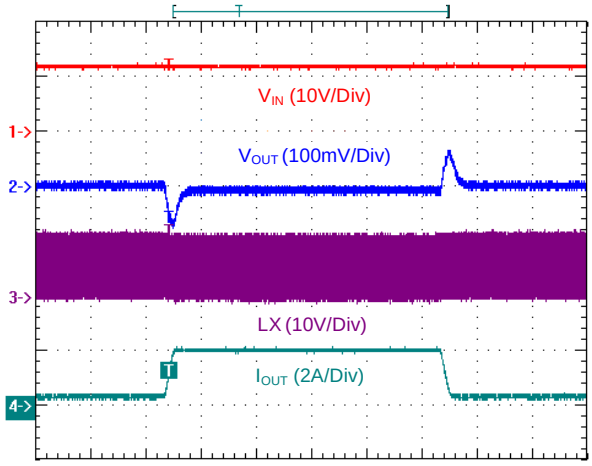
Steady State Waveforms



2us/Div
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A at PSM

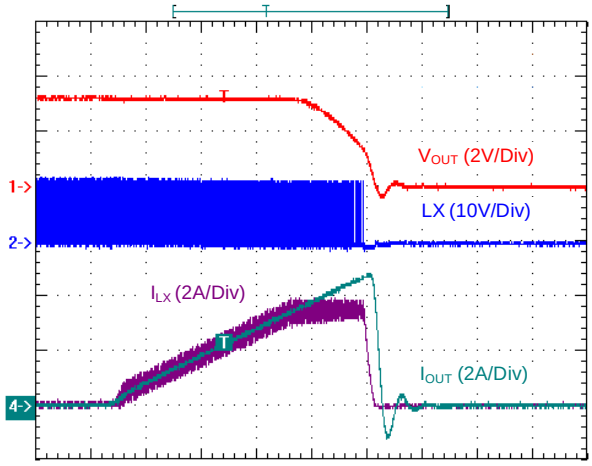
Typical Operation Characteristics

Load Transient Waveforms



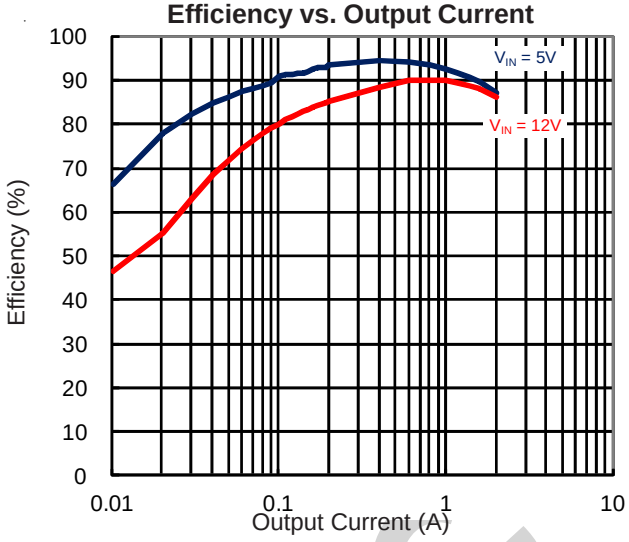
200us/Div
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A

Current Limit Waveforms



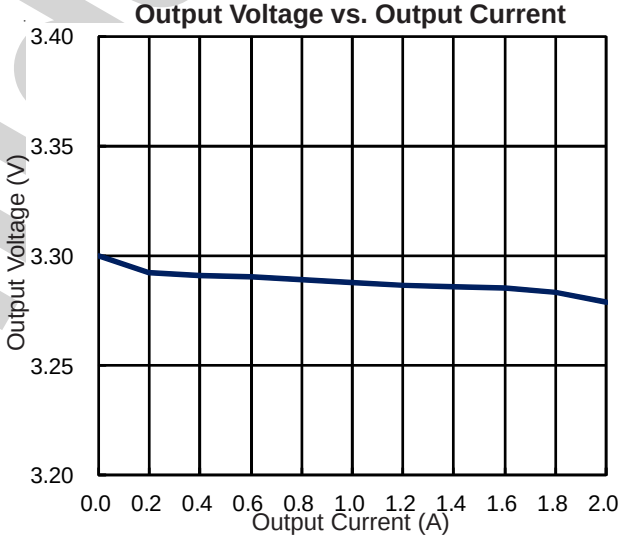
100us/Div
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A

Efficiency vs. Output Current



V_{IN} = 5V ~ 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ 2A

Output Voltage vs. Output Current



V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ 2A

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Application Information

Output Inductor Selection

Output inductor selection is usually based the considerations of inductance, rated current value, size requirements and DC resistance (DCR).

The inductance is chosen based on the desired ripple current. Large value inductors result in lower ripple currents and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in the equation below. A reasonable starting point for setting ripple current is ΔIL = 900mA (30% of 3000mA). For most applications, the value of the inductor will fall in the range of 1uH to 10uH.

$$\Delta IL = \frac{1}{(f_{OSC} \times L_{OUT})} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current. If possible, choose an inductor with rated current higher than 4.3A so that it will not saturate even under current limit condition.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size, current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends on the price vs. size requirements and any radiated field/EMI requirements.

Input Capacitor Selection

The buck converter draws pulsed current with sharp edges from the input capacitor resulting in ripple and noise at the input supply voltage. A minimum 10uFx2 X5R or X7R ceramic capacitor is highly recommended to filter the pulsed current. The input capacitor should be placed as near the device as possible to avoid the stray inductance along the connection trace. Y5V dielectrics, aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

The capacitor with low ESR (equivalent series resistance) provides the small drop voltage to stabilize the input voltage during the transient loading. For input capacitor selection, the ceramic capacitor larger than 10uFx2 is recommend. The capacitor must conform to the RMS current requirement. The maximum RMS ripple current is calculated as:

$$\Delta V_{OUT} = \Delta I_C \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

This formula has a maximum at V_{IN} = 2xV_{OUT}, where I_{IN}(RMS) = I_{OUT}(MAX)/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

Using Ceramic Capacitors

Higher value, lower cost ceramic capacitors are now available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used to achieve very low output ripple and small circuit size.

However, care must be taken when these capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part. When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{OUT} x ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{OUT} also begins to discharge or charge C_{OUT}, which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

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PCB Layout Considerations

High switching frequencies and relatively large peak currents make the PCB layout a very important part of switching mode power supply design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Follow the PCB layout guidelines for optimal performance of uP1723.

1 For the main current paths, keep their traces short, direct and wide.

2 Put the input/output capacitors as close as possible to the device pins.

3 LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.

4 Connect feedback network behind the output capacitors. Place the feedback components near the uP1723 and keep the loop area small. .

5 A ground plane is preferred, but if not available, keep the signal and power grounds separated with small signal components returning to the GND pin at one point. They should not share the high current path of C_{IN} or C_{OUT}.

6 Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{IN} or GND.

7 An example of 2-layer PCB layout is shown in Figure 1 for reference.

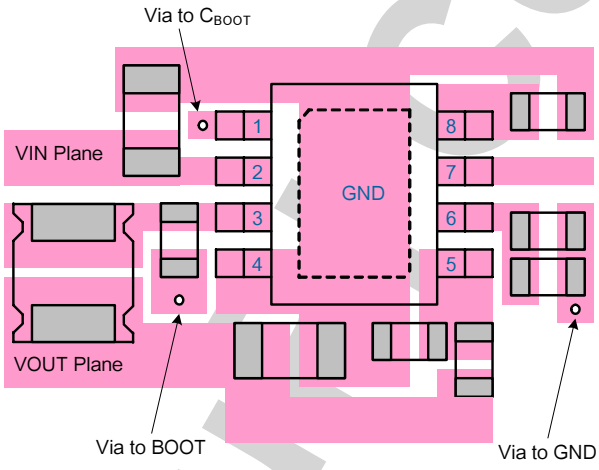
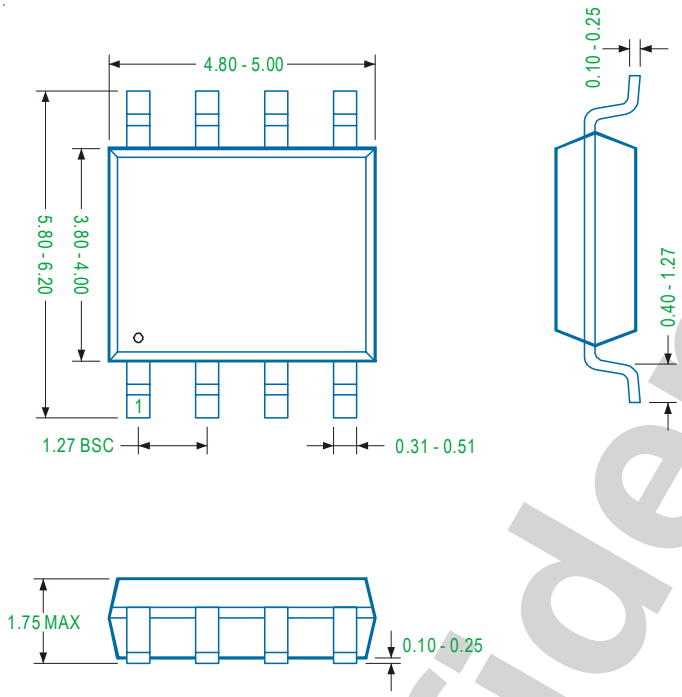


Figure 1. Top Layer Layout Example.

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Package Information

SOP - 8L



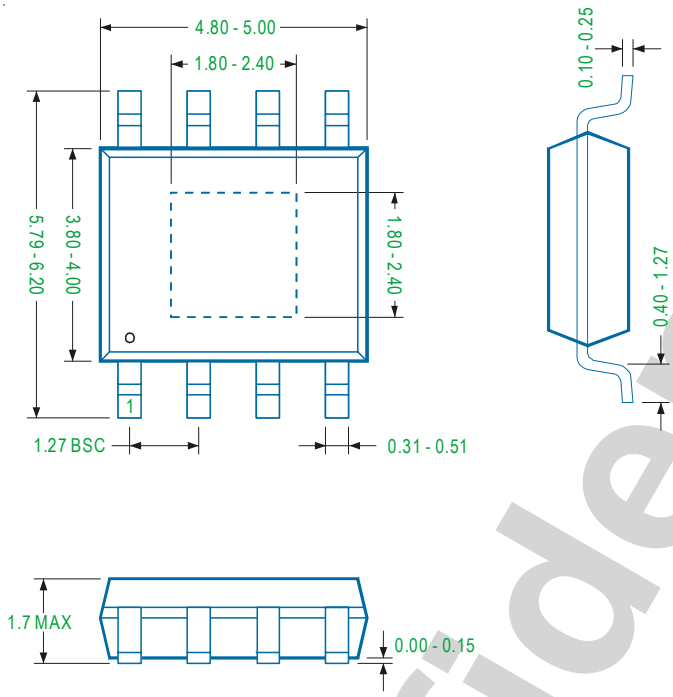
Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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Package Information

PSOP - 8L



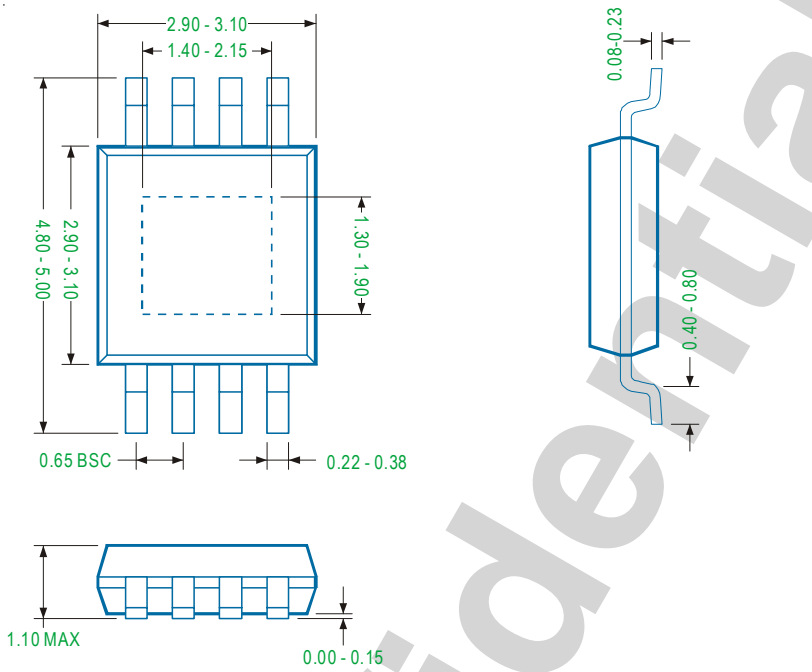
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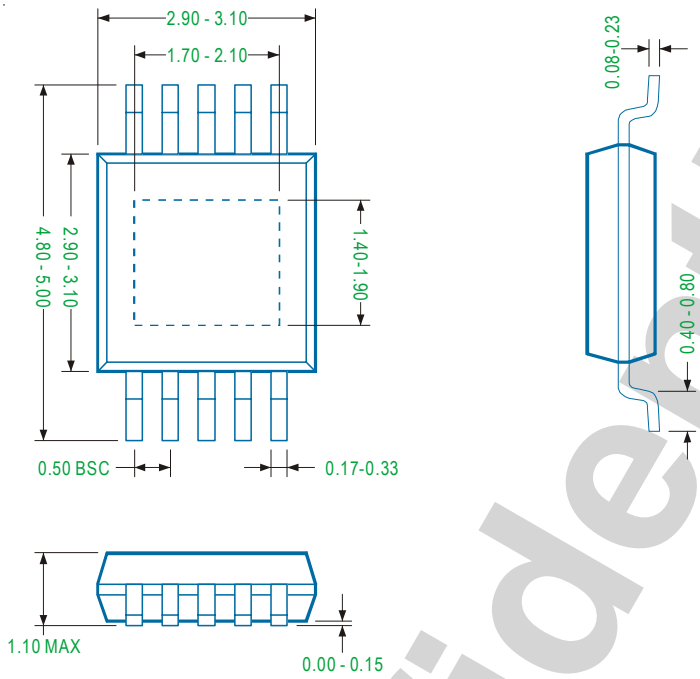
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