CY7C341B

192-Macrocell MAX® EPLD

Features

- **192 macrocells in 12 logic array blocks (LABs)**
- **Eight dedicated inputs, 64 bidirectional I/O pins**
- **Advanced 0.65-micron CMOS technology to increase performance**
- **Programmable interconnect array**
- **384 expander product terms**
- **Available in 84-pin HLCC, PLCC, and PGA packages**

Functional Description

The CY7C341B is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX® architecture is 100% user-configurable, allowing the devices to accommodate a variety of independent logic functions.

The 192 macrocells in the CY7C341B are divided into 12 Logic Array Blocks (LABs), 16 per LAB. There are 384 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

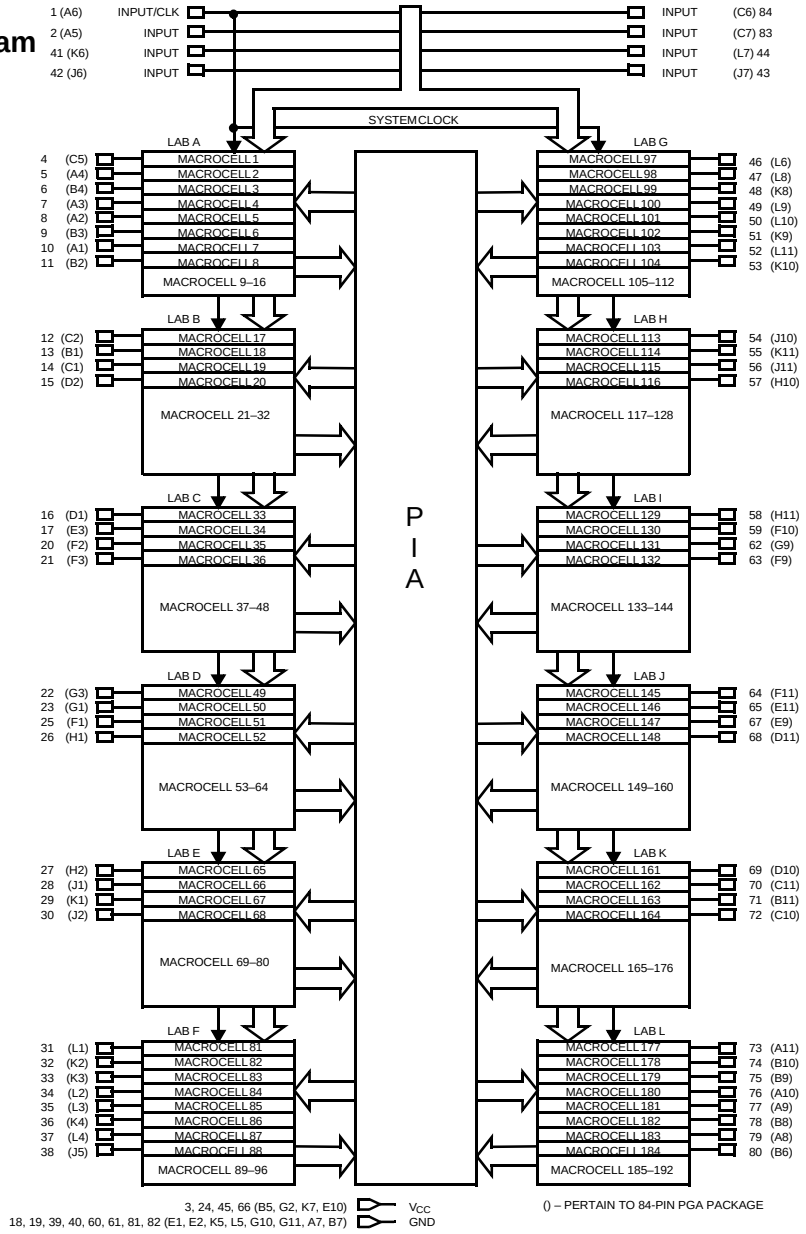
The speed and density of the CY7C341B allows it to be used in a wide range of applications, from replacement of large amounts of 7400-series TTL logic, to complex controllers and multifunction chips. With greater than 37 times the functionality of 20-pin PLDs, the CY7C341B allows the replacement of over 75 TTL devices. By replacing large amounts of logic, the CY7C341B reduces board space, part count, and increases system reliability.

Each LAB contains 16 macrocells. In LABs A, F, G, and L, 8 macrocells are connected to I/O pins and eight are buried, while for LABs B, C, D, E, H, I, J, and K, four macrocells are connected to I/O pins and 12 are buried. Moreover, in addition to the I/O and buried macrocells, there are 32 single product term logic expanders in each LAB. Their use greatly enhances the capability of the macrocells without increasing the number of product terms in each macrocell.

Selection Guide

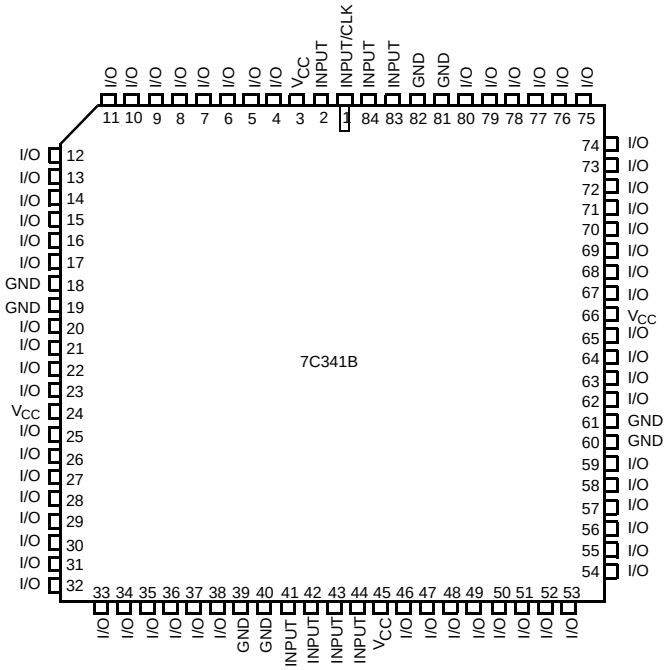
	7C341B-25	7C341B-35	Unit
Maximum Access Time	25	35	ns

Logic Block Diagram



Pin Configurations

PLCC/HLCC Top View



PGA Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L	I/O	I/O	I/O	I/O	GND	I/O	INPUT	I/O	I/O	I/O	I/O
K	I/O	I/O	I/O	I/O	GND	INPUT	V_{CC}	I/O	I/O	I/O	I/O
J	I/O	I/O			I/O	INPUT	INPUT			I/O	I/O
H	I/O	I/O								I/O	I/O
G	I/O	V_{CC}	I/O			7C341B			I/O	GND	GND
F	I/O	I/O	I/O						I/O	I/O	I/O
E	GND	GND	I/O						I/O	V_{CC}	I/O
D	I/O	I/O								I/O	I/O
C	I/O	I/O	■		I/O	INPUT	INPUT			I/O	I/O
B	I/O	I/O	I/O	I/O	V_{CC}	I/O	GND	I/O	I/O	I/O	I/O
A	I/O	I/O	I/O	I/O	INPUT	INPUT/ CLK	GND	I/O	I/O	I/O	I/O

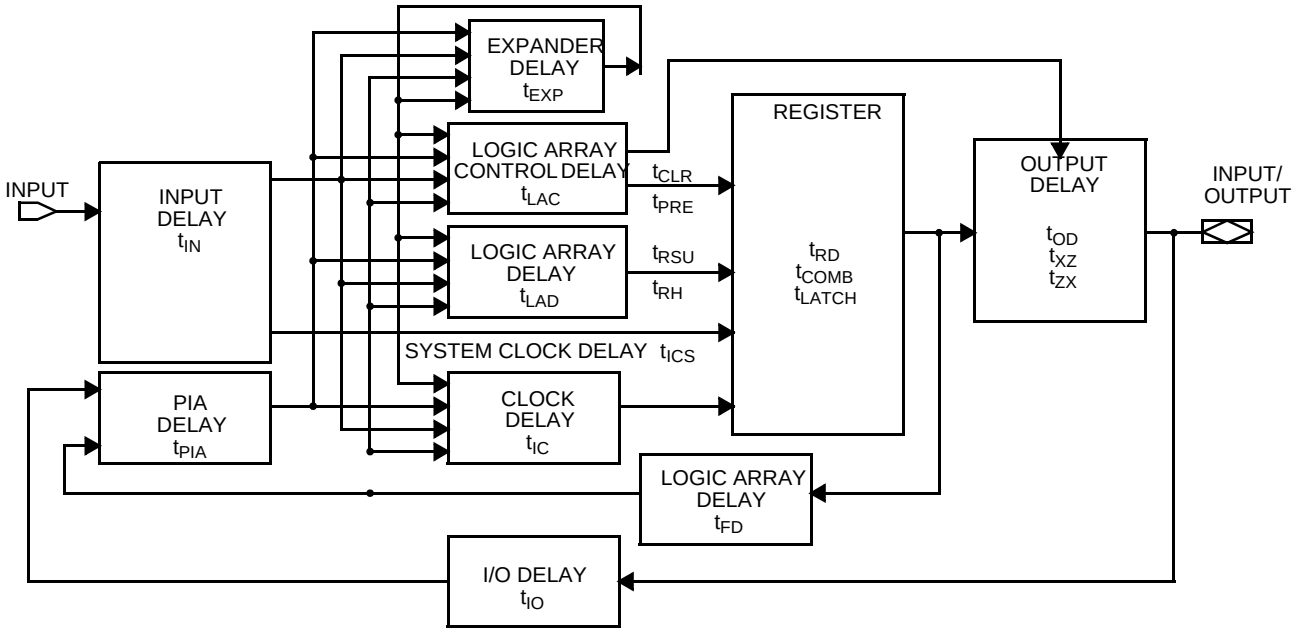
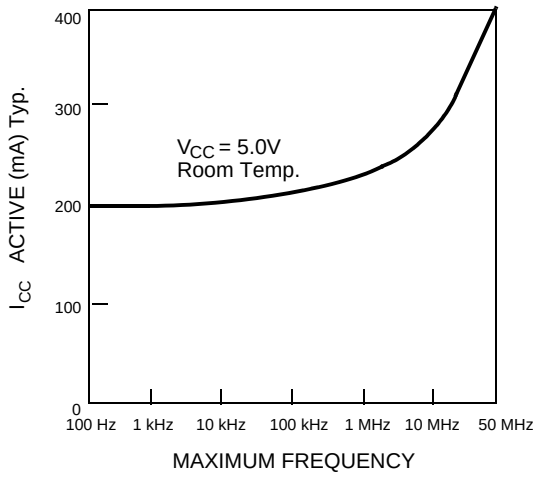


Figure 1. CY7C341B Internal Timing Model

Logic Array Blocks

There are 12 logic array blocks in the CY7C341B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C341B provides eight dedicated inputs, one of which may be used as a system clock. There are 64 I/O pins that may be individually configured for input, output, or bidirectional data flow.



Typical I_{CC} vs. f_{MAX}

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Design Recommendations

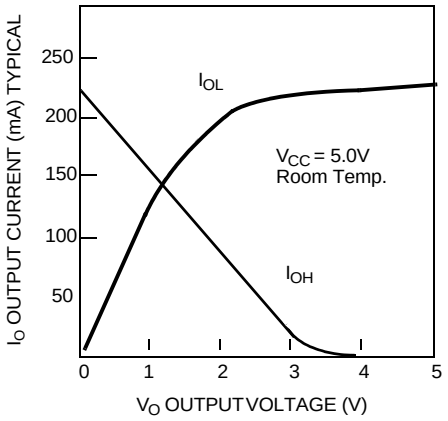
For proper operation, input and output pins must be constrained to the range GND ≤ (VIN or VOUT) ≤ VCC. Unused inputs must always be tied to an appropriate logic level (either VCC or GND). Each set of VCC and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 mF must be connected between VCC and GND. For the most effective decoupling, each VCC pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Design Security

The CY7C341B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

The CY7C341B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.



Output Drive Current

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....-65°C to +135°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Maximum Junction Temperature (Under Bias).....150°C

Supply Voltage to Ground Potential[1].....–2.0V to +7.0V

DC Output Current, per Pin[1]..... –25 mA to +25 mA

DC Input Voltage[1].....–2.0V to +7.0V

Operating Range[3]

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	–40°C to +85°C	5V ± 10%

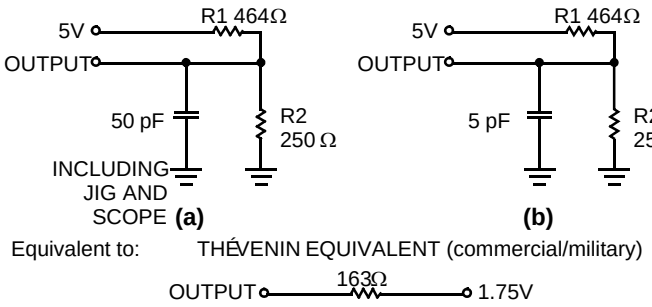
Electrical Characteristics Over the Operating Range

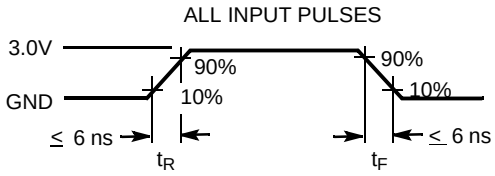
Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{CC}	Output HIGH Voltage	Maximum V_{CC} rise time is 10 ms	4.75(4.5)	5.25(5.5)	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA[2]	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA[2]		0.45	V
V_{IH}	Input HIGH Level		2.0	V_{CC}+ 0.3	V
V_{IL}	Input LOW Level		–0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}	–10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND	–40	+40	µA
t_R (Recommended)	Input Rise Time			100	ns
t_F (Recommended)	Input Fall Time			100	ns

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1.0 MHz	20	pF

AC Test Loads and Waveforms





Notes:

1. Minimum DC input is –0.3V. During transactions, input may undershoot to –2.0V or overshoot to 7.0V for input currents less then 100 mA and periods shorter than 20 ns.
2. The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
3. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.

External Switching Characteristics Over the Operating Range

Parameter	Description		7C341B-25 Min.	7C341B-25 Max.	7C341B-35 Min.	7C341B-35 Max.	Unit
t_{PD1}	Dedicated Input to Combinatorial Output Delay[4]	Commercial		25		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[4]	Commercial		40		55	ns
t_{SU}	Global Clock Set-up Time	Commercial	15		25		ns
t_{CO1}	Synchronous Clock Input to Output Delay[4]	Commercial		14		20	ns
t_{H}	Input Hold Time from Synchronous Clock Input	Commercial	0		0		ns
t_{WH}	Synchronous Clock Input High Time	Commercial	8		12.5		ns
t_{WL}	Synchronous Clock Input Low Time	Commercial	8		12.5		ns
f_{MAX}	Maximum Register Toggle Frequency[5]	Commercial	62.5		40.0		MHz
t_{ACO1}	Dedicated Asynchronous Clock Input to Output Delay[4]	Commercial		25		35	ns
t_{AS1}	Dedicated Input or Feedback Set-up Time to Asynchronous Clock Input	Commercial	5		10		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input	Commercial	6		10		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[6]	Commercial	11		16		ns
t_{AWL}	Asynchronous Clock Input LOW Time[6]	Commercial	9		14		ns
t_{CNT}	Minimum Global Clock Period	Commercial		20		30	ns
t_{ODH}	Output Data Hold Time After Clock	Commercial	2		2		ns
f_{CNT}	Maximum Internal Global Clock Frequency[7]	Commercial	50		33.3		MHz
t_{ACNT}	Minimum Internal Array Clock Frequency	Commercial		20		30	ns
f_{ACNT}	Maximum Internal Array Clock Frequency[7]	Commercial	50		33.3		MHz

Internal Switching Characteristics Over the Operating Range

Parameter	Description		7C341B-25 Min.	7C341B-25 Max	7C341B-35 Min.	7C341B-35 Max	Unit
t_{IN}	Dedicated Input Pad and Buffer Delay	Commercial		5		11	ns
t_{IO}	I/O Input Pad and Buffer Delay	Commercial		6		11	ns
t_{EXP}	Expander Array Delay	Commercial		12		20	ns
t_{LAD}	Logic Array Data Delay	Commercial		12		14	ns
t_{LAC}	Logic Array Control Delay	Commercial		10		13	ns
t_{OD}	Output Buffer and Pad Delay[4]	Commercial		5		6	ns
t_{ZX}	Output Buffer Enable Delay[4]	Commercial		10		13	ns
t_{XZ}	Output Buffer Disable Delay[8]	Commercial		10		13	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Commercial	6		12		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Commercial	4		8		ns
t_{LATCH}	Flow-Through Latch Delay	Commercial		3		4	ns
t_{RD}	Register Delay	Commercial		1		2	ns
t_{COMB}	Transparent Mode Delay	Commercial		3		4	ns
t_{IC}	Asynchronous Clock Logic Delay	Commercial		14		16	ns
t_{ICS}	Synchronous Clock Delay	Commercial		3		1	ns

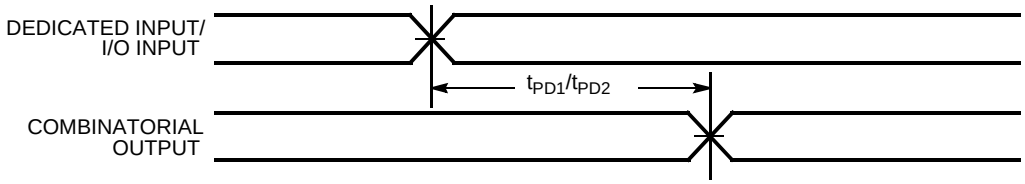
Notes:
4. C1 = 35 pF.
5. The f_{MAX} values represent the highest frequency for pipeline data.
6. This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameter must be swapped.
7. This parameter is measured with a 16-bit counter programmed into each LAB.
8. C1 = 5 pF.

Internal Switching Characteristics Over the Operating Range (continued)

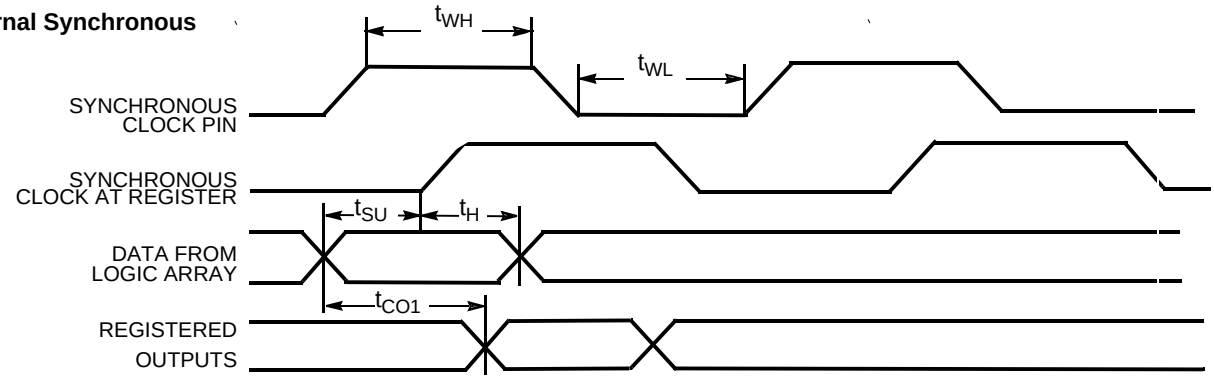
Parameter	Description		7C341B-25		7C341B-35		Unit
			Min.	Max	Min.	Max	
t_{FD}	Feedback Delay	Commercial		1		2	ns
t_{PRE}	Asynchronous Register Preset Time	Commercial		5		7	ns
t_{CLR}	Asynchronous Register Clear Time	Commercial		5		7	ns
t_{PIA}	Programmable Interconnect Array Delay	Commercial		14		20	ns

Switching Waveforms

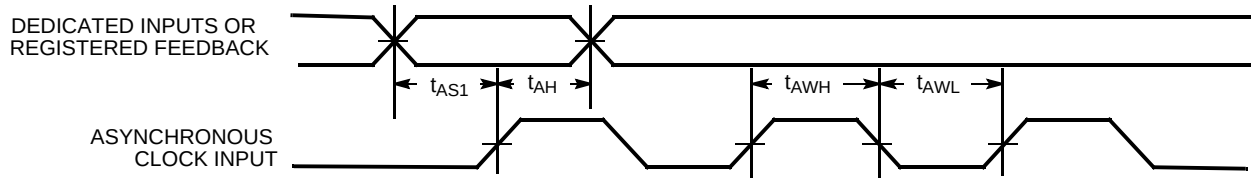
External Combinatorial



External Synchronous

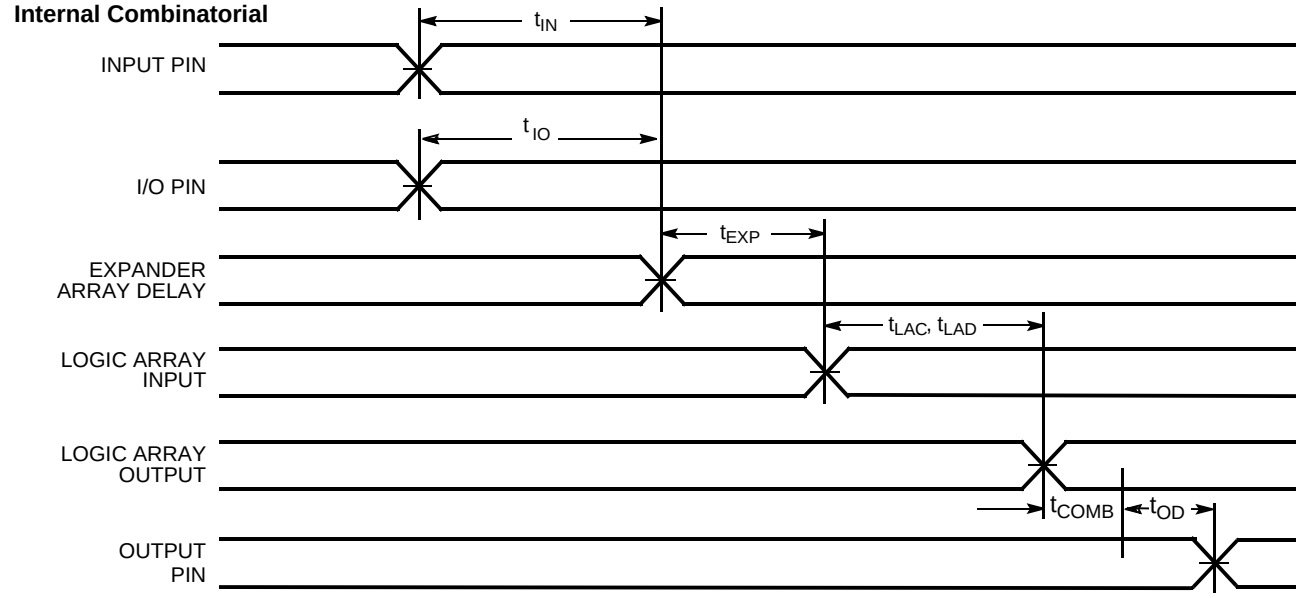


External Asynchronous

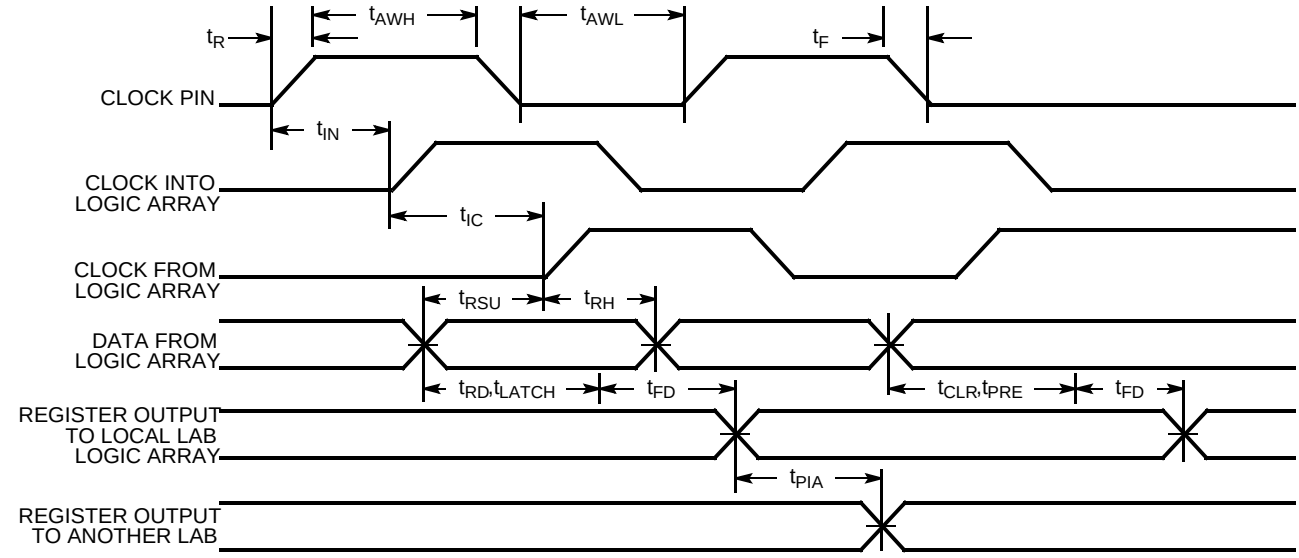


Switching Waveforms (continued)

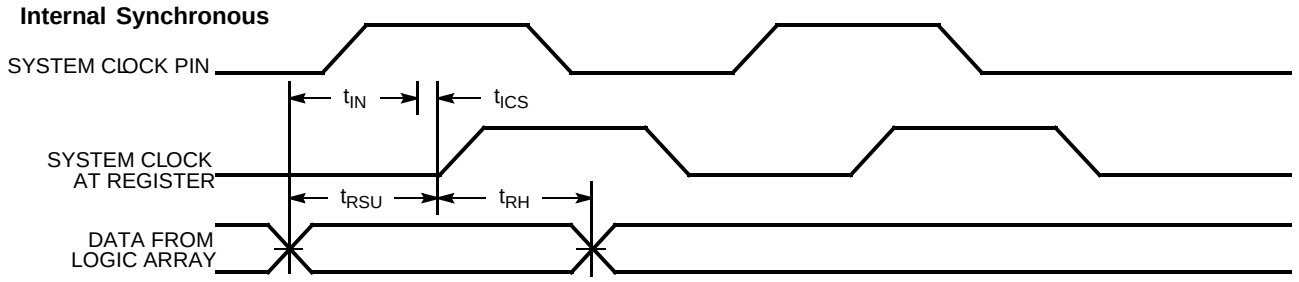
Internal Combinatorial



Internal Asynchronous

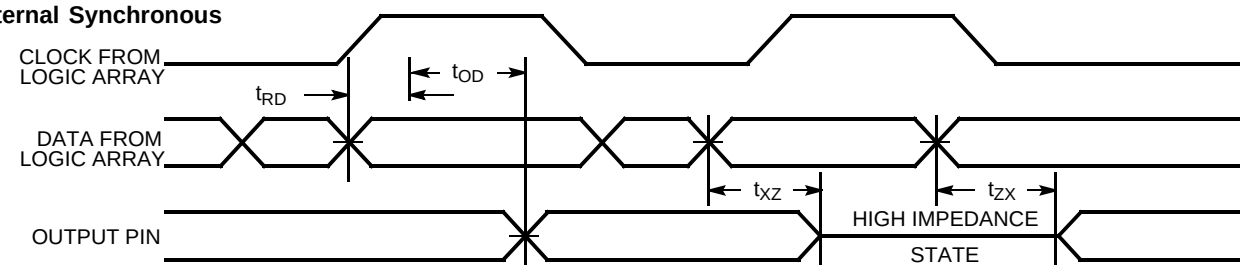


Internal Synchronous



Switching Waveforms (continued)

Internal Synchronous

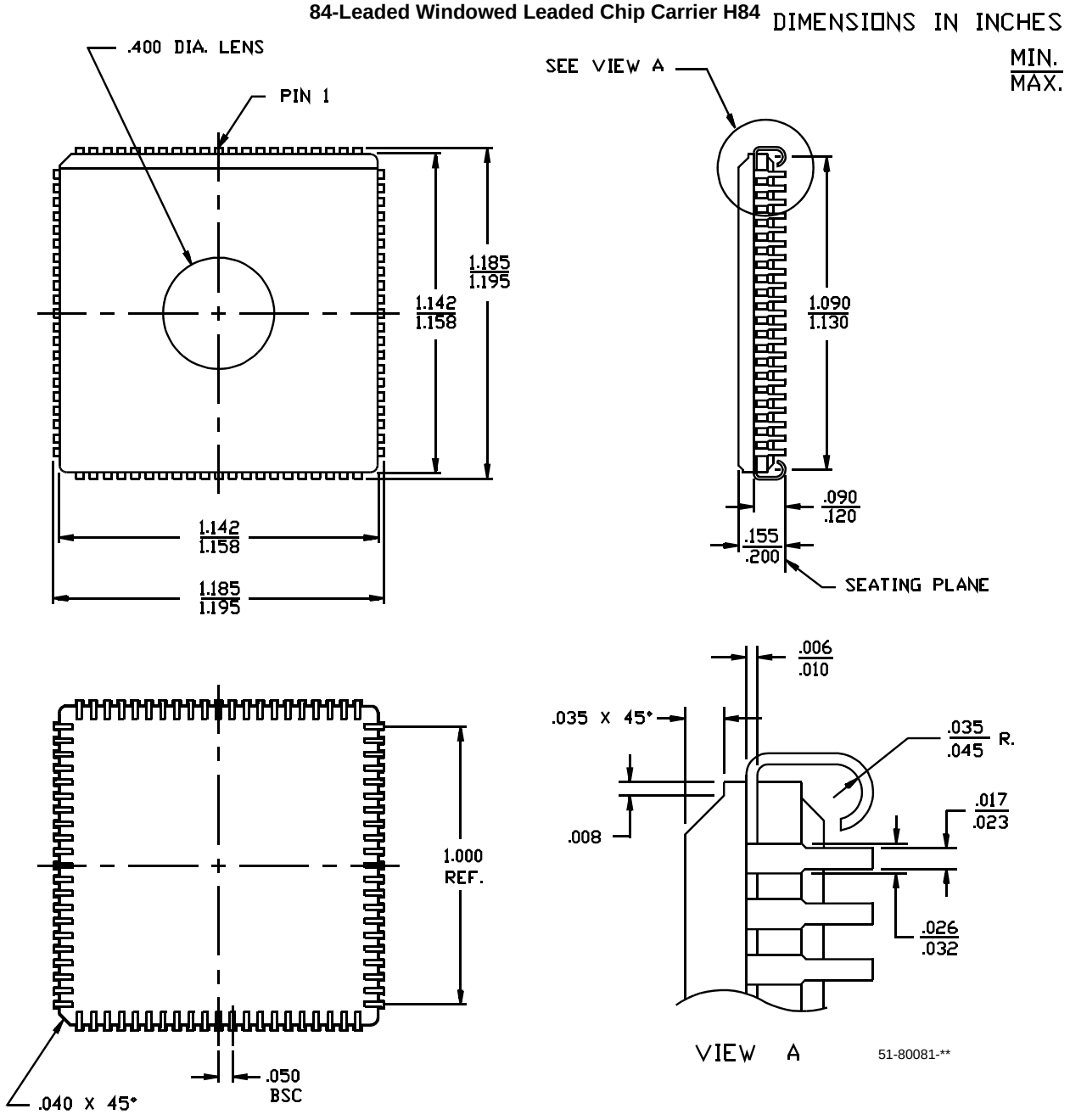


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C341B-25HC/HI	H84	84-lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341B-25JC/JI	J83	84-lead Plastic Leaded Chip Carrier	
	CY7C341B-25RC/RI	R84	84-lead Windowed Pin Grid Array	
35	CY7C341B-35HC/HI	H84	84-lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C341B-35JC/JI	J83	84-lead Plastic Leaded Chip Carrier	
	CY7C341B-35RC/RI	R84	84-lead Windowed Pin Grid Array	

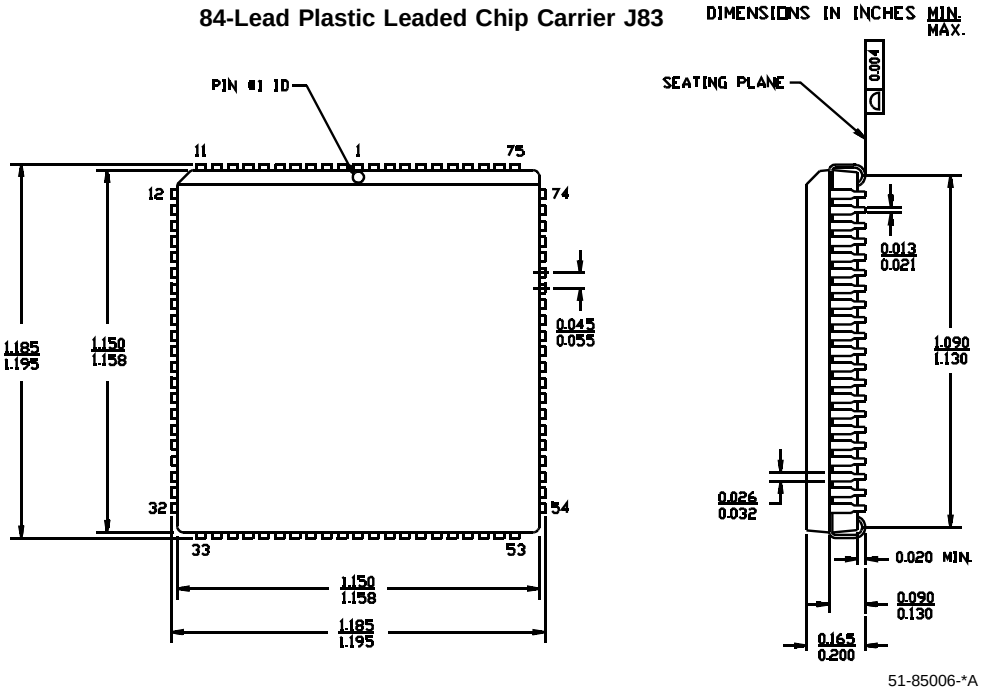
Package Diagrams

84-Leaded Windowed Leaded Chip Carrier H84



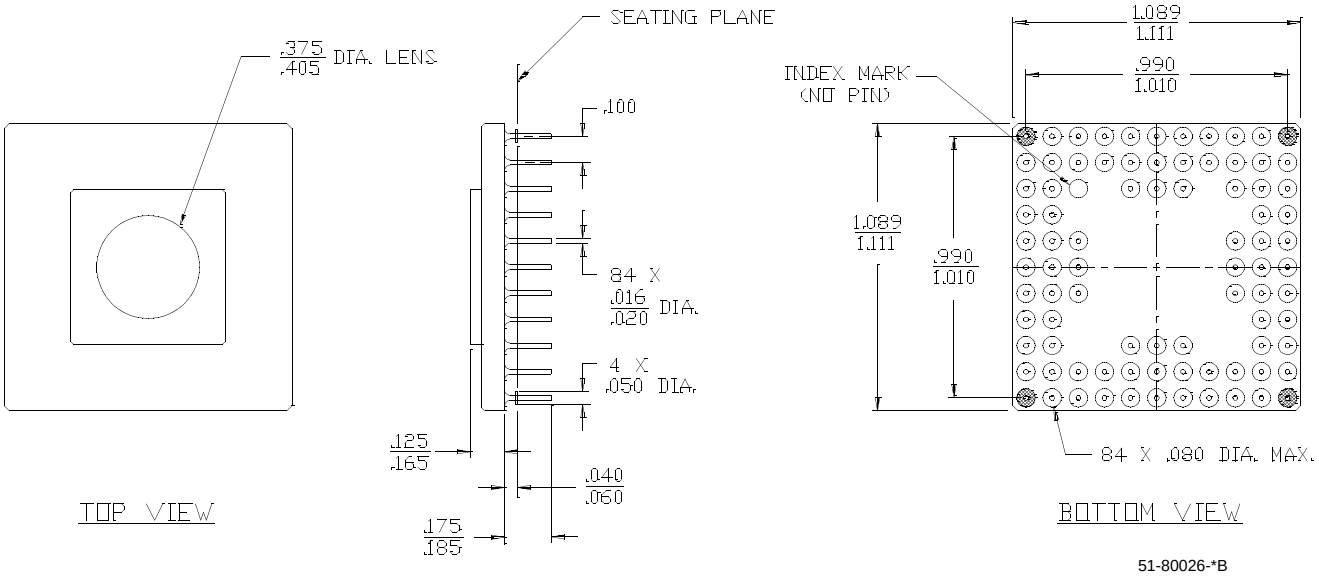
Package Diagrams (continued)

84-Lead Plastic Leaded Chip Carrier J83



51-85006-*A

84-Lead Windowed Pin Grid Array R84



51-80026-*B

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Document History Page

Document Title: CY7C341B 192-Macrocell MAX® EPLD Document Number: 38-03016				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106316	05/17/01	SZV	Change from ecn #: 38-00137 to 38-03016
*A	113613	04/11/02	OOR	PGA package diagram dimensions were updated
*B	122227	12/28/02	RBI	Power-up requirements added to Operating Range Information
*C	213375	See ECN	FSG	Added note to title page: “Use Ultra37000 For All New Designs”