PART NUMBER: VEFT1-SMT **DESCRIPTION:** single output series dc-dc converter

Description

Designed to convert fixed voltages into an isolated voltage, the VEFT1-SMT single series is well suited for providing board-mount local supplies in a wide range of applications, including mixed analog/digital circuits, test & measurement equip., process/machine controls, datacom/telecom fields, etc...

The semi-regulated output can be followed by 3-terminal regulators to provide output protection, in addition to output regulation.

Features

- **Isolated 1 W output**
- **Temperature range: -40°C~+85°C**
- **Unregulated**
- **High efficiency to 80%**
- **Single voltage output**
- **Small footprint**
- **SMD package style**
- **Industry standard pinout**
- **UL94-V0 package**
- **No heatsink required**
- **3K Vdc isolation**
- **Power density 0.85 W/cm³**
- **No external component required**
- **Low cost**

RoHS

MODEL	Input Voltage		Output	Output Current			Package	
	Nominal	Range	Voltage	Max.	Min.	Efficiency	Style	UL60950-1
VEFT1-S3.3-S3.3-SMT	3.3 Vdc	3.00~3.60 Vdc	3.3 Vdc	300 mA	30 mA	72%	SMD	NO
VEFT1-S3.3-S5-SMT	3.3 Vdc	3.00~3.60 Vdc	5 Vdc	200 mA	20 mA	73%	SMD	NO
VEFT1-S5-S3.3-SMT	5 Vdc	4.5~5.5 Vdc	3.3 Vdc	300 mA	30 mA	74%	SMD	NO
VEFT1-S5-S5-SMT	5 Vdc	4.5~5.5 Vdc	5 Vdc	200 mA	20 mA	70%	SMD	YES
VEFT1-S5-S9-SMT	5 Vdc	4.5~5.5 Vdc	9 Vdc	111 mA	12 mA	75%	SMD	YES
VEFT1-S5-S12-SMT	5 Vdc	4.5~5.5 Vdc	12 Vdc	83 mA	9 mA	78%	SMD	YES
VEFT1-S5-S15-SMT	5 Vdc	4.5~5.5 Vdc	15 Vdc	67 mA	7 mA	80%	SMD	YES
VEFT1-S5-S24-SMT	5 Vdc	4.5~5.5 Vdc	24 Vdc	42 mA	5 mA	78%	SMD	NO
VEFT1-S12-S3.3-SMT	12 Vdc	10.8~13.2 Vdc	3.3 Vdc	300 mA	30 mA	75%	SMD	NO
VEFT1-S12-S5-SMT	12 Vdc	10.8~13.2 Vdc	5 Vdc	200 mA	20 mA	72%	SMD	YES
VEFT1-S12-S9-SMT	12 Vdc	10.8~13.2 Vdc	9 Vdc	111 mA	12 mA	76%	SMD	YES
VEFT1-S12-S12-SMT	12 Vdc	10.8~13.2 Vdc	12 Vdc	83 mA	9 mA	79%	SMD	YES
VEFT1-S12-S15-SMT	12 Vdc	10.8~13.2 Vdc	15 Vdc	67 mA	7 mA	81%	SMD	YES
VEFT1-S12-S24-SMT	12 Vdc	10.8~13.2 Vdc	24 Vdc	42 mA	5 mA	79%	SMD	NO
VEFT1-S24-S3.3-SMT	24 Vdc	21.6~26.4 Vdc	3.3 Vdc	300 mA	30 mA	73%	SMD	NO
VEFT1-S24-S5-SMT	24 Vdc	21.6~26.4 Vdc	5 Vdc	200 mA	20 mA	79%	SMD	NO
VEFT1-S24-S9-SMT	24 Vdc	21.6~26.4 Vdc	9 Vdc	111 mA	12 mA	80%	SMD	NO
VEFT1-S24-S12-SMT	24 Vdc	21.6~26.4 Vdc	12 Vdc	83 mA	9 mA	81%	SMD	NO
VEFT1-S24-S15-SMT	24 Vdc	21.6~26.4 Vdc	15 Vdc	67 mA	7 mA	79%	SMD	NO
VEFT1-S24-S24-SMT	24Vdc	21.6~26.4 Vdc	24 Vdc	42 mA	5 mA	80%	SMD	NO

OUTPUT SPECIFICATIONS

Item	Test conditions	Min.	Typ.	Max.	Units
Output power		0.1		1	W
Line Regulation	For Vin change of 1%			1.2	%
Load Regulation	10% to 100% full load		10	15	%
Output voltage accuracy	See tolerance envelope graph				
Temperature drift	@ 100% load			0.03	%/°C
Output ripple	20 MHz Bandwidth		75	150	mVp-p
Switching frequency	Full load, nominal input	100	125	160	KHz

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GENERAL SPECIFICATIONS

Short circuit protection		<1 second
Temperature rise at full load		25°C Max, 15°C Typ.
Cooling		Free air convection
Operating temperature range		-40°C to +85°C
Storage temperature range		-55°C to +125°C
Soldering temperature		300°C (1.5mm from case for 10 sec.)
Storage humidity range		<95%
Case material		Plastic (UL94-V0)
Safety[2]		approved to UL60950-1 (E222736)
MTBF		>3,500,000 hrs.
Burn-in	Full load at +85°C, for 4 hours at no-load and 4 hours at full load.	

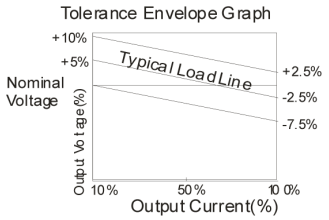
ISOLATION SPECIFICATIONS

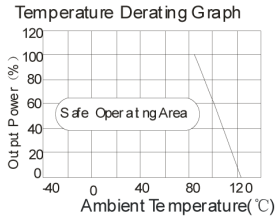
Item	Test Conditions	Min.	Typ.	Max.	Units
Isolation Voltage	Tested for 1 min.	3000			Vdc
Insulation Resistance	Test at 500 Vdc	1000			M Ω

Note:

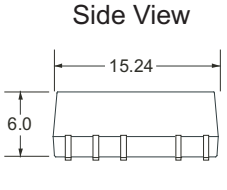
1. All specifications measured at TA=25°C, humidity <75%, nominal input voltage and rated output load unless otherwise specified.
2. See table on page 1 for available models

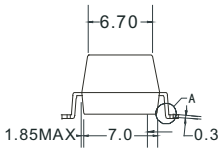
TYPICAL CHARACTERISTICS

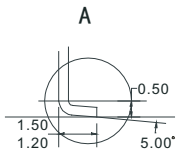


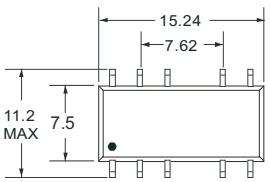


OUTLINE DIMENSIONS & RECOMMENDED LAYOUT PATTERN

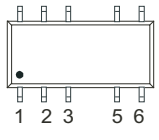








Pin	Function
1	-Vin
2	+Vin
3	NC
5	-Vout
6	NC



Pin	Function
7	NC
8	+Vout
10	NC
11	NC
12	NC

Note: All Pins on a 2.54mm pitch; all pin diameters are 0.50mm; all dimensions in mm.

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APPLICATION NOTES:

- Input filtering

To reduce the reflected ripple current and minimize EMI, especially when the converter input is more than 2" away from the DC source, it is recommended to connect a low ESR electrolytic capacitor between Vin and Gnd. The values suggested are as shown in Table 1. If additional filtering is required, the capacitance may be increased, or expanded to an LC network as shown in Figure 1.

TABLE 1

Input Voltage	External Input Capacitance
5 V	4.7 µF
12 V	2.2 µF
24 V	1.0 µF

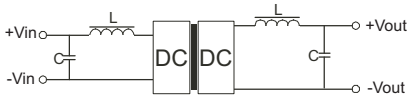
- Output filtering

An output capacitor is needed to meet output ripple requirements as shown in Table 2.

Output capacitance may be increased for additional filtering, but should not exeed 10µF or expanded to an LC network as in Figure 1.

TABLE 2

Vout	External Ouput Capacitance
5 V	10 µF
9 V	4.7 µF
12 V	2.2 µF
15 V	1 µF
24 V	0.47 µF



<Figure 1>

- Minimum loading

The converter needs a minimum of 10% loading to maintain output regulation. Operation under no-load conditions will not cause immediate damages but may reduce reliability, and cause performance not to meet specifications.

- Regulation

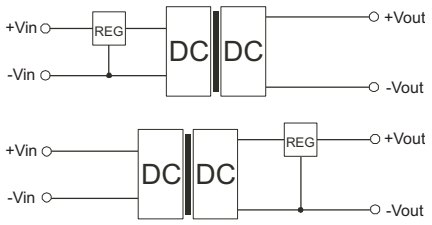
With a semi-regulated design, the converter's output voltage varies with load current and will change proportionally to the input voltage. If regulated output is needed, an external regulator can be used as shown in Figure 2.

- Protection

The converter has minimal protection against input over-voltage or output over-load, and may be permanently damaged if exposed to these conditions. An input clamping device can be used for input voltage limiting. An input fuse or an output fuse can also be used to protect against over-loading.

- External Regulator

An external 3-terminal regulator can be connected to the output of the converter to achieve full regulation. Make sure the converter's output voltage provides sufficient head room for the regulator. An additional benefit is that the built-in protection features in the regulator, such as OCP, OTP, etc, will protect the converter also. In a complimentory supply, a negative output regulator must be used to achieve the negative regulated output.



<Figure 2>