SD1731 (TH562)

RF POWER BIPOLAR TRANSISTORS
HF SSB APPLICATIONS

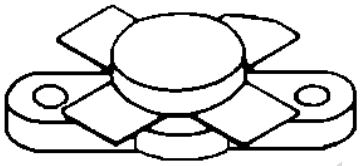
FEATURES SUMMARY

- OPTIMIZED FOR SSB
- 30 MHz
- 50 VOLTS
- EFFICIENCY 40%
- COMMON EMITTER
- GOLD METALLIZATION
- P_{OUT} = 220 W PEP WITH 13 dB GAIN

DESCRIPTION

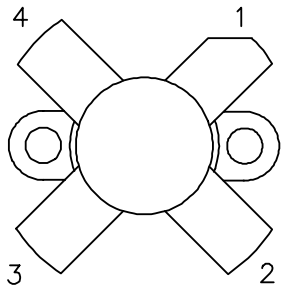
The SD1731 is a 50 V epitaxial silicon NPN planar transistor designed primarily for SSB communications. This device utilizes emitter ballasting for improved ruggedness and reliability.

Figure 1. Package



.500 4L FL (M174)
epoxy sealed

Figure 2. Pin Connection



1. Collector
2. Emitter
3. Base
4. Emitter

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Table 1. Order Codes

Order Codes	Marking	Package	Packaging
SD1731 (TH562)	SD1731	M174	PLASTIC TRAYS

Table 2. Absolute Maximum Ratings (T_{case} = 25°C)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	110	V
V_{CEO}	Collector-Emitter Voltage	55	V
V_{EBO}	Emitter-Base Voltage	4.0	V
I_C	Device Current	20	A
P_{DISS}	Power Dissipation ($T_{heatsink} \leq 25°C$)	233	W
T_J	Junction Temperature	+200	°C
T_{STG}	Storage Temperature	– 65 to +150	°C

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Junction-Case Thermal Resistance	0.55	°C/W
$R_{TH(c-s)}$	Case-Heatsink Thermal Resistance	0.2	°C/W

ELECTRICAL SPECIFICATIONS

Table 4. Static (T_{case} = 25°C)

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
BV_{CBO}	I_C = 200 mA; I_E = 0 mA	110	—	—	V
BV_{CEO}	I_C = 200 mA; I_B = 0 mA	55	—	—	V
BV_{EBO}	I_E = 20 mA; I_C = 0 mA	4.0	—	—	V
I_{CEO}	V_{CE} = 30 V; I_E = 0 mA	—	—	5	mA
I_{CES}	V_{CE} = 55 V; I_E = 0 mA	—	—	10	mA
h_{FE}	V_{CE} = 6 V; I_C = 10 A	15	—	80	—

Table 5. Dynamic ($T_{heatsink}$ = 25°C)

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
P_{OUT}	f = 30 MHz; V_{CE} = 50 V; I_{CQ} = 150 mA	220	—	—	W
G_P(1)	P_{OUT} = 220 W PEP; V_{CE} = 50 V; I_{CQ} = 150 mA	13	—	—	dB
IMD(1)	P_{OUT} = 220 W PEP; V_{CE} = 50 V; I_{CQ} = 150 mA	—	—	–30	dBc
η_c(1)	P_{OUT} = 220 W PEP; V_{CE} = 50 V; I_{CQ} = 150 mA	40	—	—	%
C_{OB}	f = 1 MHz; V_{CB} = 50 V	—	330	—	pF

Note: 1. f_1 = 30.00 MHz, f_2 = 30.001 MHz

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TYPICAL PERFORMANCE

Figure 3. Power Output PEP vs Power Input

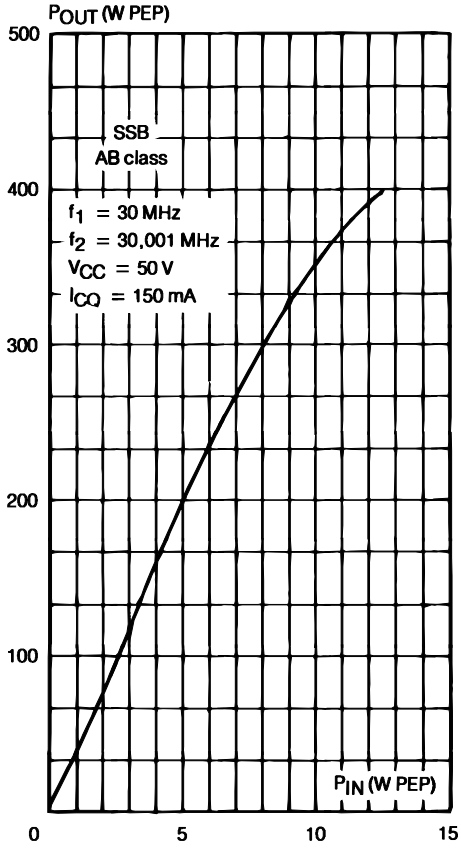


Figure 4. Collector Efficiency vs Power Output PEP

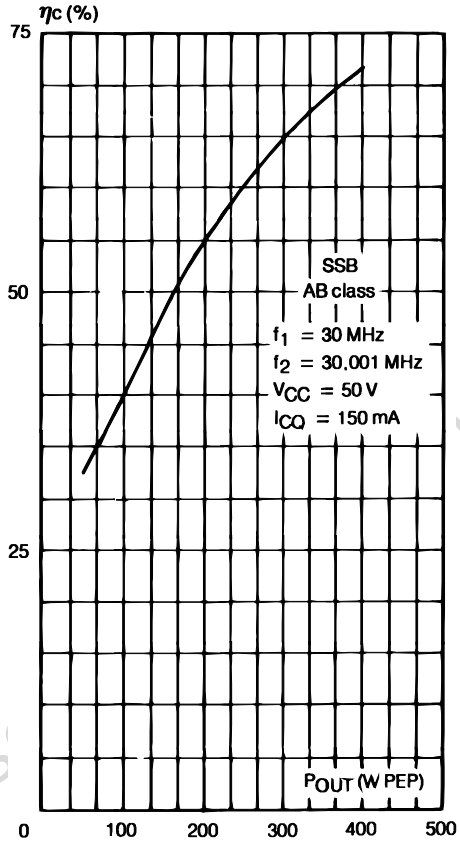


Figure 5. Intermodulation Distortion vs Power Output PEP

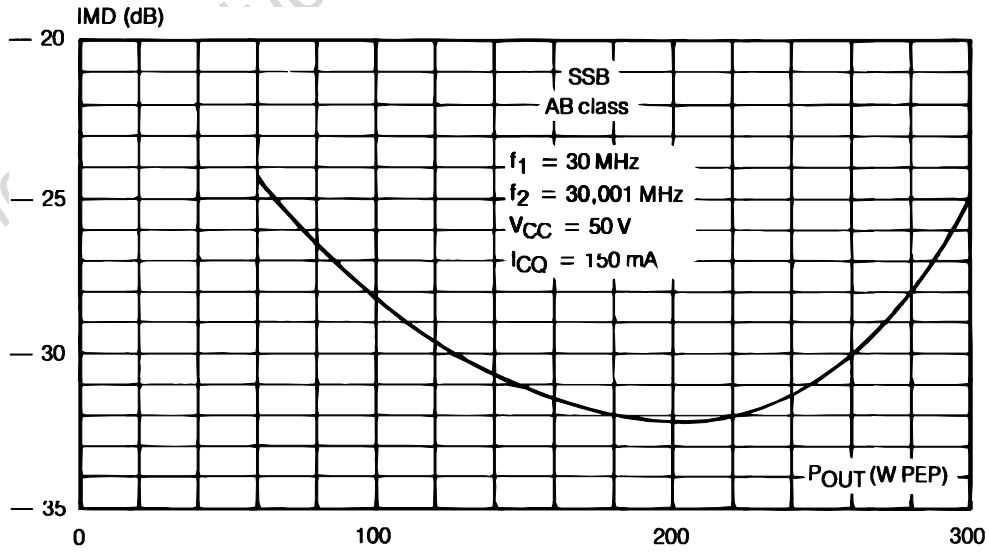


Figure 6. Power Gain vs Power Output PEP

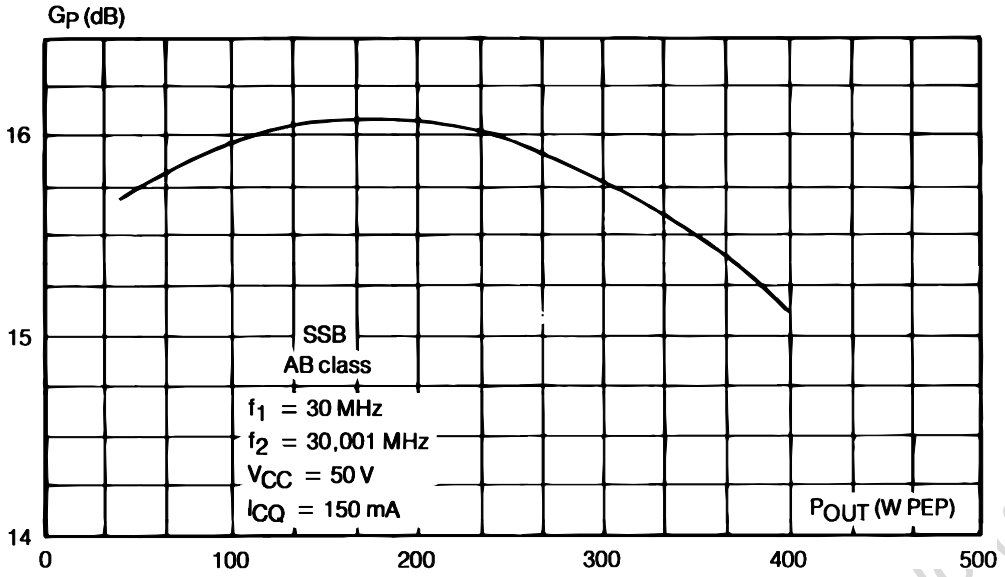
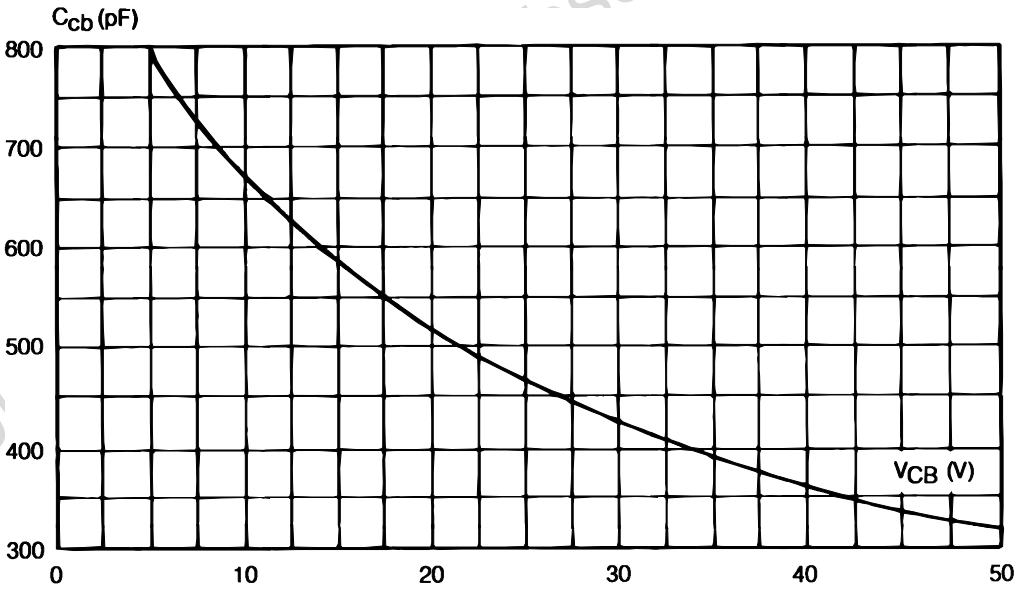


Figure 7. Collector Base Capacitance vs Collector Emitter Voltage



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TEST CIRCUIT

Figure 8. Test Circuit

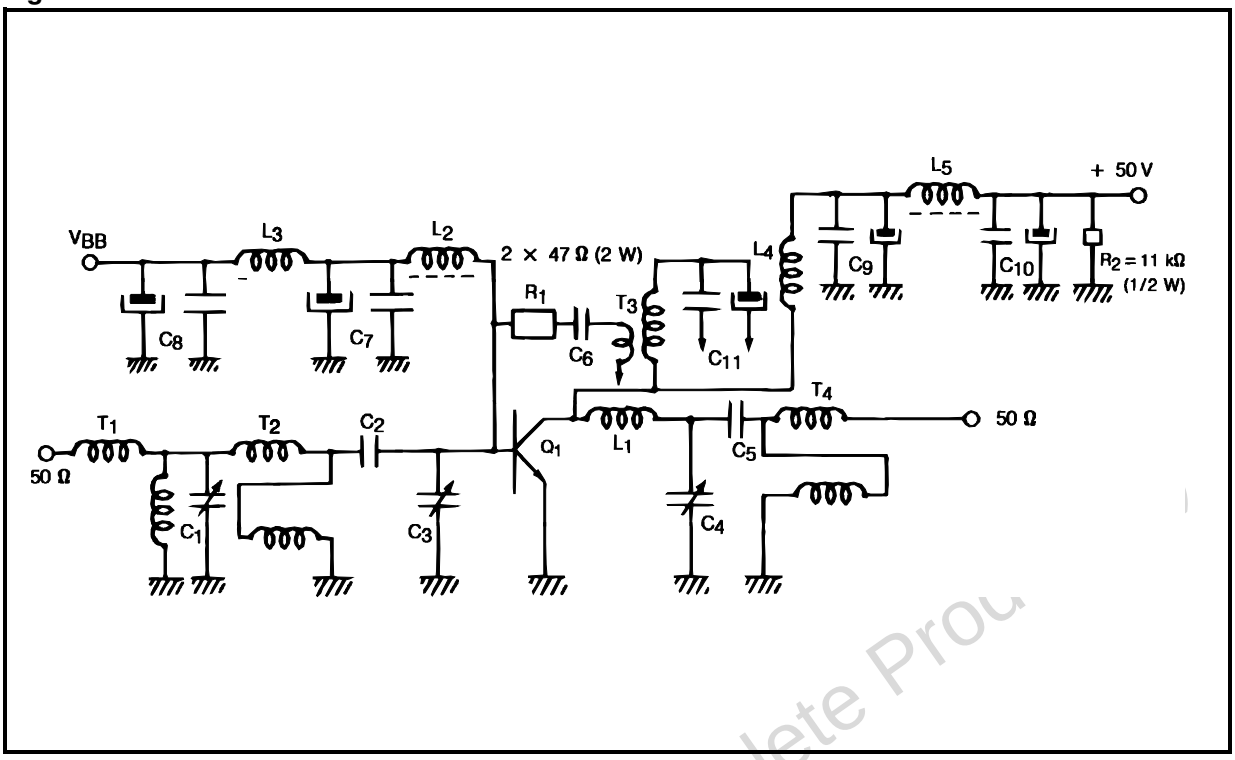

Table 6. Test Circuit

C1	Arco 426 + 220pF + 330pF Chips
C2	2 x 10nF Chips
C3	Arco 4615 + 2.2nF + 2 x 1nF LCC + 4.7nF + 560pf Chps
C4	Arco 4213 + 330pF Chip
C5	10nF Chip
C6	3 x 10nF Chips
C7, C8, C9, C10, C11	1nF + 10nF + 100nF + 4.7µF, 63V + 100µF, 63V
L1	3 Turns of 1.2mm Unenameled Wire Diameter, 7.1mm, Length 13mm
L2, L3	8 Turns of 0.55mm Enameled Wire on Ferrite Core Phillips 4C6 97170 (9 x 6 x 3)
L4	10 Turns of 1.2mm Enameled Wire, Diameter 8.1mm, Length 20mm
L5	7 Turns of 1.2mm Enameled Wire on Ferrite Core Phillips 4C6 97180
T1	6:3.5 Impedance Transformer on toriod Phillips 4C6 97180
T2	Twisted Pair 4:1 Transformer, 4 Turns Made with 1.0mm Enameled on toriod Phillips 4C6 97180
T3	Feedback Transformer Primary: 2 Turns of 1mm Enameled Wire Secondary: 8 Turns of 1mm Enameled Wire
T4	Twisted Pair 4:1 Transformer, 4 Turns of bifilar Twisted 1.2mm Wires on Ferrite Core Phillips 4C6 97200

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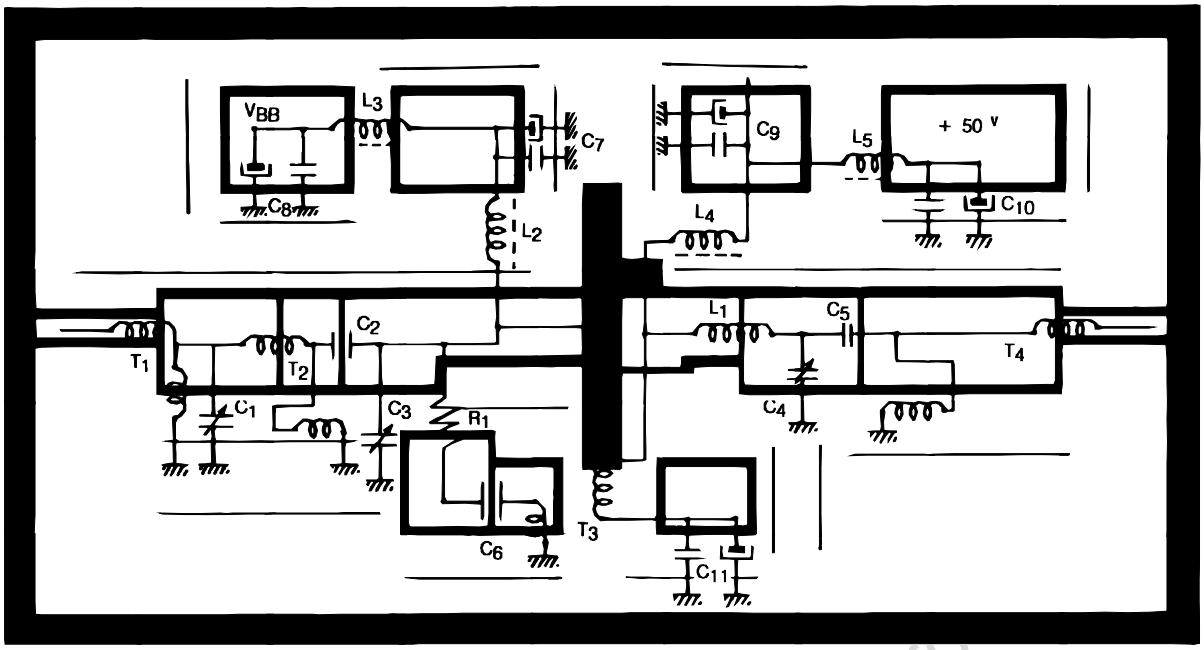
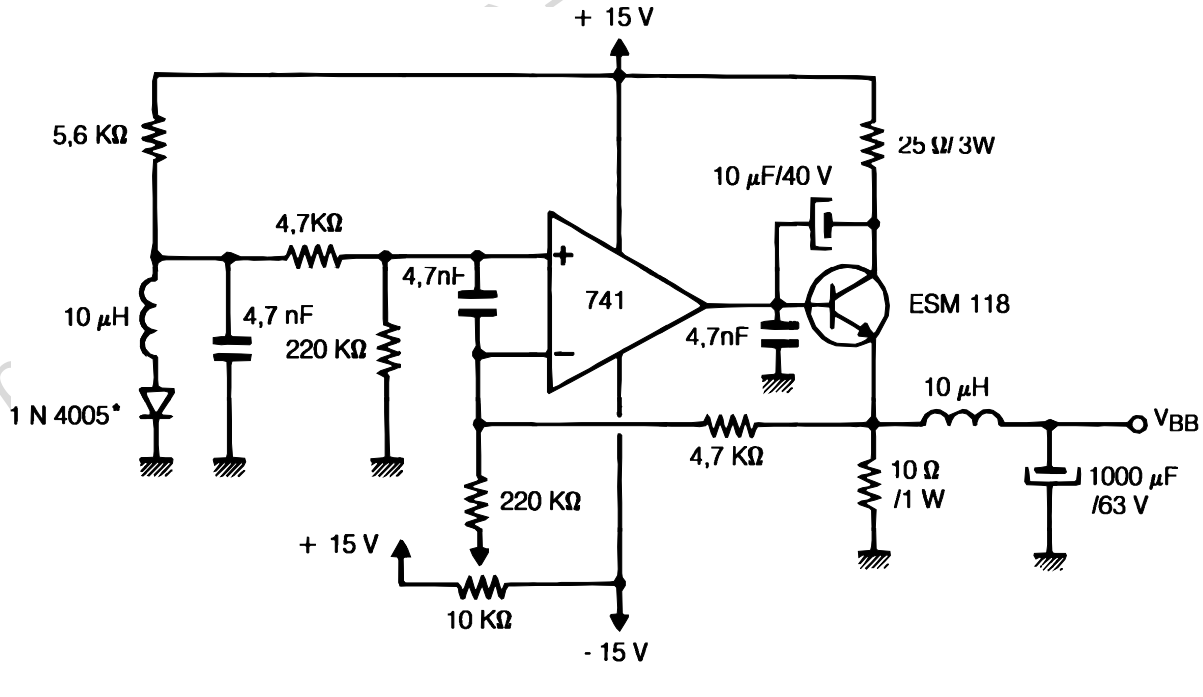
Figure 9. Mounting Circuit



BIAS CIRCUIT

Figure 10. Bias Circuit



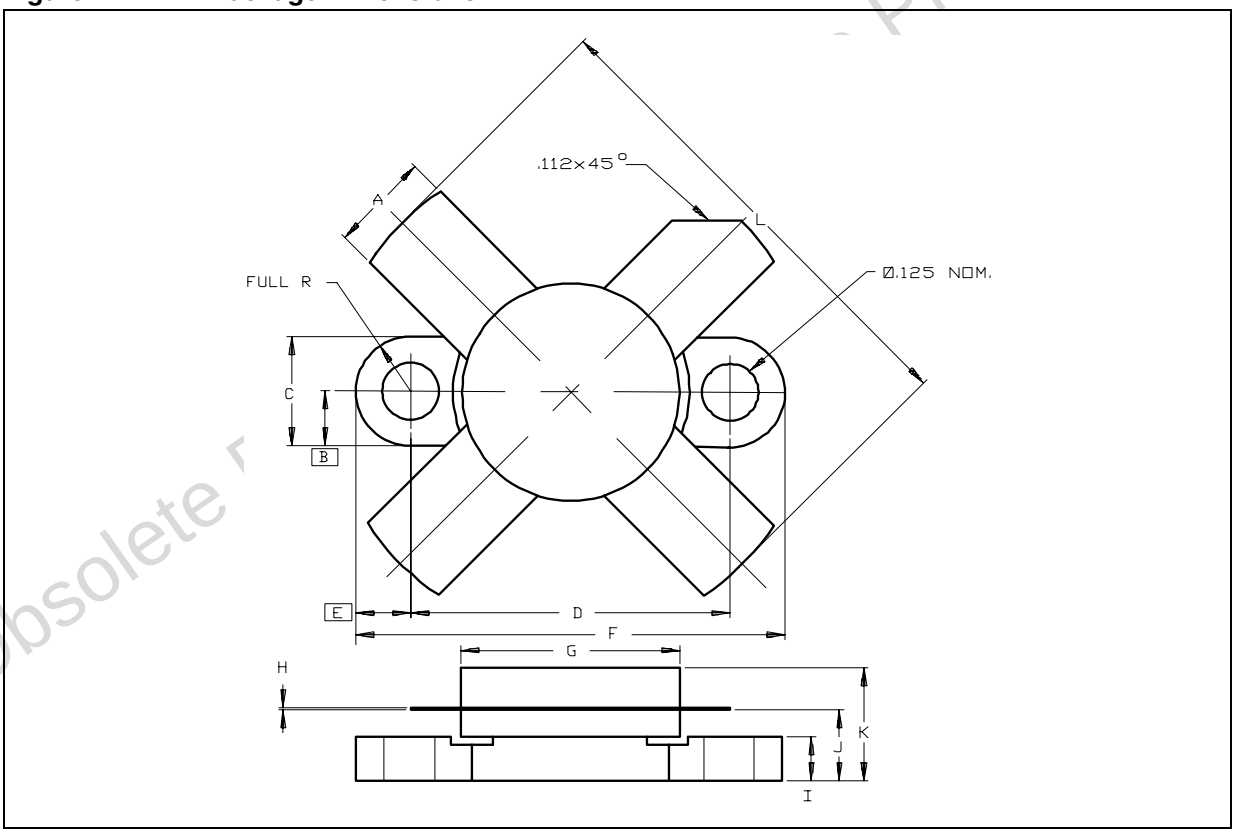
Obsolete Pro

PACKAGE MECHANICAL

Table 7. M174 Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	5.59		5.84	0.220		0.230
B		3.18			0.125	
C	6.22		6.48	0.245		0.255
D	18.28		18.54	0.720		0.730
E		3.18			0.125	
F	24.64		24.89	0.970		0.980
G	12.57		12.83	0.495		0.505
H	0.08		0.18	0.003		0.007
I	2.29		2.79	0.090		0.110
J	4.06		4.45	0.160		0.175
K			7.11			0.280
L			26.67			1.050

Figure 11. M174 Package Dimensions



Note: Drawing is not to scale.

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REVISION HISTORY

Table 8. Revision History

Date	Revision	Description of Changes
July-1995	1	First Issue
8-June-2004	2	Stylesheet update. No content change.

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