TPD1E10B06 采用 0402 封装的单通道 ESD 保护二极管

1 特性

- 可为低压 I/O 接口提供系统级静电放电 (ESD) 保护
- IEC 61000-4-2 4 级 ESD 保护
  - ±30kV 接触放电
  - ±30kV 气隙放电
- IEC 61000-4-5 浪涌：6A (8/20μs)
- I/O 电容 12pF（典型值）
- R_{DYN}：0.4Ω（典型值）
- 直流击穿电压：±6V（最小值）
- 超低泄漏电流：100nA（典型值）
- 钳位电压：10V（I_{PP} = 1A 时的最大值）
- 工业温度范围：–40°C 至 125°C
- 采用节省空间的 0402 封装
  (1mm × 0.6mm × 0.5mm)

2 应用

- 终端设备：
  - 平板电脑
  - 远程控制器
  - 可穿戴产品
  - 机顶盒
  - 电子销售点 (EPOS)
  - 电子书
- 接口：
  - 音频线路
  - 按钮
  - 通用输入/输出 (GPIO)

3 说明

TPD1E10B06 器件是一款采用小型 0402 封装的单通道 ESD 瞬态电压抑制 (TVS) 二极管。这款 TVS 保护产品提供 ±30kV 接触 ESD 和 ±30kV IEC 气隙保护，并具有一个带背靠背 TVS 二极管的 ESD 钳位电路，用于支持双极或双向信号。该 ESD 保护二极管的线路电容为 12pF，适用于支持数据传输速率 高达 400Mbps 应用。0402 封装符合行业标准，便于将元件安装到空间受限型 应用。

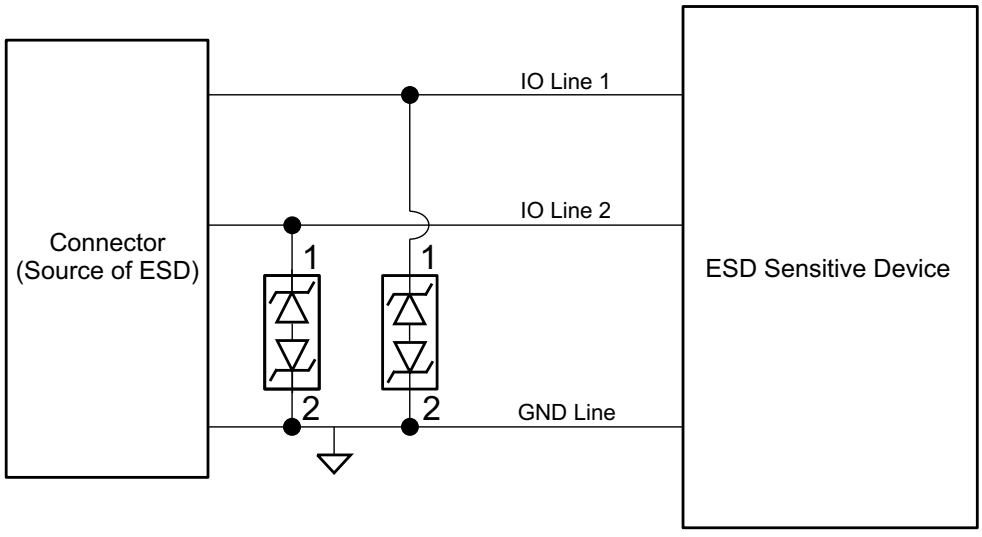
ESD 保护产品的 典型 应用是为音频线路（麦克风、耳机和扬声器）、SD 接口、键盘或其他按钮、USB 端口的 VBUS 引脚和 ID 引脚以及通用 I/O 端口等提供电路保护。该 ESD 钳位有利于为电子书、平板电脑、远程控制器、可穿戴设备、机顶盒以及电子销售点等终端设备提供保护。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD1E10B06	X1SON (2)	0.60mm x 1.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

应用电路原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (April 2015) to Revision D — **Page**

- Added Added test condition frequency to capacitance ... 4
- 已添加 *社区资源* ... 11

Changes from Revision B (October 2012) to Revision C — **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 说明* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision A (March 2012) to Revision B — **Page**

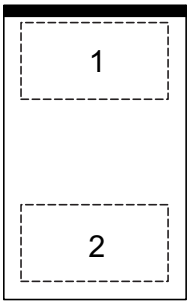
- Added THERMAL INFORMATION table. ... 4

Changes from Original (February 2011) to Revision A — **Page**

- 已更新 特性。 ... 1
- Added graphs to TYPICAL CHARACTERISTICS section. ... 5
- Added APPLICATION INFORMATION section. ... 8

5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN	I/O	DESCRIPTION
1	I/O	ESD Protected I/O
2		

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
	Operating temperature	–40	125	°C
I_{PP}	Peak pulse current (tp = 8/20 µs)		6	A
P_{PP}	Peak pulse power (tp = 8/20 µs)		90	W
T_{stg}	Storage temperature	–65	155	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		IEC 61000-4-2 Contact Discharge	30000	
		IEC 61000-4-2 Air-Gap Discharge	30000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating Free-Air Temperature, T_A		–40		125	°C
Operating Voltage	Pin 1 to 2 or Pin 2 to 1	–5.5		5.5	V

6.4 Thermal Information

THERMAL METRIC[1]		TPD1E10B06 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	615.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	404.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	493.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	127.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	493.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	162	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	Pin 1 to 2 or Pin 2 to 1			5.5	V
I_{LEAK}	Leakage current	Pin 1 = 5 V, Pin 2 = 0 V			100	nA
VClamp1,2	Clamp voltage with ESD strike on pin 1, pin 2 grounded.	I_{PP} = 1 A, tp = 8 to 20 µs[1]			10	V
		I_{PP} = 5 A, tp = 8 to 20 µs[1]			14	
VClamp2,1	Clamp voltage with ESD strike on pin 2, pin 1 grounded.	I_{PP} = 1 A, tp = 8 to 20 µs[1]			8.5	V
		I_{PP} = 5 A, tp = 8 to 20 µs[1]			14	
R_{DYN}	Dynamic resistance	Pin 1 to Pin 2[2]		0.32		Ω
		Pin 2 to Pin 1[2]		0.38		
C_{IO}	I/O capacitance	V_{IO} = 2.5 V; f = 1 MHz		12		pF
$V_{BR1,2}$	Break-down voltage, pin 1 to pin 2	I_{IO} = 1 mA	6			V
$V_{BR2,1}$	Break-down voltage, pin 2 to pin 1	I_{IO} = 1 mA	6			V

(1) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5
(2) Extraction of $R_{DYNAMIC}$ using least squares fit of TLP characteristics between I_{PP} = 10 A and I_{PP} = 20 A.

6.6 Typical Characteristics

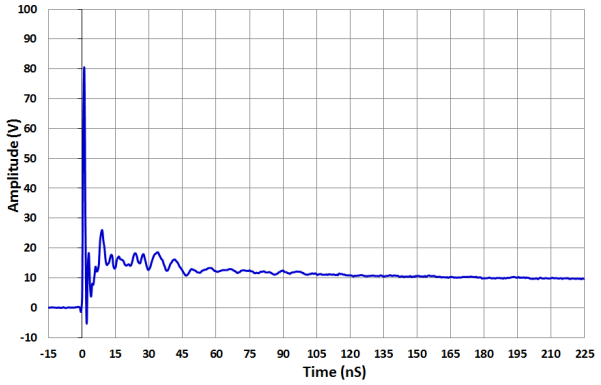


Figure 1. IEC 61000-4-2 Clamp Voltage +8-kV Contact ESD

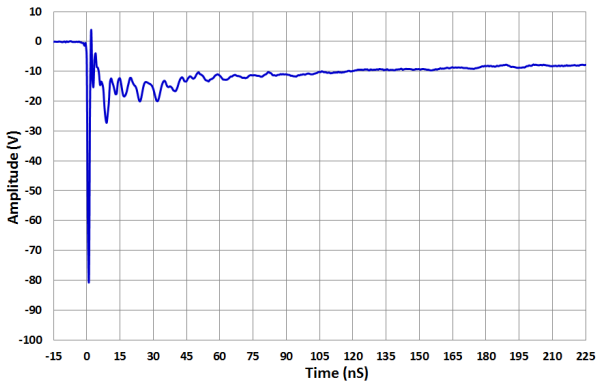


Figure 2. IEC 61000-4-2 Clamp Voltage –8-kV Contact ESD

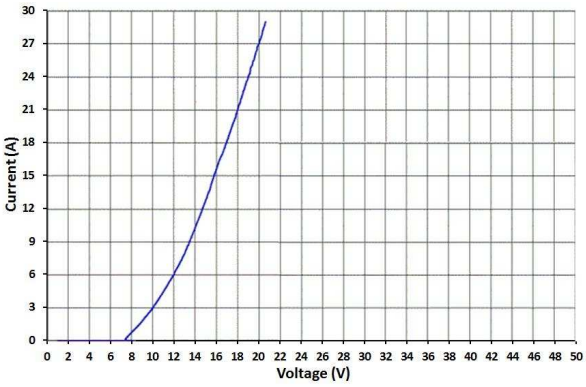


Figure 3. Transmission Line Pulse (TLP) Waveform Pin 1 to Pin 2

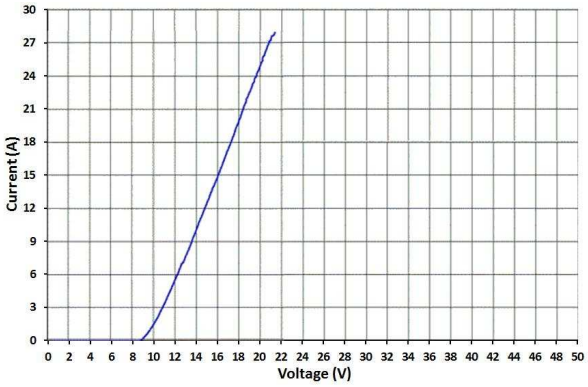


Figure 4. Transmission Line Pulse (TLP) Waveform Pin 2 to Pin 1

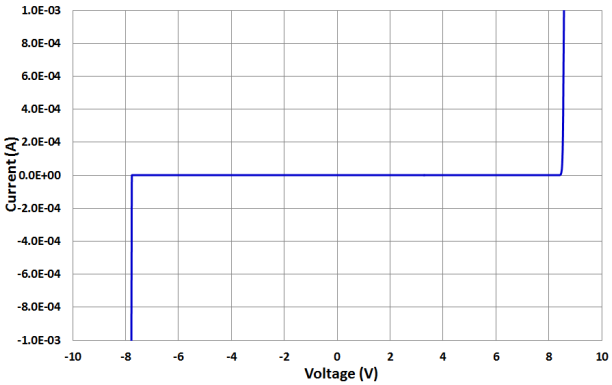


Figure 5. IV Curve

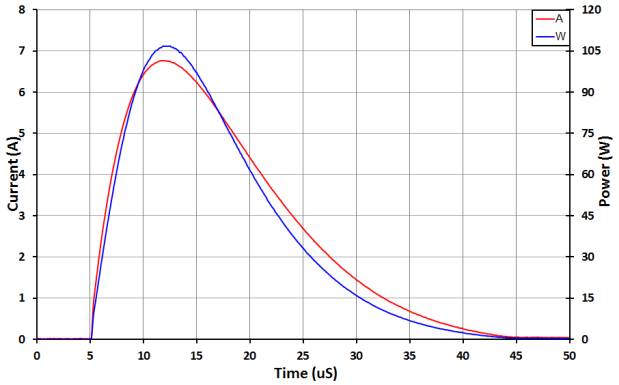


Figure 6. Positive Surge Waveform 8 to 20 µs

Typical Characteristics (continued)

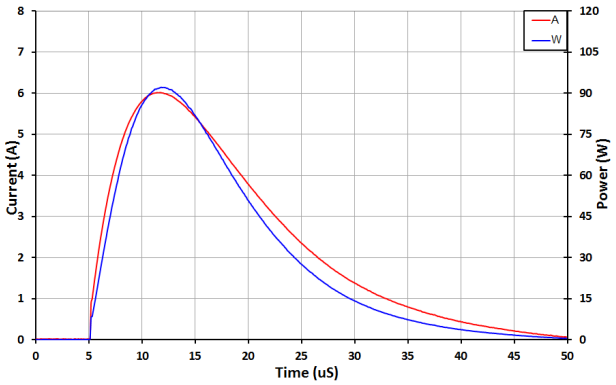


Figure 7. Negative Surge Waveform 8 to 20 µs

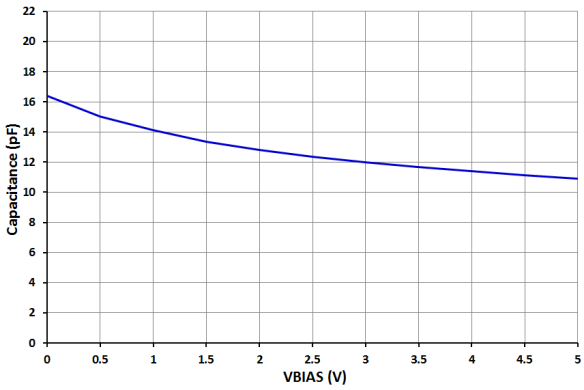


Figure 8. Pin Capacitance Across V_{BIAS}

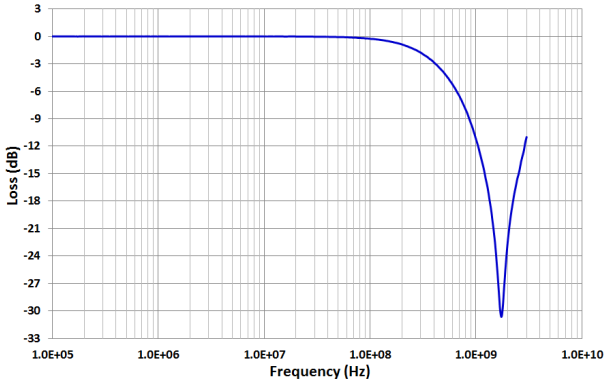


Figure 9. Insertion Loss

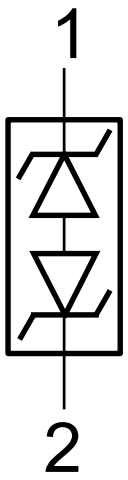
7 Detailed Description

7.1 Overview

The TPD1E10B06 is a single-channel ESD TVS diode in a small 0402 package. This TVS protection product offers ±30-kV IEC air-gap, ±30-kV contact ESD protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. The 12-pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps. The 0402 package is an industry standard and is convenient for component placement in space-saving applications.

Typical application of this ESD protection product is the circuit protection for audio lines (microphone, earphone, and speakerphone), SD interfacing, keypad or other buttons, VBUS pin and ID pin of USB ports, and general-purpose I/O ports. This ESD clamp is a good fit for the protection of the end equipment like ebooks, tablets, remote controllers, wearables, set-top boxes, and electronic point of sale equipment.

7.2 Functional Block Diagram



7.3 Feature Description

TPD1E10B06 is a bidirectional TVS with high ESD protection level. This device protects circuit from ESD strikes up to ±30-kV contact and ±30-kV air-gap specified in the IEC 61000-4-2 level 4 international standard. The device can also handle up to 6-A surge current (IEC61000-4-5 8/20µs). The I/O capacitance of 12 pF supports a data rate up to 400 Mbps. This clamping device has a small dynamic resistance of 0.4 Ω typically, which makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 10 V when the device is taking 1-A transient current. The breakdown is bidirectional so that this protection device is a good fit for GPIO and especially audio lines which carry bidirectional signals. Low leakage allows the diode to conserve power when working below the V_{RWM}. The industrial temperature range of –40°C to 125°C makes this ESD device work at extensive temperatures in most environments. The space-saving 0402 package can fit into small electronic devices like mobile equipment and wearables.

7.4 Device Functional Modes

TPD1E10B06 is a passive clamp that has low leakage during normal operation when the voltage between pin 1 and pin 2 is below V_{RWM} and activates when the voltage between pin 1 and pin 2 goes above V_{BR}. During IEC ESD events, transient voltages as high as ±30 kV can be clamped between the two pins. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When a system contains a human interface connector, the system becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. TPD1E10B06 is a single-channel ESD protection device containing back-to-back TVS diodes, which is typically used to provide a path to ground for dissipating ESD events on bidirectional signal lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

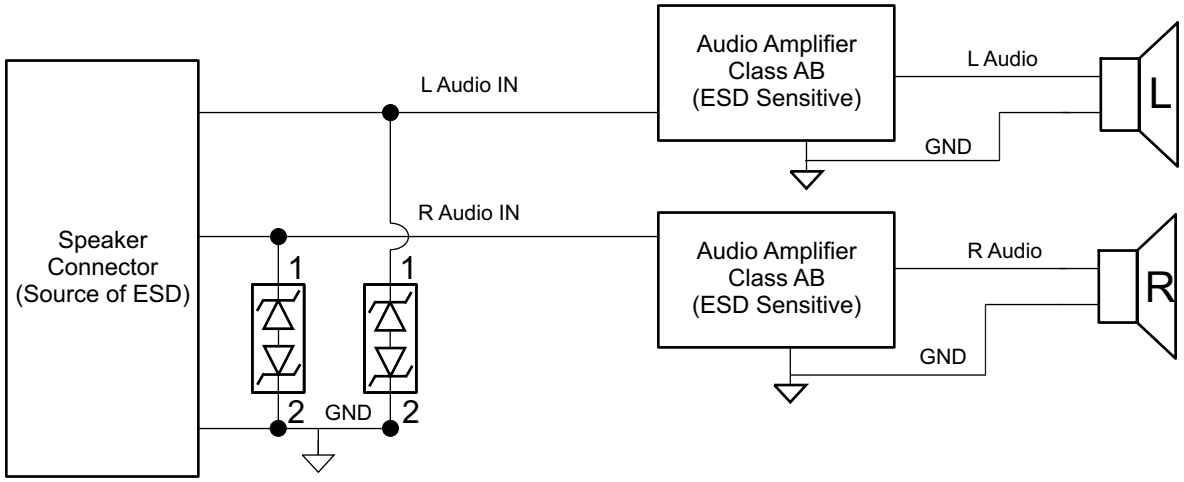


Figure 10. Typical Application Schematic

8.2.1 Design Requirements

For this design example, two TPD1E10B06s will be used to protect left and right audio channels. For this audio application, the following system parameters are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Audio Amplifier Class	AB
Audio signal voltage range	–3 V to 3 V
Audio frequency content	20 Hz to 20 kHz
Required IEC 61000-4-2 ESD Protection	±20-kV Contact/ ±25-kV Air-Gap

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer should make sure:

- Voltage range on the protected line must not exceed the reverse standoff voltage of the TVS diode(s) (V_{RWM})
- Operating frequency is supported by the I/O capacitance C_{IO} of the TVS diode
- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode

For this application, the audio signal voltage range is –3 V to 3 V. The V_{RWM} for the TVS is –5.5 V to 5.5 V; therefore, the bidirectional TVS will not break down during normal operation, and therefore normal operation of the audio signal will not be effected due to the signal voltage range. In this application, a bidirectional TVS like TPD1E10B06 is required.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from 20 Hz to 20 kHz; ensure that the TVS I/O capacitance will not distort this signal by filtering it. With TPD1E10B06 typical capacitance of 12 pF, which leads to a typical 3-dB bandwidth of 400 MHz, this diode has sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires above standard Level 4 IEC 61000-4-2 system-level ESD protection (±20-kV Contact/ ±25-kV Air-Gap). A standard TVS cannot survive this level of IEC ESD stress. However, TPD1E10B06 can survive at least ±30-kV Contact/ ±30-kV Air-Gap. Therefore, the device can provide sufficient ESD protection for the interface, even though the requirements are stringent. For any TVS diode to provide the full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, a system designer must use proper board layout of their TVS ESD protection diodes. See *Layout* for instructions on properly laying out TPD1E10B06.

8.2.3 Application Curves

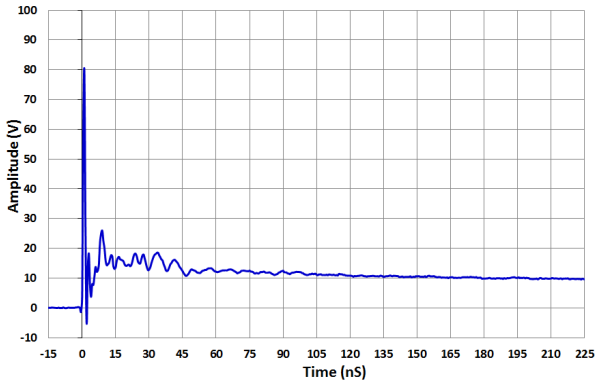


Figure 11. IEC 61000-4-2 Clamp Voltage +8-kV Contact ESD

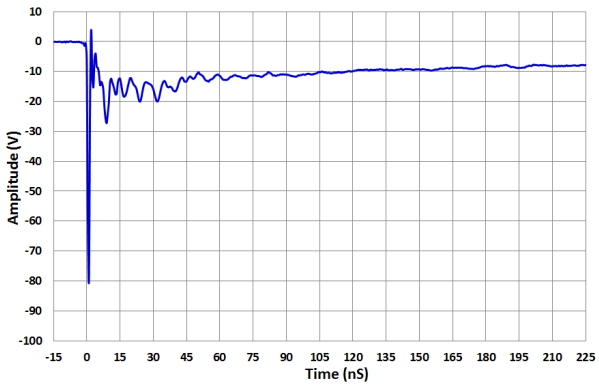


Figure 12. IEC 61000-4-2 Clamp Voltage –8-kV Contact ESD

9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, therefore there is no requirement to power it. Take care to make sure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path

10.2 Layout Example

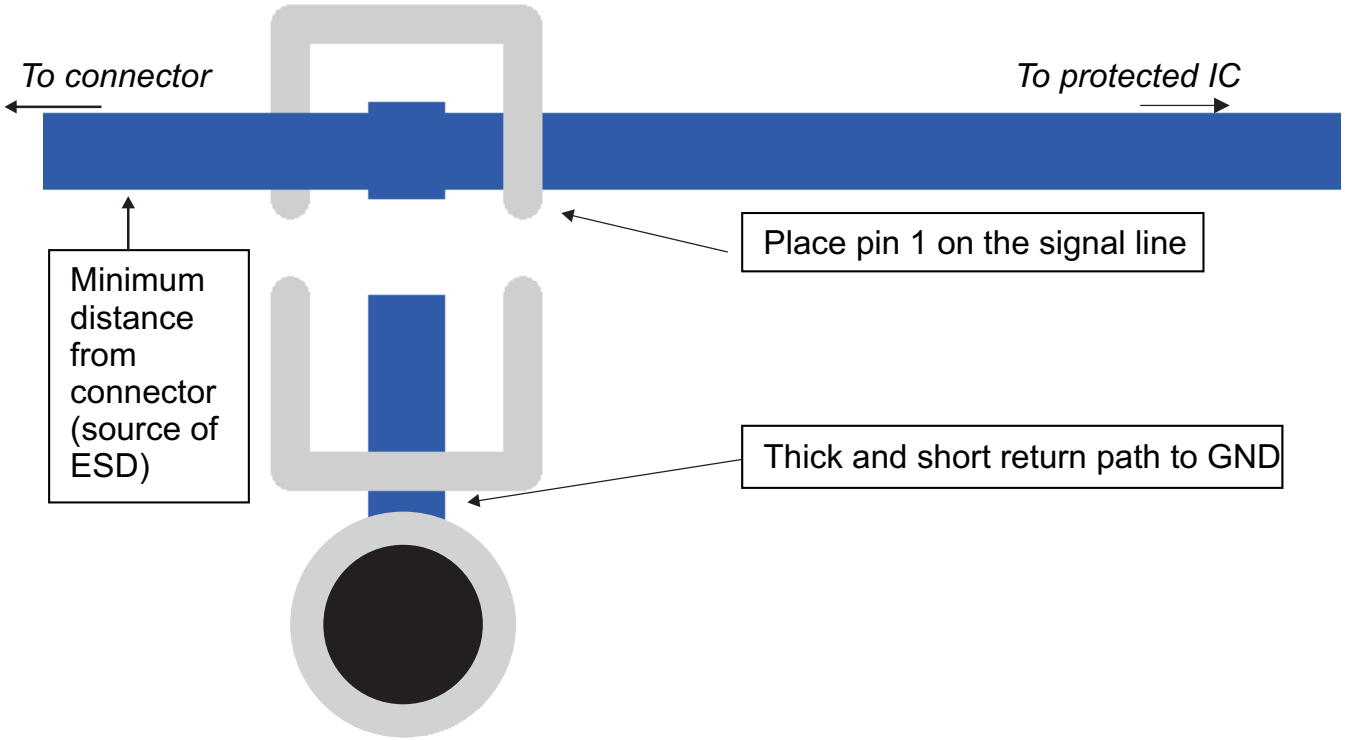


Figure 13. Layout Recommendation

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E10B06DPYR	ACTIVE	X1SON	DPY	2	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(B1 ~ B2 ~ B6)	Samples
TPD1E10B06DPYT	ACTIVE	X1SON	DPY	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(B1 ~ B2 ~ B6)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

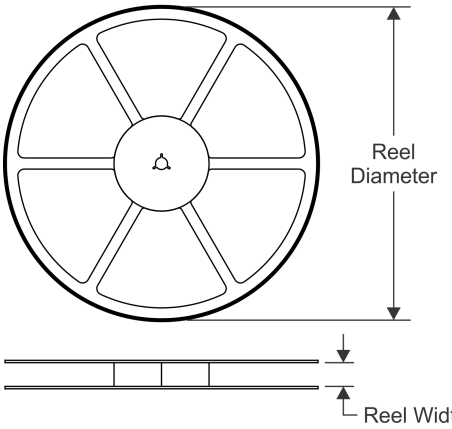
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

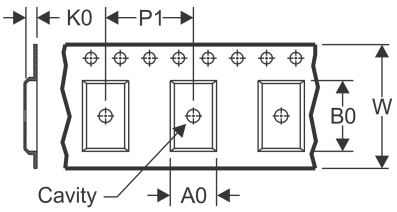
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

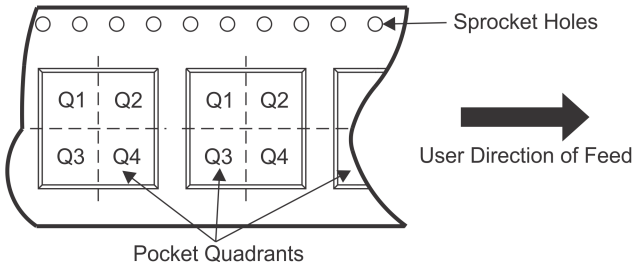


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

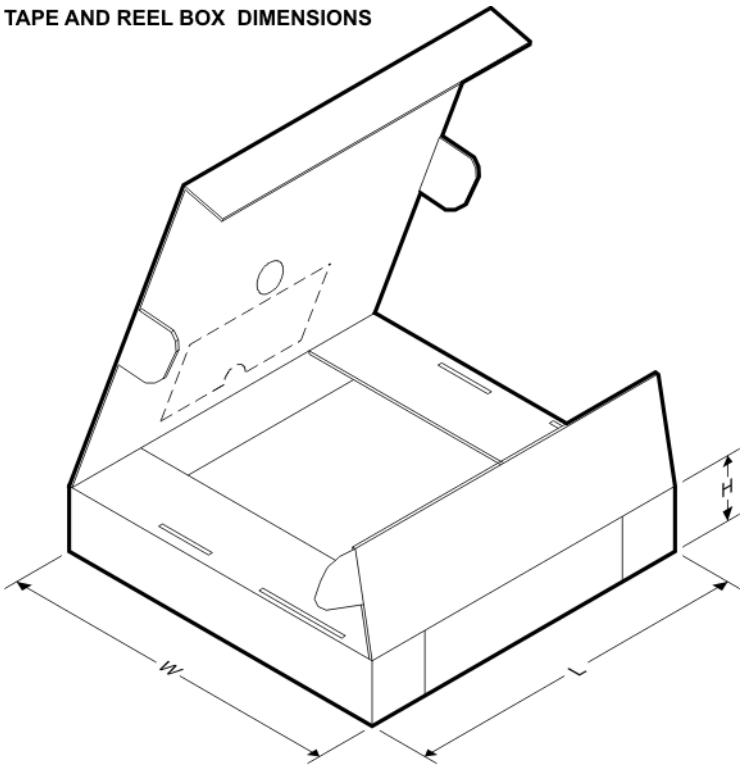
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E10B06DPYR	X1SON	DPY	2	10000	180.0	9.5	0.72	1.12	0.43	2.0	8.0	Q1
TPD1E10B06DPYR	X1SON	DPY	2	10000	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B06DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TPD1E10B06DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B06DPYT	X1SON	DPY	2	250	180.0	9.5	0.72	1.12	0.43	2.0	8.0	Q1
TPD1E10B06DPYT	X1SON	DPY	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

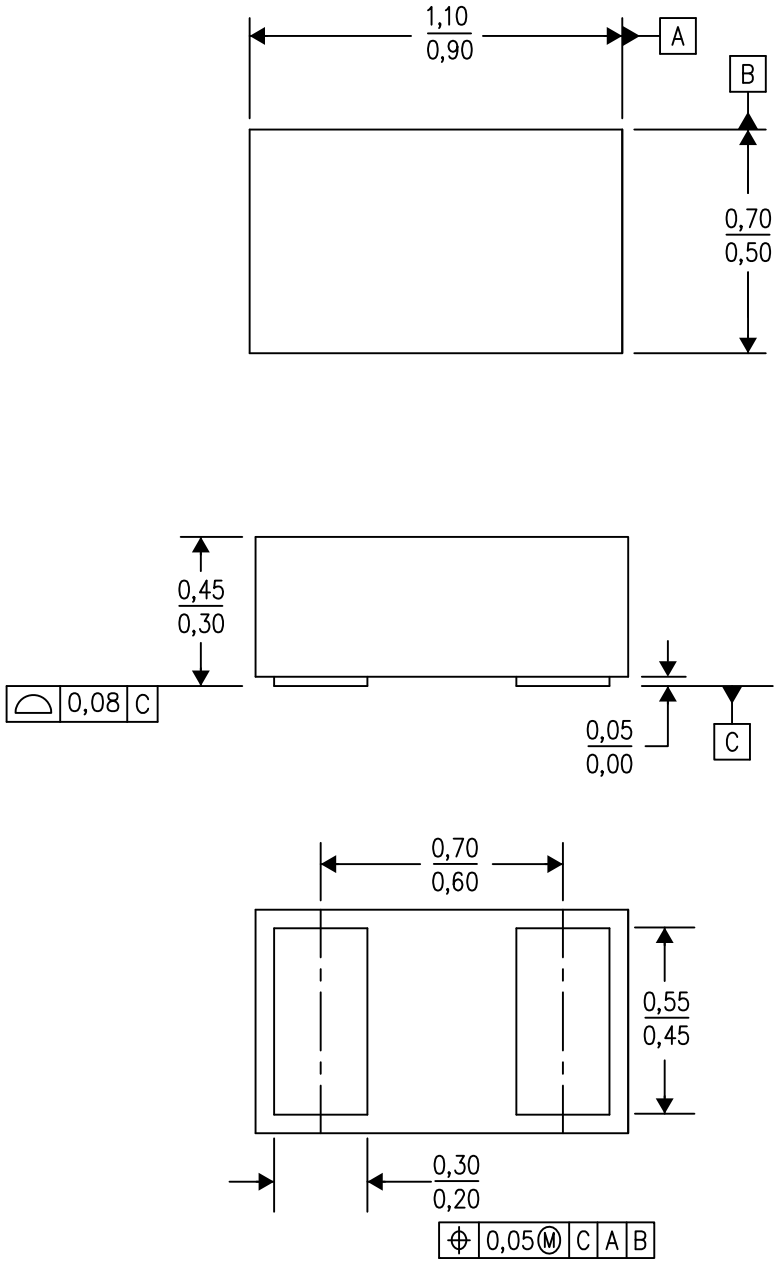
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E10B06DPYR	X1SON	DPY	2	10000	189.0	185.0	36.0
TPD1E10B06DPYR	X1SON	DPY	2	10000	184.0	184.0	19.0
TPD1E10B06DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0
TPD1E10B06DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD1E10B06DPYT	X1SON	DPY	2	250	189.0	185.0	36.0
TPD1E10B06DPYT	X1SON	DPY	2	250	205.0	200.0	33.0

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

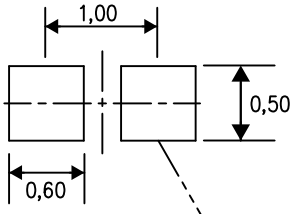


4211012/D 08/14

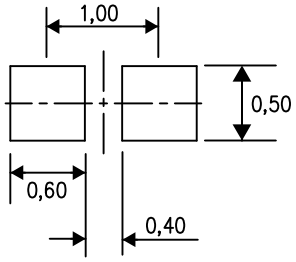
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

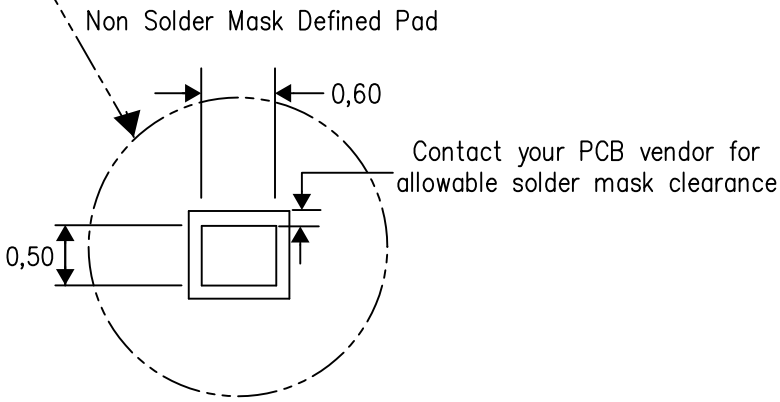
DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)





4215270/B 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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