3W STEREO CLASS-D Audio Amplifier and Class AB Headphone Driver (DC VOLUME, UVP and AGC Function)

Description

The PAM8009 is a 3W, Class D audio-power amplifier for driving bridged-tied stereo speakers. Advanced DC volume control minimizes external components and allows BTL (Speaker) volume control and SE (Headphone) volume control, the gain range is from +20dB (Volume=5V) to -60dB (Volume=0V) with 64 steps precise control.

Integrated power-limit technology suppresses the output signal clip automatically due to the over level input signal. This technology also offers low THD+N and protects speaker.

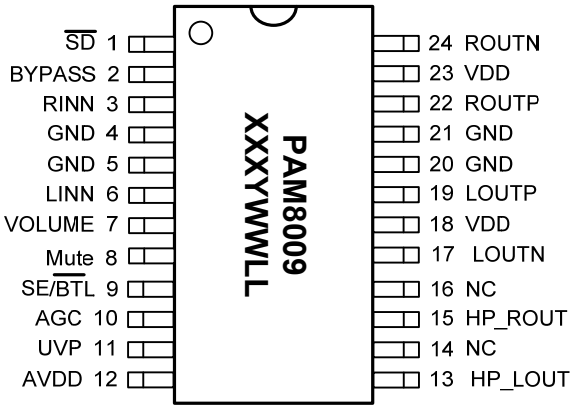
Integrated Undervoltage Protection (UVP) technology, external undervoltage detection can be used to shut down the PAM8009 before an input device can generate a pop.

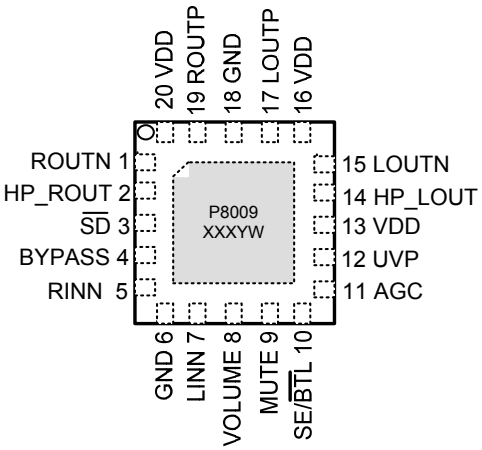
PAM8009 is available in SO-24 and U-QFN4040-20.

Features

- Operating Voltage: 2.8v ~ 5.5v
- Filter – Free and Low EMI
- Low Quiescent Current
- IDD=7mA @ VDD= 5V
- 64 Steps DC Volume Control from -80dB to +20dB by DC Voltage with Hysteresis
- Power Limit Function
  - Disable: 0.45VDD ~ VDD
  - Max. Power: GND
- UVP Function
  - Disable: Floating
- Output Power @ THD+N=1%
  - BTL Mode
    - VDD=5V, Rl=4Ω; Po=2.4W
    - VDD=5V, Rl=8Ω; Po=1.4W
  - SE Mode
    - VDD=5V, Rl=32Ω; Po=60mW
- Output Power @ THD+N = 10%
  - BTL Mode
    - VDD=5V, Rl=4Ω; Po=3.0W
    - VDD=5V, Rl=8Ω; Po=1.7W
- Input Signal and Headphone Output Signal in Phase
- Thermal and Over-Current Protections with Auto-Recovery
- Power Enhance Package SO-24 and U-QFN4040-20
- Lead Free and Green Devices Available (RoHS Compliant)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green Device (Note 3)**

Pin Assignments





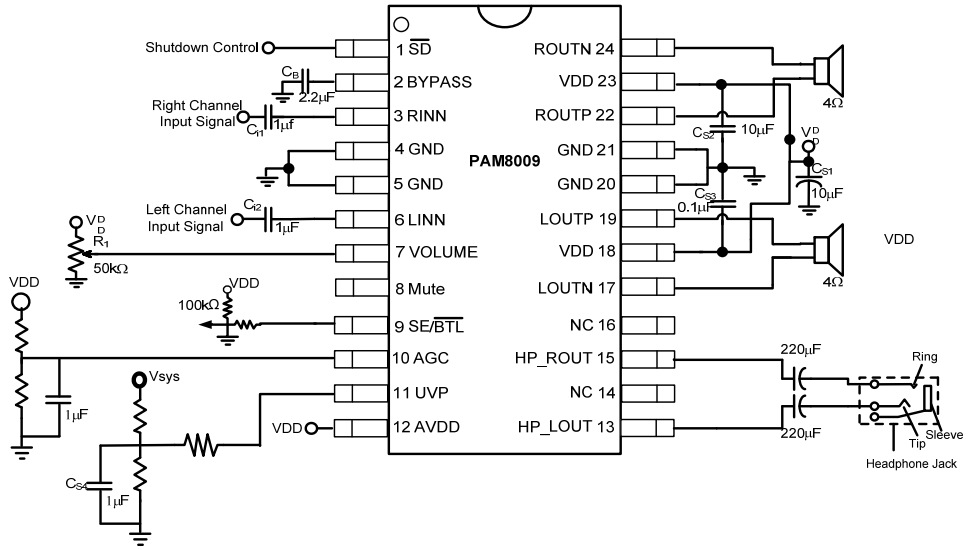
Applications

- LCD Monitor / Projects
- Projects / All-In-One Computers
- Portable Speakers
- Portable DVD Player / Game Machines

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Applications Circuit

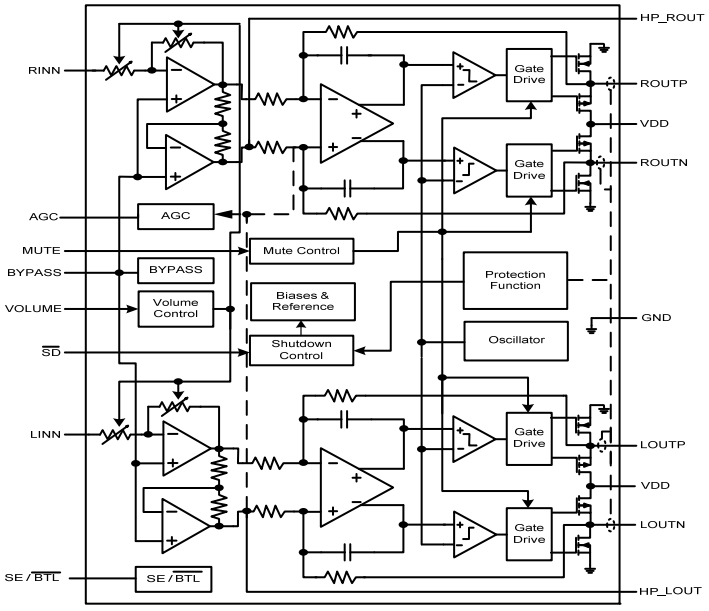


Pin Descriptions

Package Name			Function
SO-24	QFN-20	Name	
1	3	/SD	Full Chip Shutdown Control Input (Active Low)
2	4	Bypass	Bias Voltage for Power Amplifier
3	5	RIN	Negative Input of Right Channel Power Amplifier
4, 5, 20, 21	6, 18	GND	Ground Connection
6	7	LIN	Negative Input of Left Channel Power Amplifier
7	8	VOLUME	Internal Gain Setting Input Connect to VDD which Set Max. Gain = +20dB
8	9	MUTE	Mute Control Signal Input (Active High)
9	10	SE/ BTL	Output Mode Control Input High for SE Mode and Low for BTL Mode
10	11	AGC	VDD ~ 0.45 x VDD or Floating, Disable the Function
11	12	UVP	Under Voltage Protection Input Floating or Pull High Disable the Function
12, 18, 23	13,16,20	VDD	Power
13	14	HP_LOUT	Headphone Output of Left Channel Power Amplifier
14, 16	-	N.C	No Connection
15	2	HP_ROUT	Headphone Output of Right Channel Power Amplifier
17	15	LOUTN	Negative Output of Left Channel Power Amplifier
19	17	LOUTP	Positive Output of Left Channel Power Amplifier
22	19	ROUTP	Positive Output of Right Channel Power Amplifier
24	1	ROUTN	Negative Output of Left Channel Power Amplifier

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Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 6.0	V
V_{DD}	Input Voltage	-0.3 to V_{DD} + 0.3	
T_J	Maximum Junction Temperature	+150	°C
T_{STG}	Storage Temperature Range	- 65 to +150	
T_{SDR}	Maximum Soldering Temperature Range, 5 Seconds	+300	

Notes: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Max	Unit
V_{DD}	Supply Voltage Range		2.8 ~ 5.5	V
V_{IH}	High Level Threshold Voltage	SD, MUTE	2 ~ V_{DD}	V
		SE, BTL	0.8 x V_{DD} ~ V_{DD}	V
V_{IL}	Low Level Threshold Voltage	SD, MUTE	0 ~ 0.8	V
		SE, BTL	0 ~ 1.0	V
V_{ICM}	Common Mode Input Voltage		1 ~ V_{DD} - 1	V
T_A	Ambient Operation Temperature Range		-40 ~ + 85	°C
T_J	Junction Temperature Range		-40 + 125	

Thermal Information (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Thermal Resistance – Junction to Ambient	SO-24 QFN4040-20	+96 +45	°C/W
θ_{JC}	Ambient Operation Temperature Range	SO-24 QFN4040-20	+18 +7	°C/W

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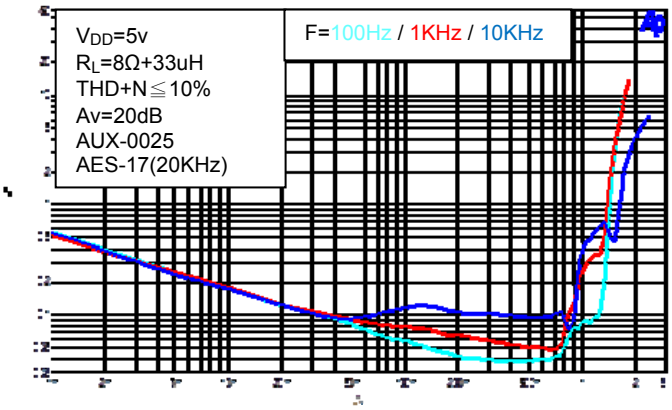
Electrical Characteristics (@T_A = +25°C, V_{DD} = 5V, Gain = Max., R_L=8Ω, unless otherwise specified.)

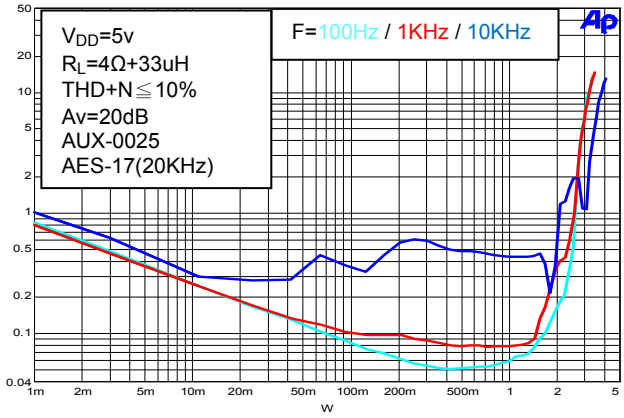
Symbol	Parameter	Conditions	Min	Typ	Max	Units
BTL Mode						
VDD	Supply Voltage Range	-	2.8	-	5.5	V
I_Q	Quiescent Current (BTL)	V_{MUTE}=0, V_{SD}=5V, No Load	-	7	-	mA
I_Q	Quiescent Current (SE)	V_{MUTE}=0, V_{SD}=5V, No Load	-	4	-	mA
I_{MUTE}	Mute Current (BTL)	V_{MUTE}=0, V_{SD}=5V, No Load	-	3	-	mA
I_{MUTE}	Mute Current (SE)	V_{MUTE}=0, V_{SD}=5V, No Load	-	4	-	mA
I_{SD}	Shutdown Current	V_{MUTE}=0, V_{SD}=0V, No Load	-	-	1	μA
F_{OSC}	Oscillator Frequency	-	200	250	300	KHz
Ri	Input Resistance (BTL)	Gain=20dB	-	-	33	KΩ
Ri	Input Resistance (SE)	Gain=3.5dB	-	-	56	KΩ
V_{OS}	Output Offset Voltage	No load	-	10	-	mV
$R_{DS(on)}$	Drain – Source on-State Resistance	VDD=5.5V, Ids=0.8A P MOSFET	-	0.26	-	Ω
		VDD=5.5V, Ids=0.8A N MOSFET	-	0.19	-	
		VDD=4.5V, Ids=0.6A P MOSFET	-	0.28	-	
		VDD=4.5V, Ids=0.6A N MOSFET	-	0.21	-	
		VDD=3.6V, Ids=0.4A P MOSFET	-	0.29	-	
		VDD=3.6V, Ids=0.4A N MOSFET	-	0.21	-	
$T_{START\ UP}$	Startup time from Shutdown	Bypass Capacitor, Cb=2.2uF	-	1.72	-	S
Po	Output Power	THD+N=10%, f=1KHz, Rl=8Ω	1.5	1.7	-	W
		THD+N=10%, f=1KHz, Rl=4Ω	2.8	3.0	-	
THD+N	Total Harmonic Distortion Plus Noise	Rl=8Ω, Po=0.8W, f=1KHz	-	0.08	-	%
		Rl=4Ω, Po=1.6W, f=1KHz	-	0.08	-	
PSRR	Power Supply Ripple Rejection	Input AC-GND, f=1KHz, V_{pp}=200mV	-	- 61	-	dB
CS	Channel Separation	Po=1W, f=1KHz	-	-82	-	dB
η	Efficiency	Po=1.7W, f=1KHz, Rl=8Ω	85	90	-	%
		Po=3W, f=1KHz, Rl=4Ω	80	88	-	
V_N	Noise	Input AC-GND, A-weighting	-	180	-	uV
		Non A-weighting	-	270	-	uV
SNR	Signal Noise Ratio	F=20 ~ 20KHz, THD=1%	-	83	-	dB
SE Mode						
Vos	Output Offset Voltage	No load	-	2.5	-	V
Po	Output Power	THD+N=1%, Rl=32Ω, f=1KHz	-	60	-	mW
THD+N	Total Harmonic Distortion Plus Noise	Rl=32Ω, Po=50mW, f=1KHz	-	0.02	-	%
PSRR	Power Supply Ripple Rejection	Input AC-GND,F=1KHz,Vpp=200mV	-	75	-	dB
CS	Channel Separation	Po=1W, f=1KHz	-	-87	-	dB
Vn	Noise	Input AC-GND, A-weighting	-	74	-	uV
		Non A-weighting	-	58	-	uV
SNR	Signal Noise Ratio	F=20 ~ 20KHz, THD=1%	-	89	-	dB
Control Section						
V_{IH}	/SD Input High	-	1.4	-	-	V
V_{IL}	/SD Input Low	-	-	-	0.6	V
V_{MH}	Mute Input High	-	1.4	-	-	V
V_{ML}	Mute Input Low	-	-	-	0.6	V
OTP	Over Temperature Protection	-	-	150	-	°C
OTH	Over Temperature Hysteresis	-	-	108	-	°C

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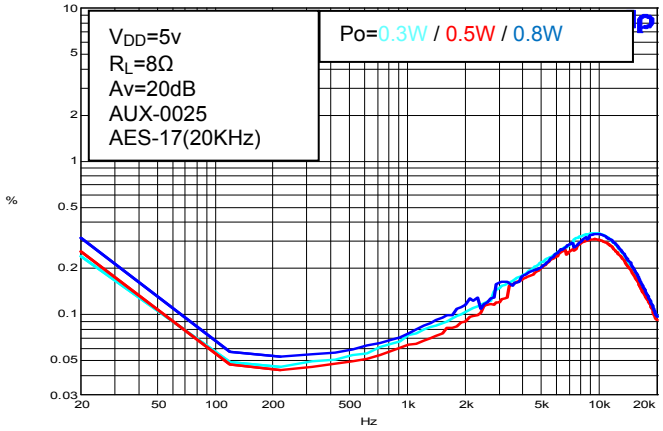
Typical Performance Characteristics

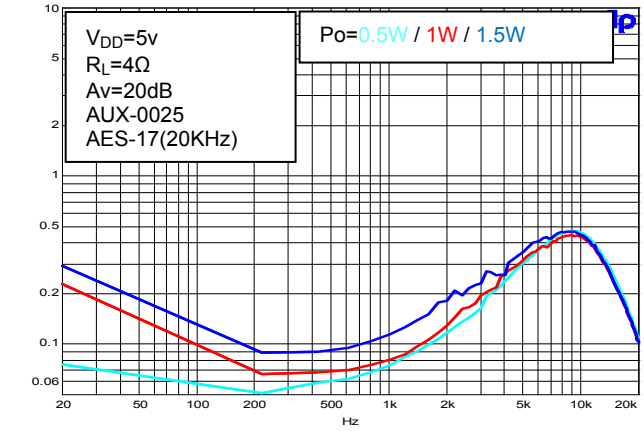
THD+N vs. Output Power



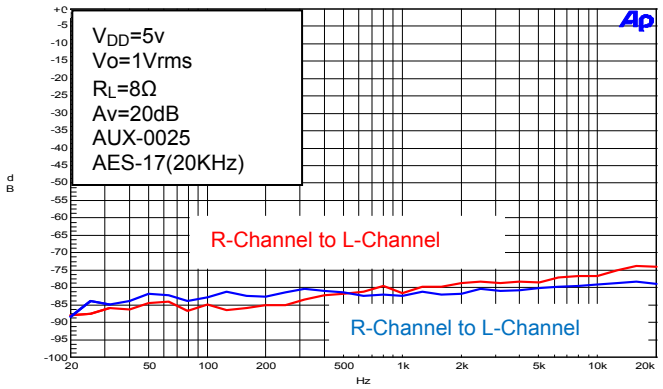


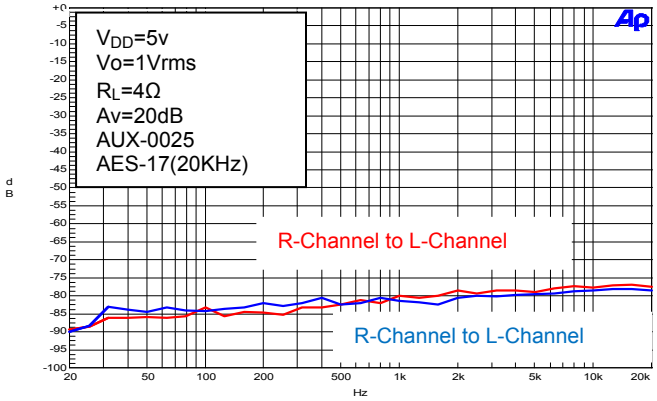
THD+N vs. Frequency





Crosstalk vs. Frequency

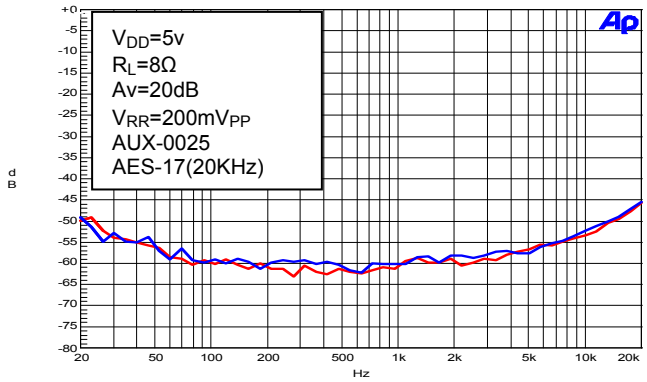


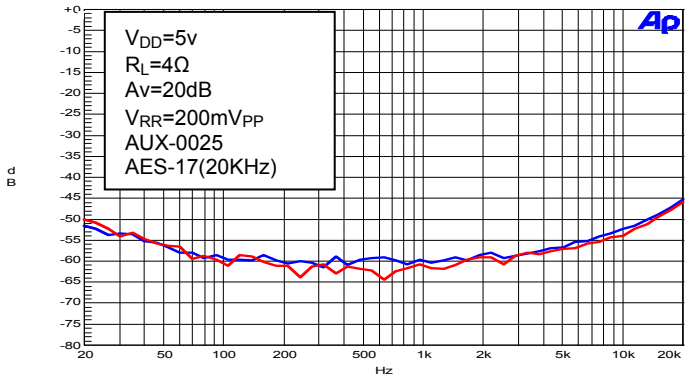


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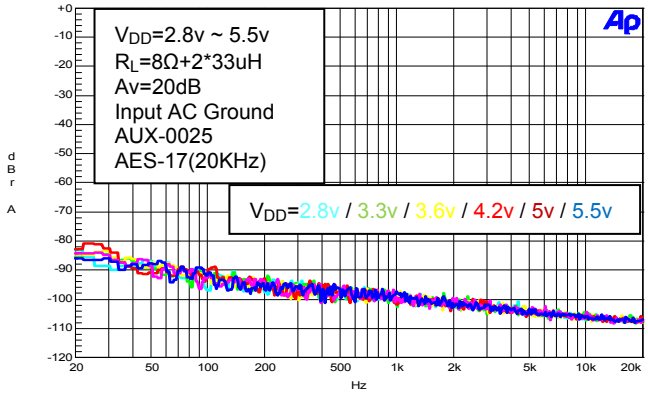
Typical Performance Characteristics (Cont.)

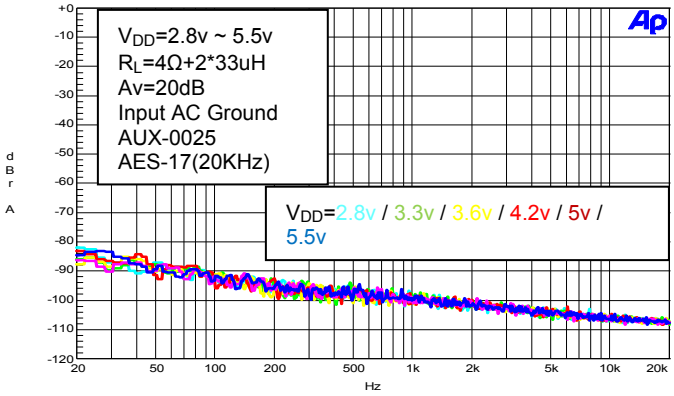
PSRR vs. Frequency





Output Noise vs. Frequency





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Typical Performance Characteristics (Cont.)

Table 1 DC Volume Control

STEP	BTL Gain(dB)	SE Gain(dB)	DC Volume (v)		STEP	BTL Gain(dB)	SE Gain(dB)	DC Volume (v)
1	20	3.51	4.708 ~ Max.		33	6.70	-7.11	2.389 ~ 2.461
2	19.6	3.22	4.637 ~ 4.708		34	6.40	-7.43	2.315 ~ 2.389
3	19.2	2.94	4.565 ~ 4.637		35	6.00	-7.76	2.243 ~ 2.315
4	18.8	2.66	4.493 ~ 4.565		36	5.70	-8.09	2.169 ~ 2.243
5	18.4	2.39	4.421 ~ 4.493		37	5.30	-8.42	2.097 ~ 2.169
6	18.0	2.12	4.347 ~ 4.421		38	4.90	-8.76	2.025 ~ 2.097
7	17.6	1.85	4.273 ~ 4.347		39	4.60	-9.09	1.951 ~ 2.025
8	17.1	1.46	4.195 ~ 4.273		40	4.20	-9.43	1.879 ~ 1.951
9	16.6	1.07	4.116 ~ 4.195		41	3.80	-9.77	1.807 ~ 1.879
10	16.1	0.69	4.045 ~ 4.116		42	3.50	-10.10	1.733 ~ 1.807
11	15.6	0.32	3.979 ~ 4.045		43	3.10	-10.46	1.661 ~ 1.733
12	15.1	-0.05	3.909 ~ 3.979		44	2.70	-10.81	1.589 ~ 1.661
13	14.6	-0.41	3.839 ~ 3.909		45	2.30	-11.16	1.517 ~ 1.589
14	14.2	-0.77	3.767 ~ 3.839		46	2.00	-11.52	1.443 ~ 1.517
15	13.7	-1.12	3.695 ~ 3.767		47	1.60	-11.88	1.371 ~ 1.443
16	13.3	-1.47	3.621 ~ 3.695		48	1.20	-12.24	1.297 ~ 1.371
17	12.9	-1.82	3.551 ~ 3.621		49	0.80	-12.62	1.225 ~ 1.297
18	12.5	-2.16	3.476 ~ 3.551		50	0.40	-12.99	1.153 ~ 1.225
19	12.0	-2.50	3.403 ~ 3.476		51	0.00	-13.38	1.079 ~ 1.153
20	11.6	-2.84	3.332 ~ 3.403		52	-1.00	-14.37	1.005 ~ 1.079
21	11.2	-3.18	3.259 ~ 3.332		53	-2.10	-15.42	0.929 ~ 1.005
22	10.8	-3.51	3.186 ~ 3.259		54	-3.00	-16.30	0.849 ~ 0.929
23	10.5	-3.84	3.114 ~ 3.186		55	-5.00	-18.23	0.771 ~ 0.849
24	10.1	-4.17	3.043 ~ 3.114		56	-7.00	-20.16	0.701 ~ 0.771
25	9.7	-4.50	2.969 ~ 3.043		57	-9.00	-22.08	0.633 ~ 0.701
26	9.3	-4.82	2.897 ~ 2.969		58	-10.9	-23.96	0.563 ~ 0.633
27	8.9	-5.16	2.823 ~ 2.897		59	-17.0	-30.01	0.491 ~ 0.563
28	8.6	-5.48	2.751 ~ 2.823		60	-22.8	-35.83	0.419 ~ 0.491
29	8.2	-5.80	2.678 ~ 2.751		61	-29.0	-41.98	0.347 ~ 0.419
30	7.8	-6.13	2.605 ~ 2.678		62	-33.5	-46.46	0.275 ~ 0.347
31	7.5	-6.45	2.533 ~ 2.605		63	-39.5	-52.58	0.201 ~ 0.275
32	7.1	-6.78	2.461 ~ 2.533		64	-60.0	-92.95	0 ~ 0.201

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Application Information

AGC Function

When output reaches the maximum power-setting value, the Internal Programmable Gain Amplifier will decrease the gain to prevent the output waveform from clipping. This feature prevents speaker damage from occurring using the AGC pin to set the AGC function, limiting the output power.

Table 1: AGC Setting Threshold vs. Output

AGC Function	Output Power
VDD ~ 0.45VDD or AGC Floating	AGC function Disable
0.45VDD ~ 0.27VDD	Po=[[8(1/2VDD-VAGC)^2]/Rl] x 0.95
0.27VDD ~ GND	Po=2.3W (Max. output power 4Ω) Po=1.2W (Max. output power 8Ω)

Mute Operation

The MUTE pin is an input for controlling the Class-D output state of the PAM8009. A logic low on this pin enables the outputs, and a logic high on this pin disables the outputs. This pin may be used to quickly disable or enable the outputs without a volume fade. Quiescent current is listed in the electrical characteristics table. The MUTE pin can be left floating due to the internal pull-down.

Shutdown Operation

In order to reduce power consumption while not in use, the PAM8009 contains shutdown circuit to turn off the amplifier's bias circuit. The amplifier is turned off when logic low is placed on the /SD pin. When switching the /SD pin to low level, the amplifier enters a low-consumption current status. The /SD pin can be left floating due to the internal pull-up.

Undervoltage Protection

External undervoltage detection can be used to shut down the PAM8009 before an input device can generate a pop. The shutdown threshold at the UVP pin is 1.2V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application.

The threshold can be determined as below:

With the condition: R3 >> R1//R2

V_{UVP} = [1.2-(6uA x R3)] x (R1+R2)/ R2

Hysteresis = 5uA x R3 x (R1+R2)/ R2

Power Supply Decoupling

The PAM8009 is a high performance CMOS audio-amplifier that requires adequate power supply decoupling to ensure the outputs of THD and PSRR are as low as possible. Power supply decoupling also prevents oscillation caused by long lead between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good Low-Equivalent-Series-Resistance (ESR) ceramic-capacitor, typically 0.1uF is recommend, placing it as close as possible to the device's V_{DD} lead. For filtering lower-frequency noise signals, a large capacitor of 10uF or greater placed near the audio amplifier is recommended.

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Application Information (Cont.)

Input Capacitor (Ci)

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequency without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large-input-capacitor may not increase actual system performance. In this case, Input Capacitor (Ci) and Input Resistance (Ri) of the amplifier form a high-pass filter with the corner frequency determined equation below:

$$Fc = 1/ 2\pi Ri \times Ci$$

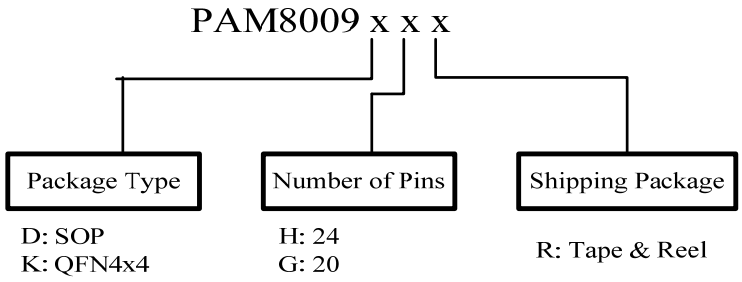
In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, Ci. A larger in/out coupling capacitor requires more charge to reach its quiescent DC voltage (Normally 1/2 V_{DD}). This charge comes from the internal circuit via the feedback and is apt to create pops upon device enabling. Thus, by minimizing the capacitor size based on necessary low frequency response, turn on pop can be minimized.

Bypass Capacitor (C_{BYP})

Bypass Capacitor (C_{BYP}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output signal. The noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N.

A ceramic bypass capacitor (C_{BYP}) of 0.47uF to 1.0uF is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown.

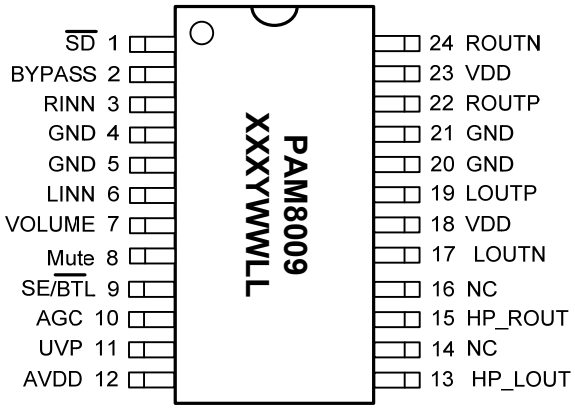
Ordering Information



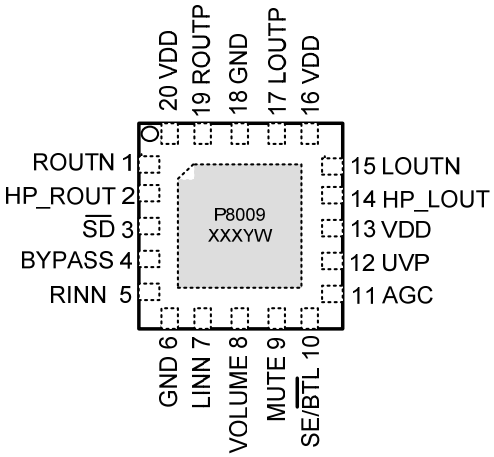
Part Number	Package Type	Standard Package
PAM8009DHR	SOP-24	1000 Unit/Tape&Reel
PAM8009KGR	U-QFN4040	3000 Unit/Tape&Reel

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Marking Information



X: Internal Code
Y: Year
WW: Week
LL: Internal Code



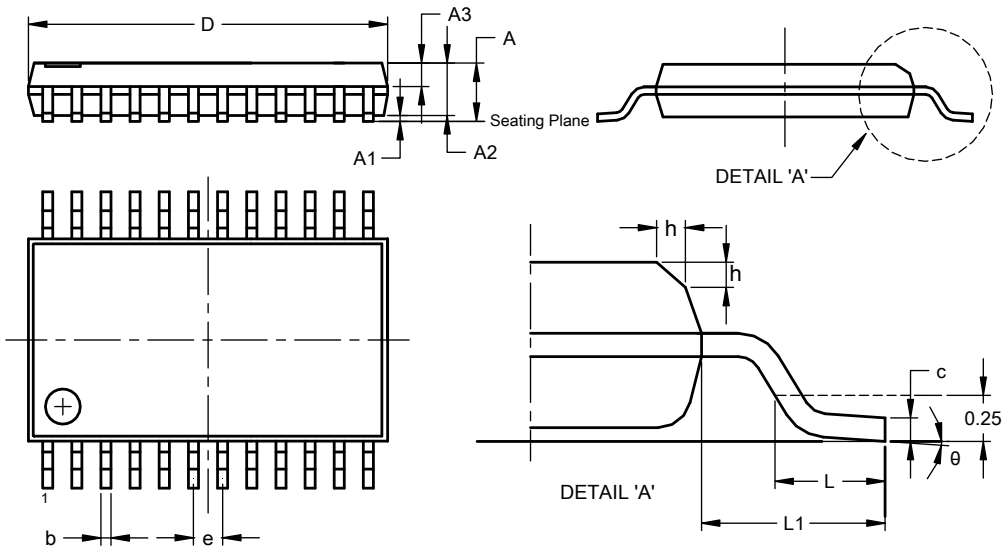
X: Internal Code
Y: Year
W: Week

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Package Outline Dimensions (All dimensions in mm.)

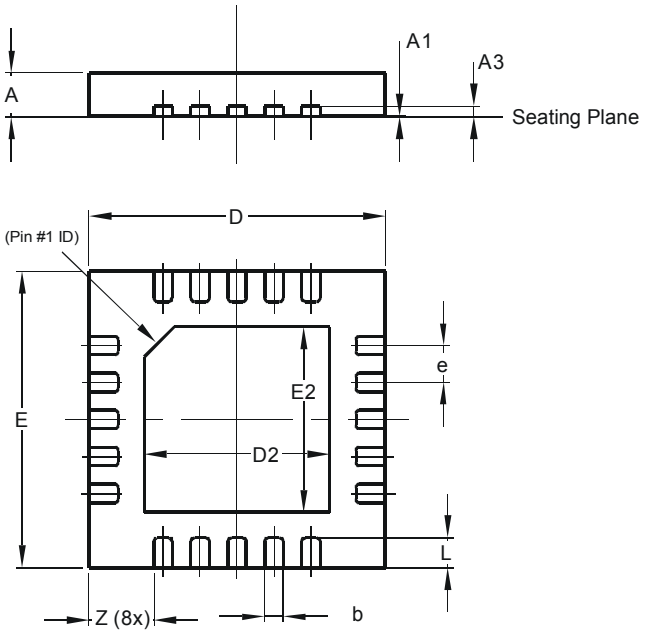
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

SO-24 (Type TH)



SO-24 (Type TH)			
Dim	Min	Max	Typ
A	2.36	2.64	2.54
A1	0.10	0.30	0.20
A2	2.26	2.35	2.30
A3	0.97	1.07	1.02
b	0.39	0.48	-
c	0.25	0.31	-
D	15.20	15.60	15.40
e	1.27BSC		
E	10.10	10.50	10.30
E1	7.40	7.60	7.50
h	0.25	0.75	-
L	0.70	1.00	-
L1	1.40 BSC		
θ	0°	8°	-
All Dimensions in mm			

U-QFN4040-20



U-QFN4040-20			
Dim	Min	Max	Typ
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D2	2.40	2.60	2.50
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	0.50 BSC		
L	0.35	0.45	0.40
Z	-	-	0.875
All Dimensions in mm			

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