NTMS4807N

Power MOSFET
30 V, 14.8 A, N–Channel, SO–8

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- This is a Pb–Free Device

Applications

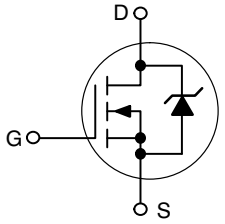
- Disk Drives
- DC–DC Converters
- Printers

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$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	6.1 mΩ @ 10 V	14.8 A
	7.5 mΩ @ 4.5 V	

N–Channel



MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	30	V
Gate–to–Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	12.2	A
		T_A = 70°C		9.8	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	1.55	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	I_D	9.1	A
		T_A = 70°C		7.3	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	P_D	0.86	W
Continuous Drain Current $R_{\theta JA}$, t ≤ 10 s (Note 1)		T_A = 25°C	I_D	14.8	A
		T_A = 70°C		11.8	
Power Dissipation $R_{\theta JA}$, t ≤ 10 s(Note 1)		T_A = 25°C	P_D	2.3	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	50	A
Operating Junction and Storage Temperature			T_J, T_{stg}	–55 to 150	°C
Source Current (Body Diode)			I_S	2.9	A
Single Pulse Drain–to–Source Avalanche Energy (T_J = 25°C, V_{DD} = 30 V, V_{GS} = 10 V, I_L = 14 A_{pk}, L = 1.0 mH, R_G = 25 Ω)			E_{AS}	98	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	80.5	°C/W
Junction–to–Ambient – t ≤ 10 s (Note 1)	$R_{\theta JA}$	54.9	
Junction–to–Foot (Drain)	$R_{\theta JF}$	19.5	
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	145	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

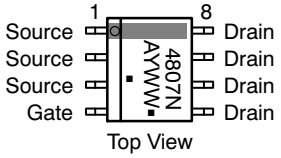
1. Surfacemounted on FR4 board using 1 in sq pad size.
2. Surfacemounted on FR4 board using the minimum recommended pad size.



1

SO–8
CASE 751
STYLE 12

MARKING DIAGRAM/ PIN ASSIGNMENT



Top View

4807N = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMS4807NR2G	SO–8 (Pb–Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				29		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 100°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				6.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 14.8 A			5.1	6.1	mΩ
		V_{GS} = 4.5 V, I_D = 12 A			6.5	7.5	
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 14.8 A			16		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 24 V			2900		pF
Output Capacitance	C_{oss}				562		
Reverse Transfer Capacitance	C_{rss}				307		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 14.8 A			24		nC
Threshold Gate Charge	$Q_{G(TH)}$				3.4		
Gate−to−Source Charge	Q_{GS}				7.7		
Gate−to−Drain Charge	Q_{GD}				10.4		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 14.8 A			46		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 1.0 A, R_G = 6.0 Ω			14		ns
Rise Time	t_r				6.5		
Turn−Off Delay Time	$t_{d(off)}$				47		
Fall Time	t_f				17		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.9 A	T_J = 25°C		0.75	1.0	V
			T_J = 125°C		0.58		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 2.9 A			30		ns
Charge Time	t_a				15		
Discharge Time	t_b				15		
Reverse Recovery Charge	Q_{RR}				23		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			0.66		nH
Drain Inductance	L_D	T_A = 25°C			0.20		nH
Gate Inductance	L_G	T_A = 25°C			1.5		nH
Gate Resistance	R_G	T_A = 25°C			0.9	1.4	Ω

3. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

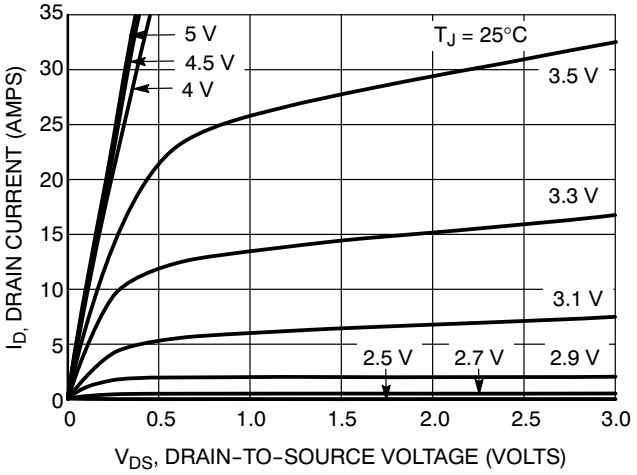


Figure 1. On−Region Characteristics

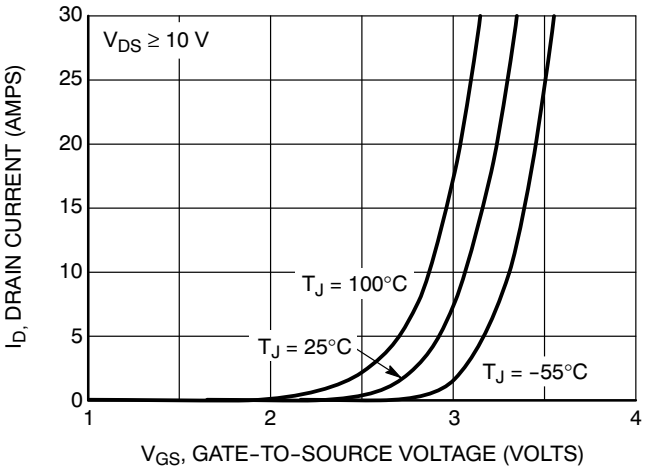


Figure 2. Transfer Characteristics

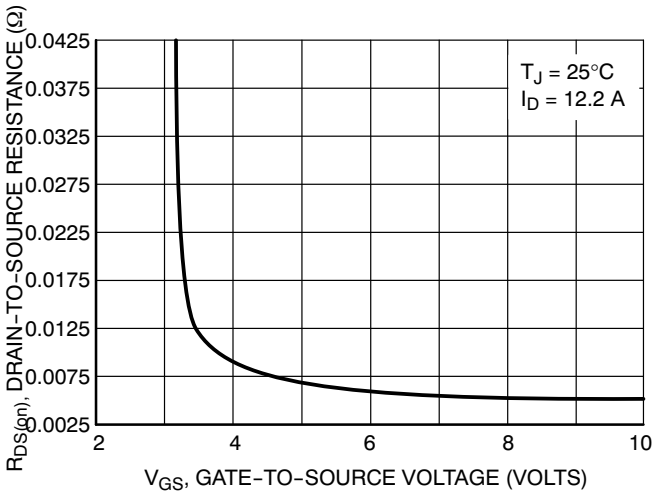


Figure 3. On−Resistance vs. Gate−to−Source Voltage

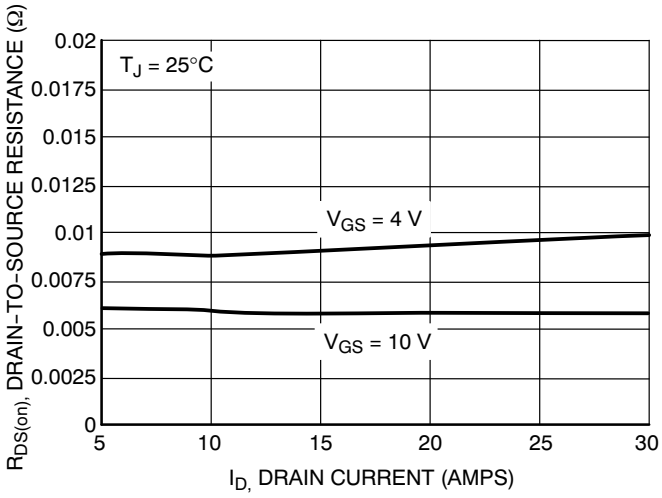


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

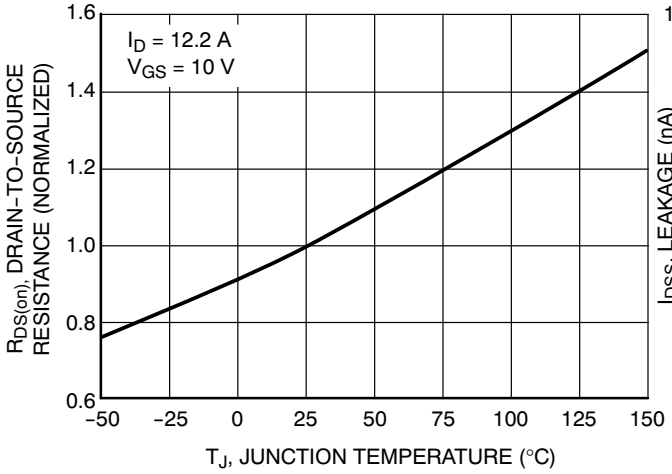


Figure 5. On−Resistance Variation with Temperature

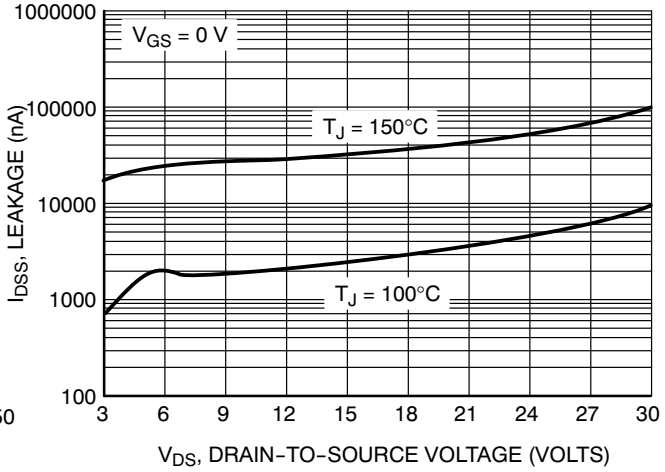


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

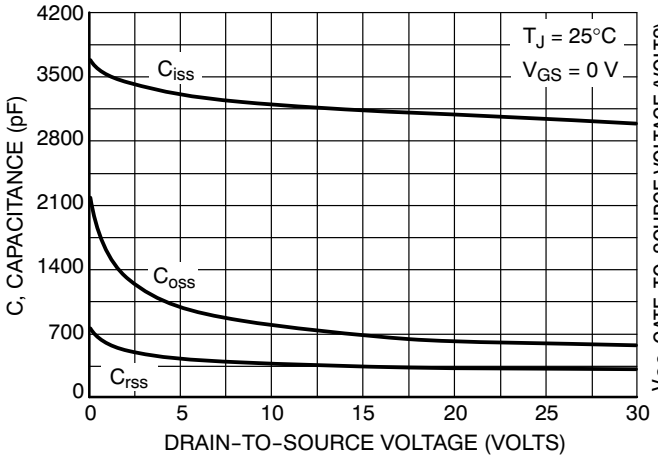


Figure 7. Capacitance Variation

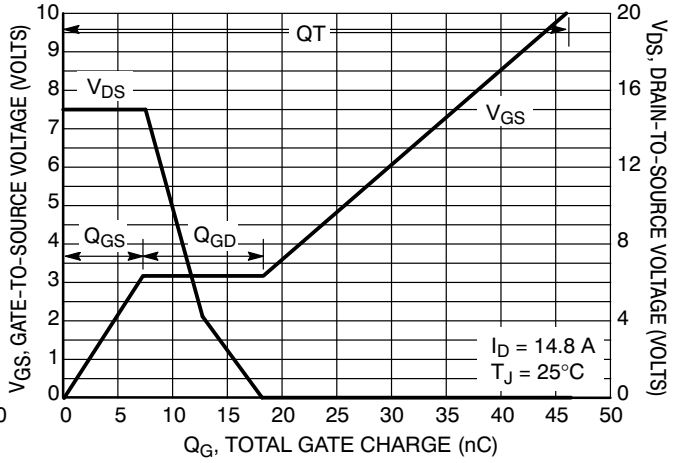


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

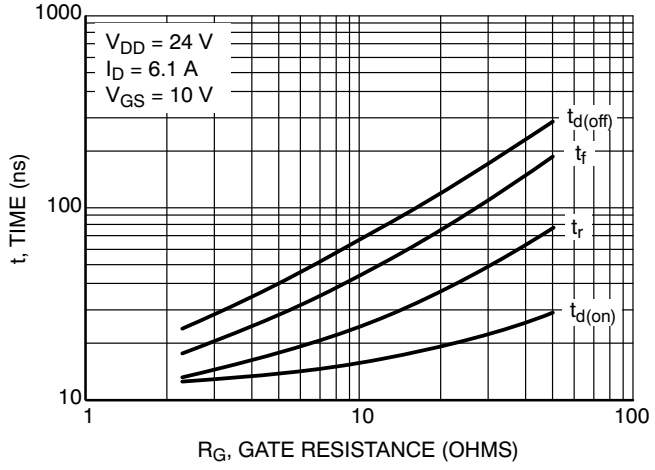


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

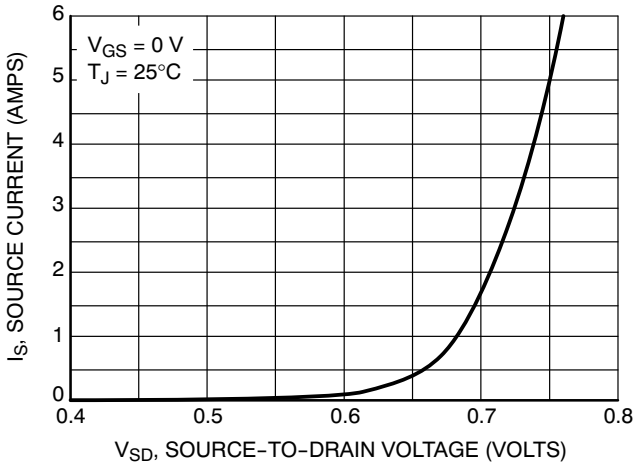


Figure 10. Diode Forward Voltage vs. Current

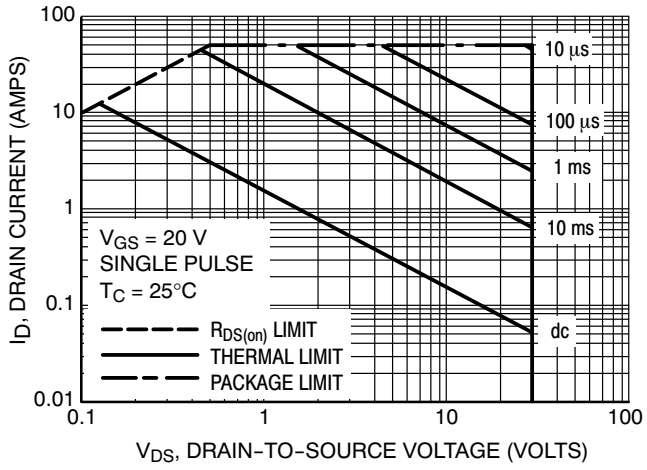


Figure 11. Maximum Rated Forward Biased Safe Operating Area

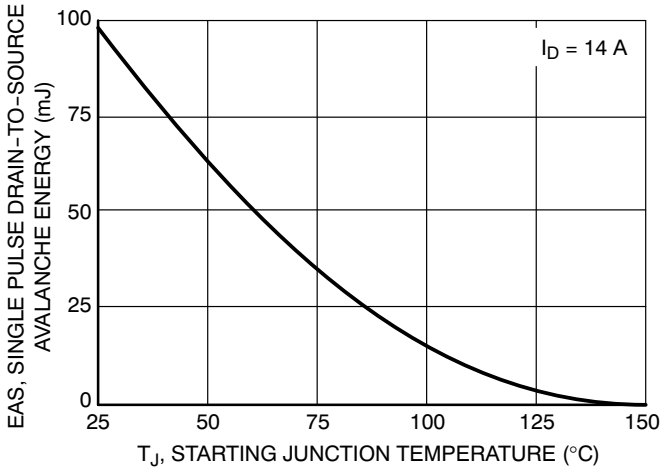
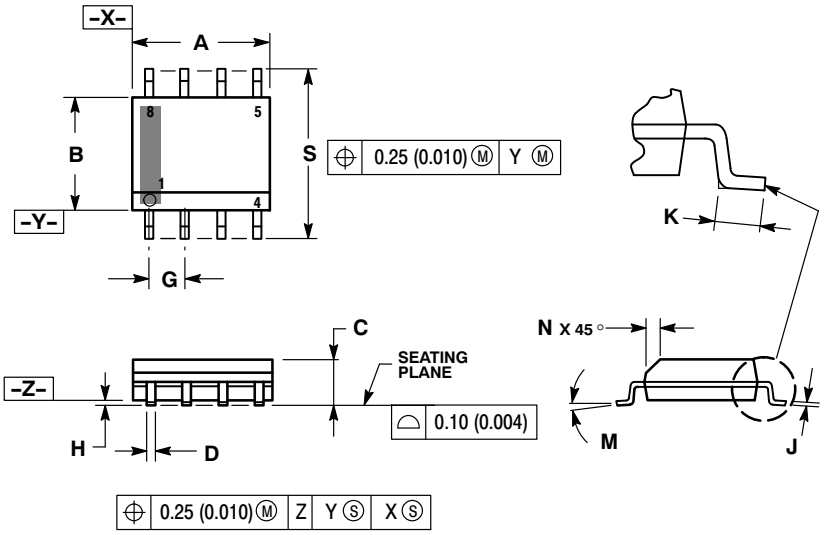


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

PACKAGE DIMENSIONS

SOIC−8
CASE 751−07
ISSUE AJ

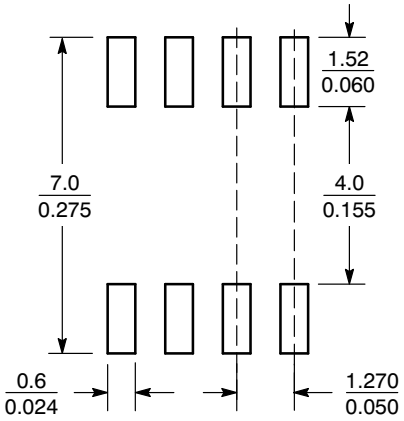


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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