APS12200, APS12210, and APS12230

High-Temperature Precision Hall-Effect Latches

FEATURES AND BENEFITS

- Symmetrical latch switchpoints
- ASIL A functional safety compliance
- Automotive-grade ruggedness and fault tolerance
  - □ Extended AEC-Q100 qualification
  - □ Reverse-battery and 40 V load dump protection
  - □ Operation from –40°C to 175°C junction temperature
  - □ High EMC immunity, ±12 kV HBM ESD
  - □ Output short-circuit and overvoltage protection
  - □ Superior temperature stability
  - □ Resistant to physical stress
- Operation from unregulated supplies, 2.8 to 24 V
- Chopper stabilization
- Solid-state reliability
- Industry-standard packages and pinouts

PACKAGES:

Not to scale



3-pin SOT23W
(suffix LH)



3-pin SIP
(suffix UA)

DESCRIPTION

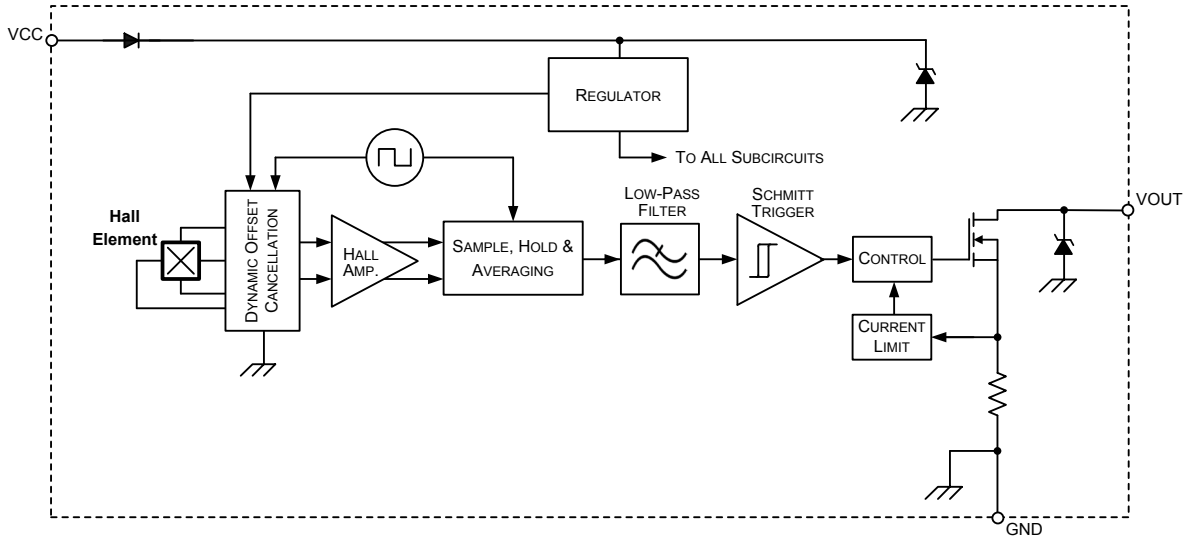
The APS12200, APS12210, and APS12230 are three-wire, planar Hall-effect sensor integrated circuits (ICs). These devices were developed in accordance with ISO 26262:2011 and support a functional safety level of ASIL A.

This family of precision Hall-effect latch ICs feature extended AEC-Q100 qualification and are ideal for high-temperature operation up to 175°C junction temperatures. In addition, the APS12200/10/30 include a number of features designed specifically to maximize system robustness, such as reverse-battery protection, output current limiter, overvoltage, and EMC protection.

The single silicon chip includes: a voltage regulator, a Hall plate, small signal amplifier, chopper stabilization, Schmitt trigger, and a short-circuit-protected open-drain output. A south pole of sufficient strength turns the output on; a north pole of sufficient strength is necessary to turn the output off. The devices include on-board transient protection for all pins, permitting operation directly from a vehicle battery or regulator with supply voltages from 2.8 to 24 V.

Two package styles provide a choice of through-hole or surface mounting. Package type LH is a modified 3-pin SOT23W surface-mount package, while UA is a three-pin ultramini SIP for through-hole mounting. Both packages are lead (Pb) free and RoHS compliant, with 100% matte-tin-plated leadframes.

Functional Block Diagram



SELECTION GUIDE

Part Number	Packing [1]	Mounting	Branding	B_{RP} (Min)	B_{OP} (Max)
APS12200LLHALX	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	A14	–35 G	35 G
APS12200LLHALT [2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	A14		
APS12200LUAA	Bulk, 500 pieces/bag	3-pin SIP through hole	A15		
APS12210LLHALX	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	A16	–80 G	80 G
APS12210LLHALT [2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	A16		
APS12210LUAA	Bulk, 500 pieces/bag	3-pin SIP through hole	A17		
APS12230LLHALX	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	A19	–180 G	180 G
APS12230LLHALT [2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	A19		
APS12230LUAA	Bulk, 500 pieces/bag	3-pin SIP through hole	A20		

[1] Contact Allegro for additional packing options.
[2] Available through authorized Allegro distributors only.

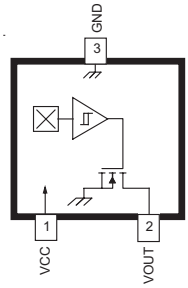
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage [1]	V_{CC}		30	V
Reverse Supply Voltage [1]	V_{RCC}		–18	V
Output Off Voltage [1]	V_{OUT}		30	V
Output Current [2]	I_{OUT}		60	mA
Reverse Output Current	I_{ROUT}		–50	mA
Magnetic Flux Density [3]	B		Unlimited	–
Maximum Junction Temperature	T_J(max)		165	°C
		For 500 hours	175	°C
Storage Temperature	T_{stg}		–65 to 170	°C
ESD Voltage [4]	$V_{ESD(HBM)}$	Human Body Model according to AEC-Q100-002	±12	kV
	$V_{ESD(CDM)}$	Charged Device Model according to AEC-Q100-011	±1	kV
	$V_{ESD(SYS)}$	ISO 10605, System Level	±15	kV

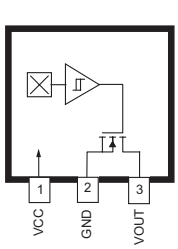
[1] This rating does not apply to extremely short voltage transients such as load dump and/or ESD. Those events have individual ratings, specific to the respective transient voltage event.
[2] Through short-circuit current limiting device.
[3] Guaranteed by design.
[4] System level ESD rating based on characterization performed under ISO 10605:2008 (2 kΩ / 330 pF) with the application circuit shown in Figure 4.

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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
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PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package LH



Package UA

Terminal List

Name	Description	Number	
		Package LH	Package UA
VCC	Connects power supply to chip	1	1
VOUT	Output from circuit	2	3
GND	Ground	3	2

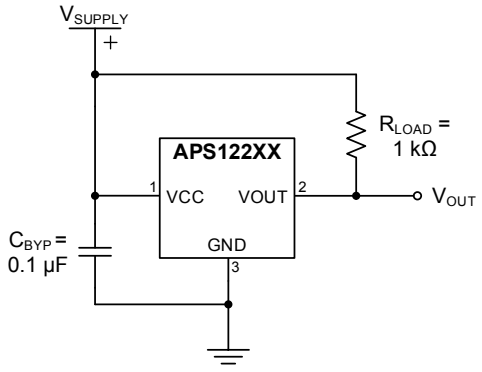


Figure 1: Typical Application Diagram

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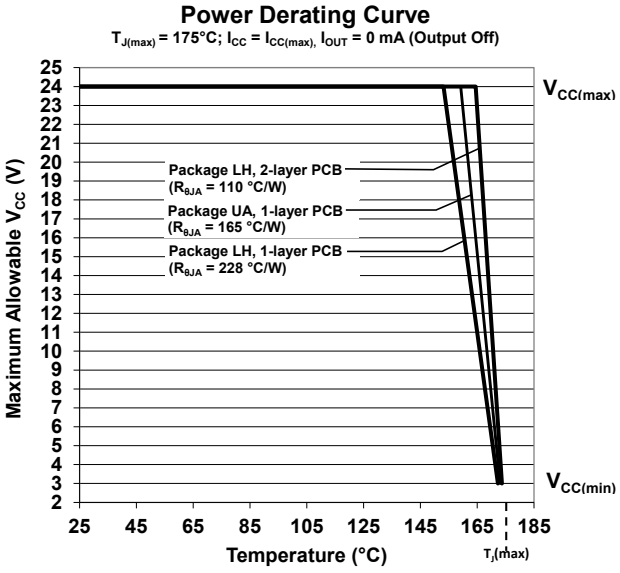
ELECTRICAL CHARACTERISTICS: Valid over full operating voltage, ambient temperature range T_A = –40°C to 150°C, and with C_{BYP} = 0.1 µF (unless otherwise specified)

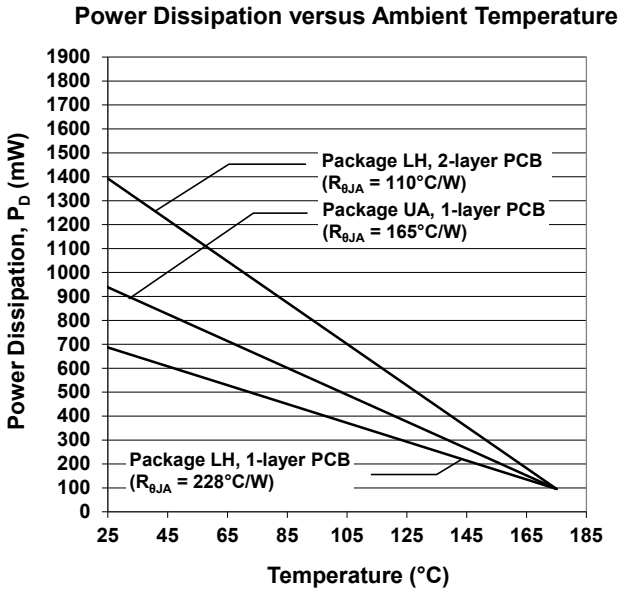
Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ELECTRICAL CHARACTERISTICS						
Forward Supply Voltage	V_{CC}	Operating, T_J < 175°C	2.8	–	24	V
Supply Current	I_{CC}		1	2	3	mA
Output Leakage Current	I_{OUTOFF}	V_{OUTOFF} = 24 V, B < B_{RP}	–	–	10	µA
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	–	200	500	mV
Output Off Voltage	V_{OUTOFF}	B < B_{RP}	–	–	24	V
Power-On Time	t_{ON}	V_{CC} ≥ V_{CC}(min), B < B_{RP}(min) – 10 G, B > B_{OP}(max) + 10 G	–	–	25	µs
Power-On State, Output [3]	POS	V_{CC} ≥ V_{CC}(min), t < t_{ON}		Low		–
Chopping Frequency	f_C		–	800	–	kHz
Output Rise Time [4]	t_r	R_{LOAD} = 1 kΩ, C_L = 20 pF	–	0.2	2	µs
Output Fall Time [4]	t_f	R_{LOAD} = 1 kΩ, C_L = 20 pF	–	0.1	2	µs
TRANSIENT PROTECTION CHARACTERISTICS						
Output Short-Circuit Current Limit	I_{OM}		30	–	60	mA
Output Zener Clamp Voltage	$V_{Zoutput}$	I_{OUT} = 3 mA, T_A = 25°C, Output Off	30	–	–	V
Reverse Battery Current	I_{RCC}	V_{RCC} = –18 V, T_A = 25°C	–	–	–5	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = I_{CC}(max) + 3 mA, T_A = 25°C	30	–	–	V
MAGNETIC CHARACTERISTICS						
Operate Point	B_{OP}	APS12200	5	20	35	G
		APS12210	25	50	80	G
		APS12230	100	150	180	G
Release Point	B_{RP}	APS12200	–35	–20	–5	G
		APS12210	–80	–50	–25	G
		APS12230	–180	–150	–100	G
Hysteresis	B_{HYS}	APS12200	10	40	70	G
		APS12210	50	100	160	G
		APS12230	200	300	360	G
Symmetry	B_{SYM}	B_{OP} + B_{RP}	–27.5	–	27.5	G
Magnetic Offset	B_{OFF}	(B_{OP} + B_{RP}) / 2	–13.75	–	13.75	G

[1] Typical data are at T_A = 25°C and V_{CC} = 12 V.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] Guaranteed by device design and characterization.
[4] C_L = oscilloscope probe capacitance.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in^2 of copper area each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W

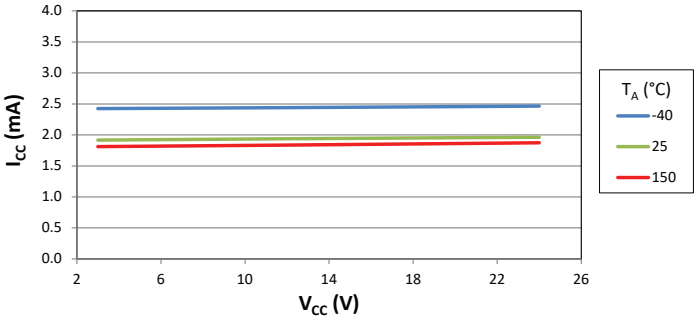




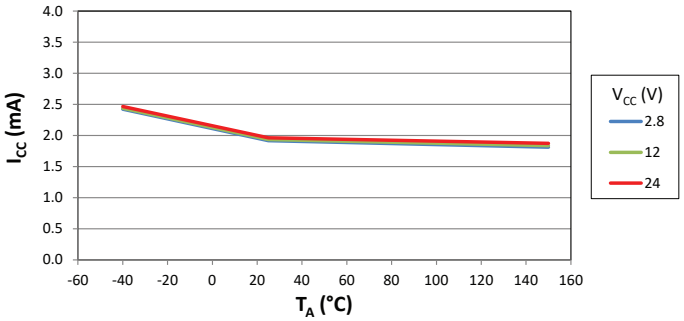
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CHARACTERISTIC PERFORMANCE DATA
Electrical Characteristics

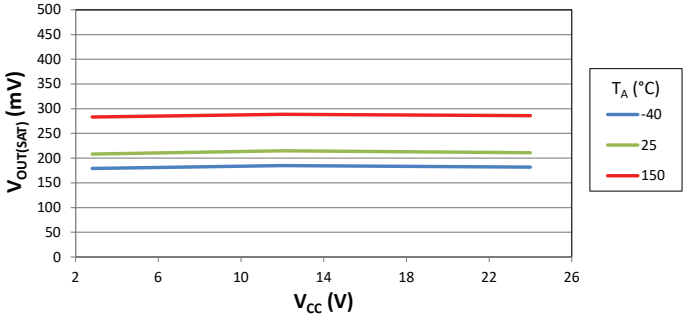
Average Supply Current versus Supply Voltage



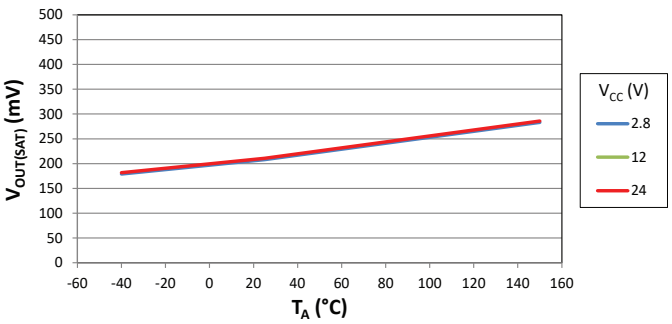
Average Supply Current versus Ambient Temperature



Average Low Output Voltage versus Supply Voltage for I_{OUT} = 20 mA

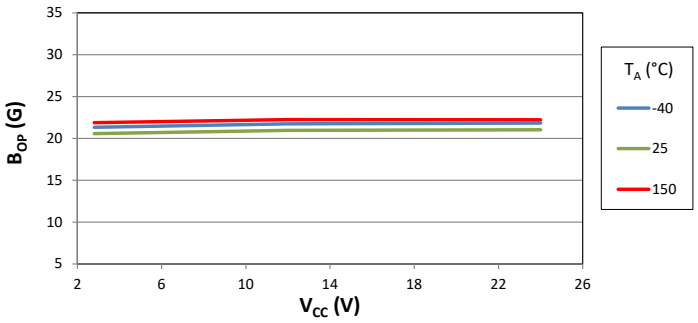


Average Low Output Voltage versus Ambient Temperature for I_{OUT} = 20 mA

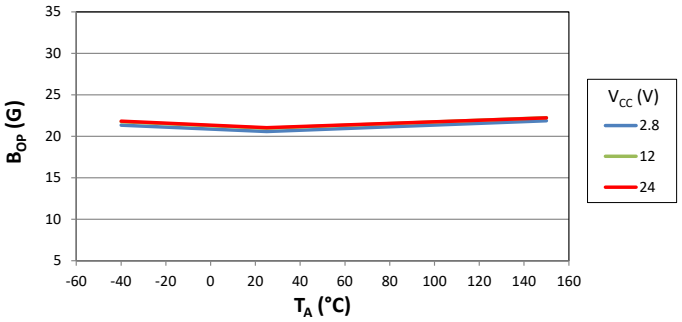


CHARACTERISTIC PERFORMANCE DATA (continued)
APS12200 Magnetic Characteristics

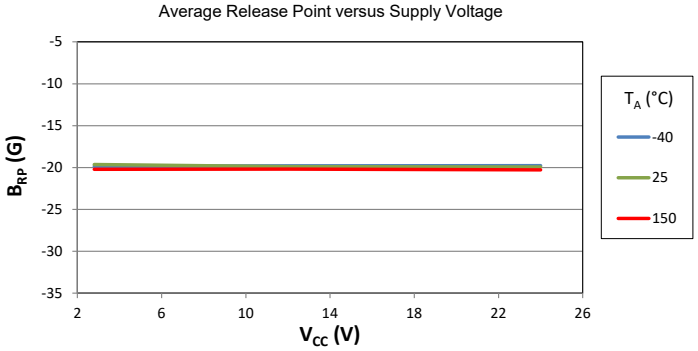
Average Operate Point versus Supply Voltage



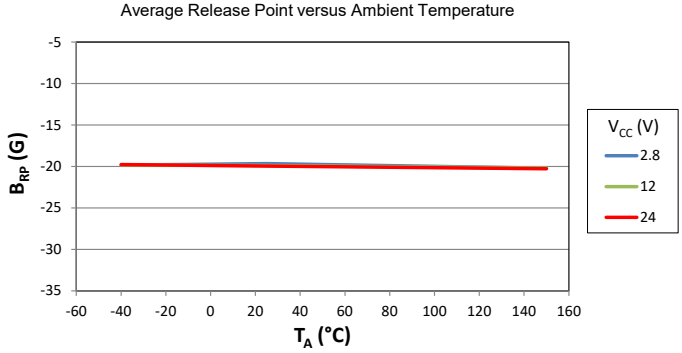
Average Operate Point versus Ambient Temperature



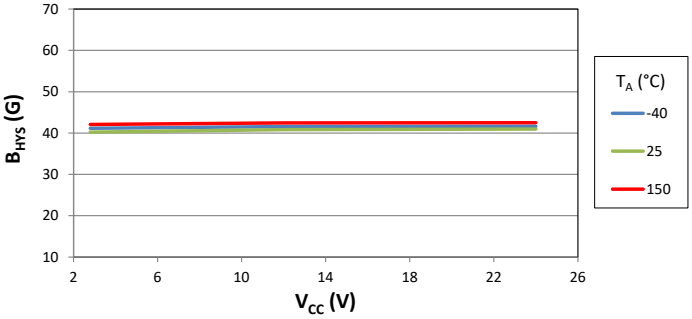
Average Release Point versus Supply Voltage



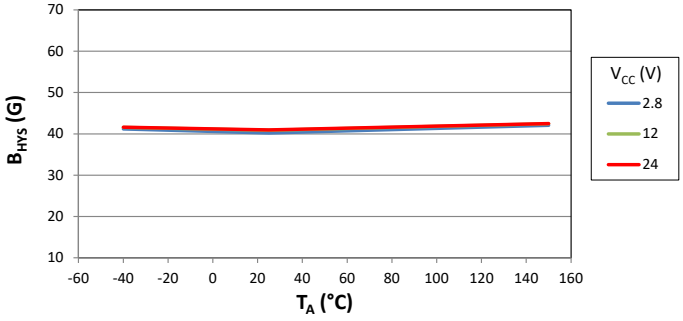
Average Release Point versus Ambient Temperature



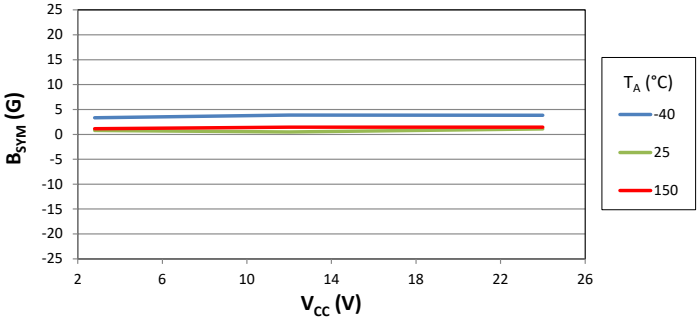
Average Switchpoint Hysteresis versus Supply Voltage



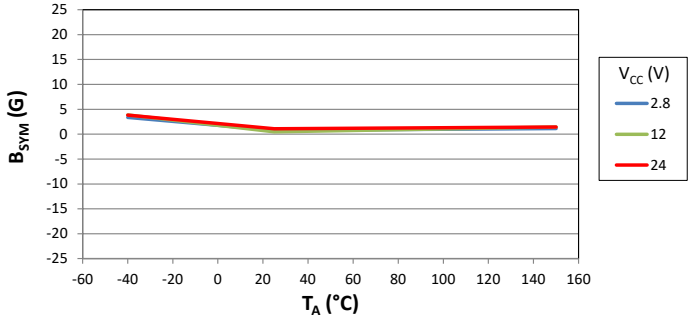
Average Switchpoint Hysteresis versus Ambient Temperature



Average B_{OP} + B_{RP} Symmetry versus Supply Voltage



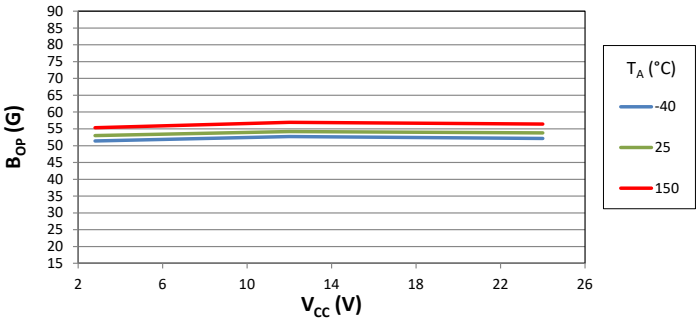
Average B_{OP} + B_{RP} Symmetry versus Ambient Temperature



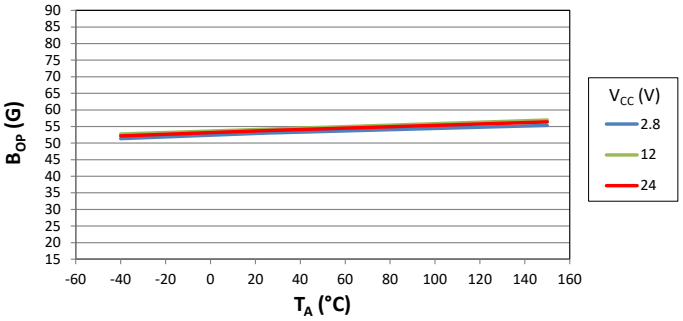
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CHARACTERISTIC PERFORMANCE DATA (continued)
APS12210 Magnetic Characteristics

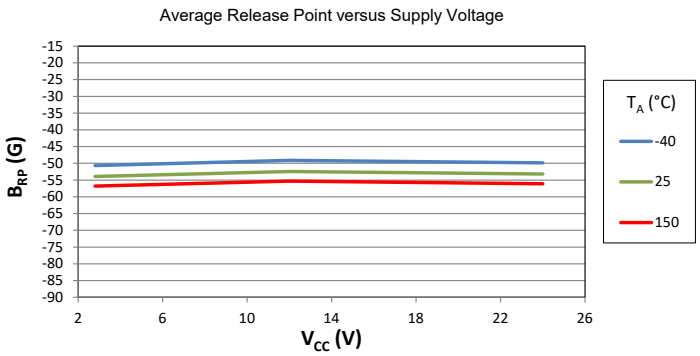
Average Operate Point versus Supply Voltage



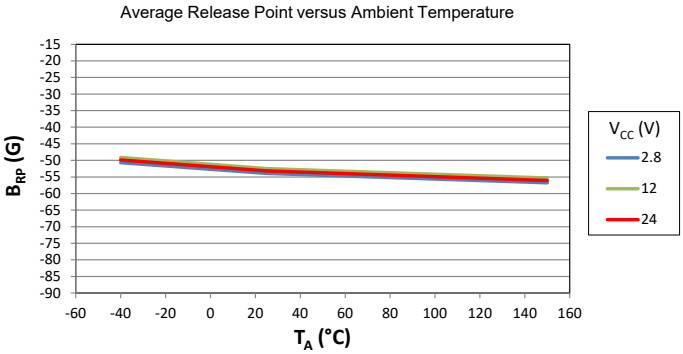
Average Operate Point versus Ambient Temperature



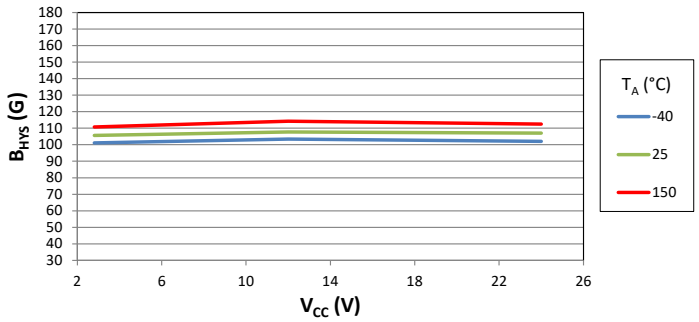
Average Release Point versus Supply Voltage



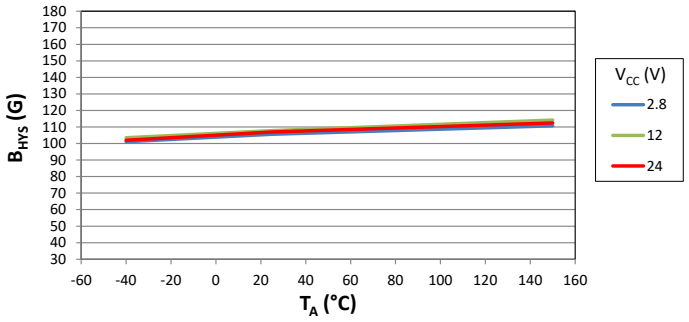
Average Release Point versus Ambient Temperature



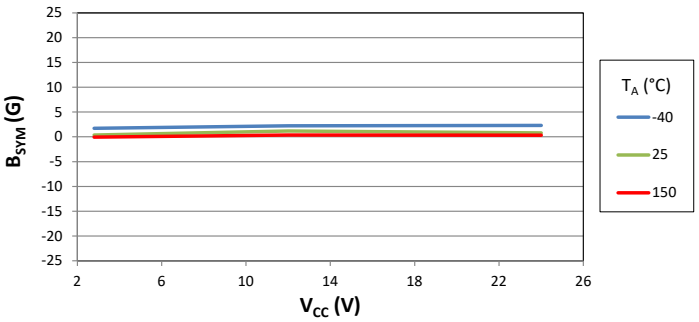
Average Switchpoint Hysteresis versus Supply Voltage



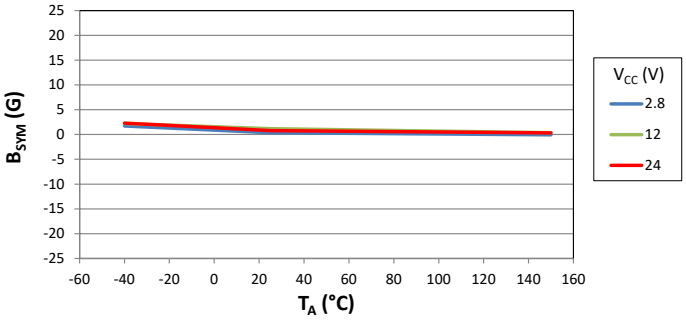
Average Switchpoint Hysteresis versus Ambient Temperature



Average B_{OP} + B_{RP} Symmetry versus Supply Voltage

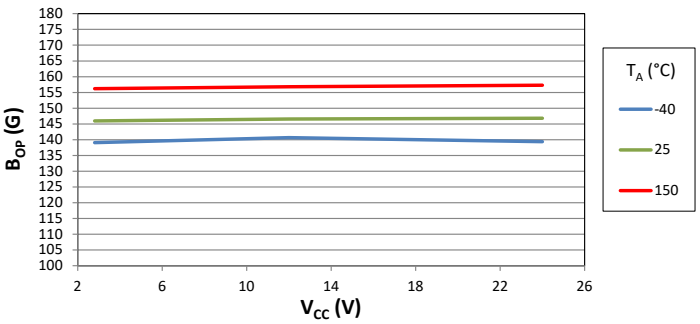


Average B_{OP} + B_{RP} Symmetry versus Ambient Temperature

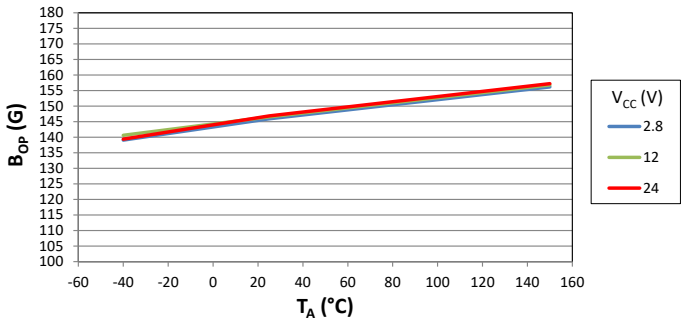


CHARACTERISTIC PERFORMANCE DATA (continued)
APS12230 Magnetic Characteristics

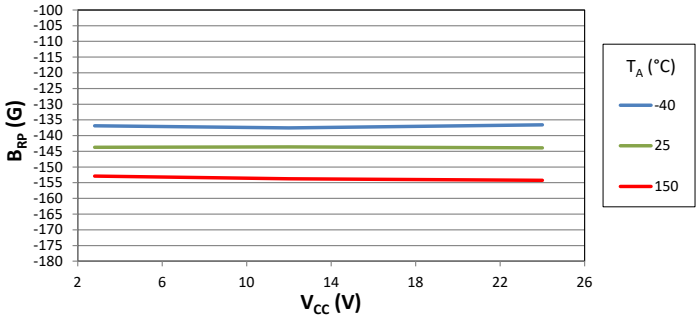
Average Operate Point versus Supply Voltage



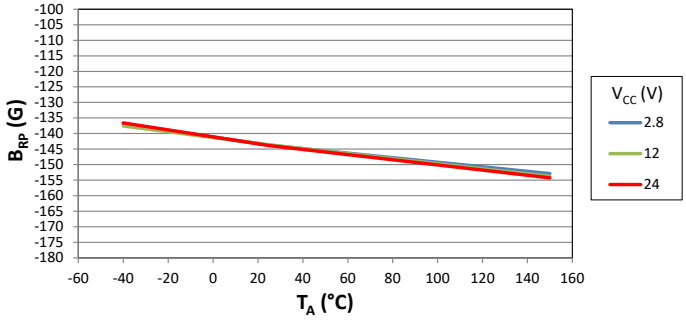
Average Operate Point versus Ambient Temperature



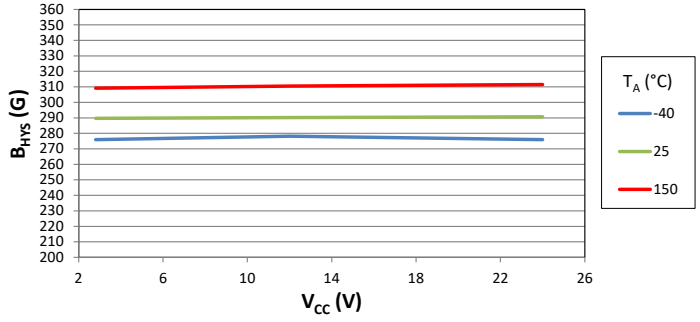
Average Release Point versus Supply Voltage



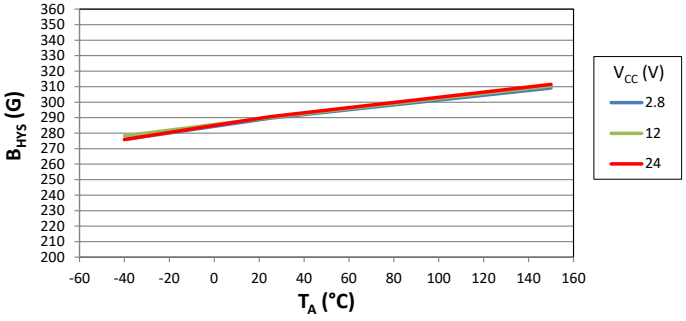
Average Release Point versus Ambient Temperature



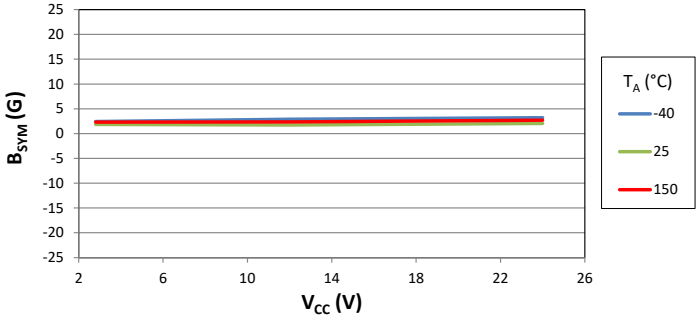
Average Switchpoint Hysteresis versus Supply Voltage



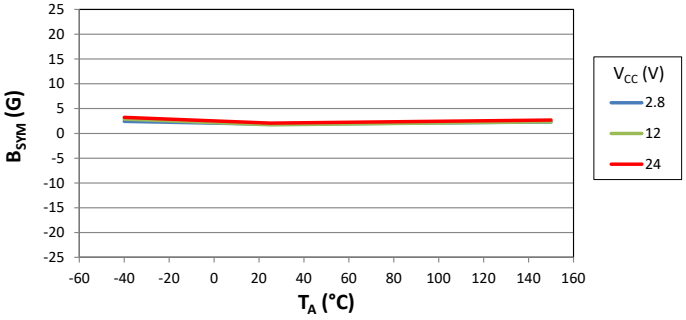
Average Switchpoint Hysteresis versus Ambient Temperature



Average B_{OP} + B_{RP} Symmetry versus Supply Voltage



Average B_{OP} + B_{RP} Symmetry versus Ambient Temperature



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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

OPERATION

The output of these devices switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OP} (see Figure 2). After turn-on, the output voltage is $V_{OUT(SAT)}$. The output transistor is capable of continuously sinking up to 30 mA. When the magnetic field is reduced below the release point, B_{RP}, the device output goes high (turns off) to V_{OUTOFF}. The difference in the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Removal of the magnetic field will leave the device output latched on if the last crossed switchpoint is B_{OP}, or latched off if the last crossed switch point is B_{RP}.

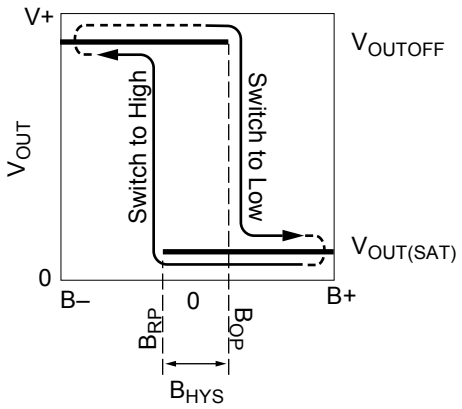


Figure 2: Switching Behavior of Latches

On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates increasing north polarity field strength.

POWER-ON BEHAVIOR

Device power-on occurs once t_{ON} has elapsed. During the time prior to t_{ON}, and after $V_{CC} \geq V_{CC}(min)$, the output state is $V_{OUT(SAT)}$ (Low). After t_{ON} has elapsed, the output will correspond with the applied magnetic field for $B > B_{OP}$ or $B < B_{RP}$. See Figure 3 for an example.

Powering-on the device in the hysteresis range (less than B_{OP} and higher than B_{RP}) will give an output state of $V_{OUT(SAT)}$. The correct state is attained after the first excursion beyond B_{OP} or B_{RP}.

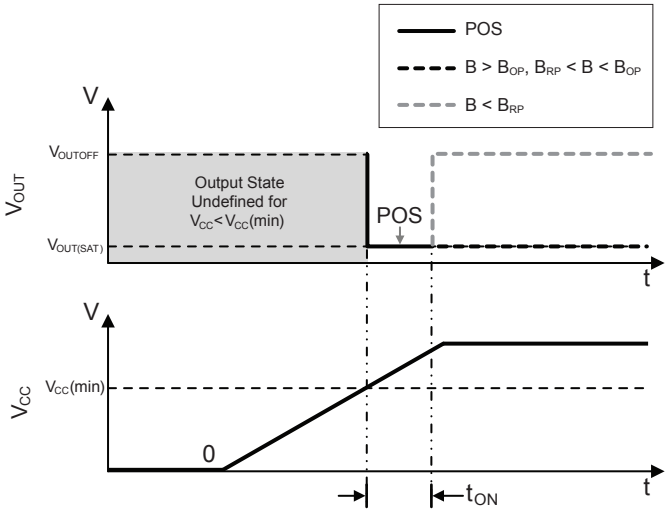


Figure 3: Power-On Timing Diagram

FUNCTIONAL SAFETY

The APS12200, APS12210, and APS12230 were designed in accordance with the international standard for automotive functional safety, ISO 26262:2011. These products achieve an ASIL (Automotive Safety Integrity Level) rating of ASIL A according to the standard. The APS12200, APS12210, and APS12230 are all classified as a SEooC (Safety Element out of Context) and can be easily integrated into safety-critical systems requiring higher ASIL ratings that incorporate external diagnostics or use measures such as redundancy. Safety documentation will be provided to support and guide the integration process. For further information, contact your local Allegro field applications engineer or sales representative.

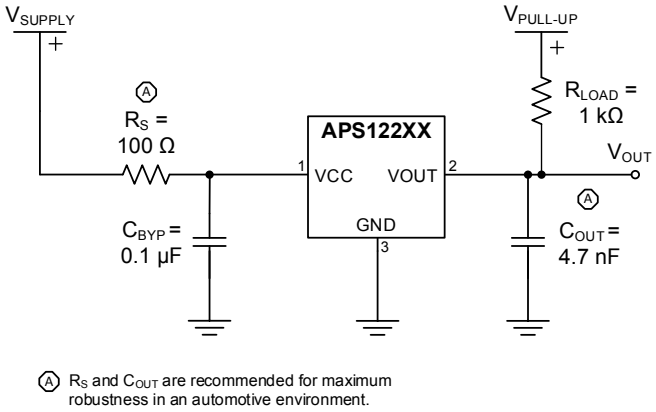


Figure 4: Enhanced Protection Circuit

APPLICATIONS

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to guarantee correct performance under harsh environmental conditions and to reduce noise from internal circuitry. As is shown in Figure 1: Typical Application Circuit, a 0.1 µF capacitor is required. In applications where maximum robustness is required, such as in an automobile, additional measures may be taken. In Figure 4: Enhanced Protection Circuit, a resistor in series with the VCC pin and a capacitor on the VOUT pin enhance the EMC immunity of the device. It is up to the user to fully qualify the Allegro sensor IC in their end system to ensure they achieve their system requirements.

These devices are sensitive in the direction perpendicular to the branded face, as depicted in Figure 5. For further information, extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices AN27703.1*
- *Soldering Methods for Allegro's Products – SMD and Through-Hole, AN26009*

All are provided on the Allegro website:

www.allegromicro.com

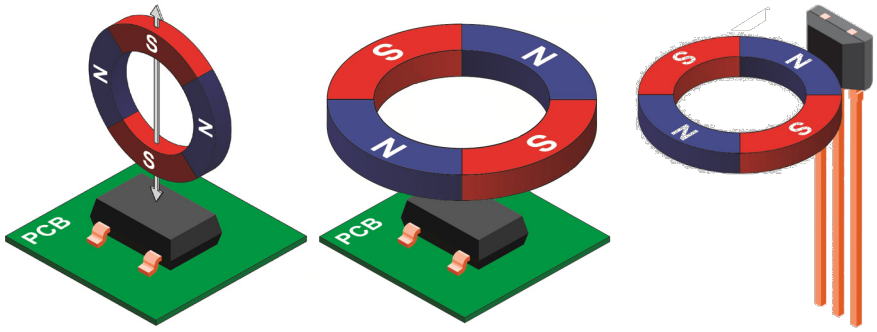


Figure 5: Sensing Configurations

CHOPPER STABILIZATION

A limiting factor for switchpoint accuracy when using Hall-effect technology is the small signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The Allegro technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. Figure 6 illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed. Allegro's innovative chopper stabilization technique uses a high-frequency clock. The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the APS12200, APS12210, and APS12230 that use this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic and sample-and-hold circuits.

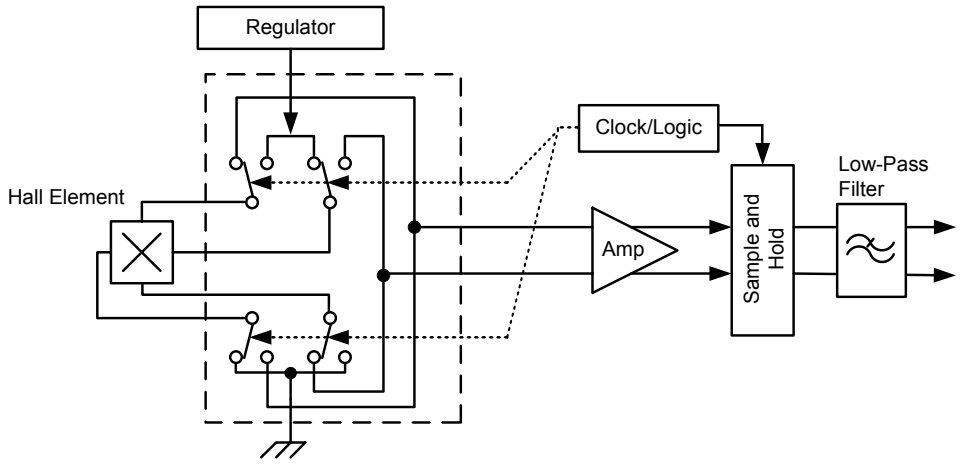


Figure 6: Model of Chopper Stabilization (Dynamic Offset Cancellation)

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

POWER DERATING

The device must be operated below the maximum junction temperature of the device, T_J(max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The resulting power dissipation capability directly reflects upon the ability of the device to withstand extreme operating conditions. The junction temperature mission profile specified in the Absolute Maximum Ratings table designates a total operating life capability based on qualification for the most extreme conditions, where T_J may reach 175°C.

The silicon IC is heated internally when current is flowing into the VCC terminal. When the output is on, current sinking into the VOUT terminal generates additional heat. This may increase the junction temperature, T_J, above the surrounding ambient temperature. The APS12200, APS12210, and APS12230 are permitted to operate up to T_J = 175°C. As mentioned above, an operating device will increase T_J according to equations 1, 2, and 3 below. This allows an estimation of the maximum ambient operating temperature.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 2 mA, V_{OUT} = 185 mV, I_{OUT} = 20 mA (output on), and $R_{\theta JA}$ = 165°C/W, then:

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{OUT}) = (12\ V \times 2\ mA) + (185\ mV \times 20\ mA) = 24\ mW + 3.7\ mW = 27.7\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 27.7\ mW \times 165°C/W = 4.6°C$$

$$T_J = T_A + \Delta T = 25°C + 4.6°C = 29.6°C$$

A worst-case estimate, P_D(max), represents the maximum allowable power level (V_{CC}(max), I_{CC}(max)), without exceeding T_J(max), at a selected $R_{\theta JA}$.

For example, given the conditions $R_{\theta JA}$ = 228°C/W, T_J(max) = 175°C, V_{CC}(max) = 24 V, I_{CC}(max) = 4 mA, V_{OUT} = 500 mV, and I_{OUT} = 25 mA (output on), the maximum allowable operating ambient temperature can be determined.

The power dissipation required for the output is shown below:

$$P_D(V_{OUT}) = V_{OUT} \times I_{OUT} = 500\ mV \times 25\ mA = 12.5\ mW$$

The power dissipation required for the IC supply is shown below:

$$P_D(V_{CC}) = V_{CC} \times I_{CC} = 24\ V \times 4\ mA = 96\ mW$$

Next, by inverting using equation 2:

$$\Delta T = P_D \times R_{\theta JA} = [P_D(V_{OUT}) + P_D(V_{CC})] \times 228°C/W = (12.5\ mW + 96\ mW) \times 228°C/W = 108.5\ mW \times 228°C/W = 24.7°C$$

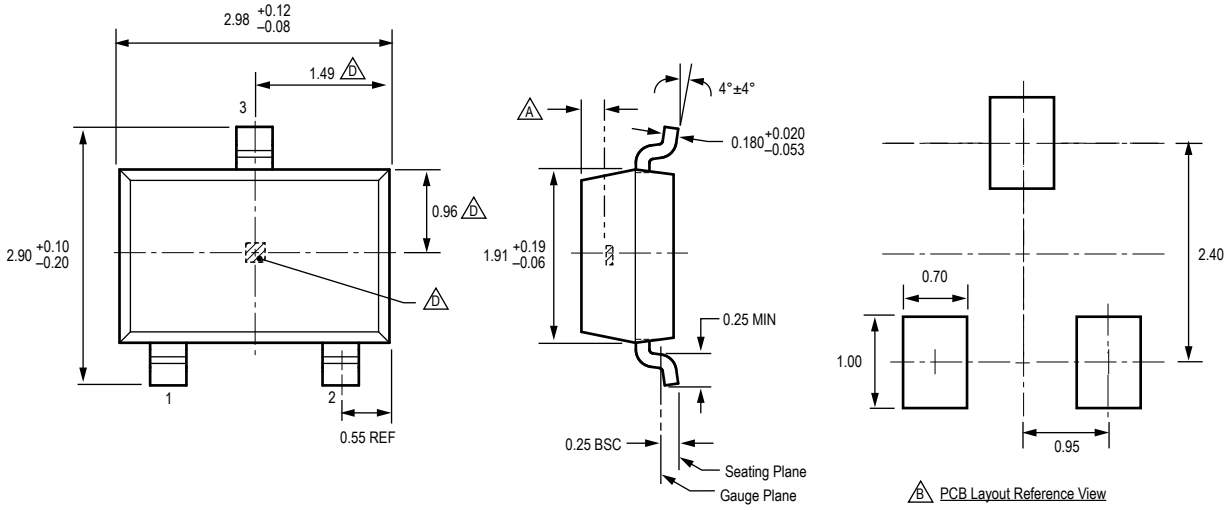
Finally, by inverting equation 3 with respect to voltage:

$$T_A(est) = T_J(max) - \Delta T = 175°C - 24.7°C = 150.3°C$$

In the above case, there is sufficient power dissipation capability to operate up to T_A(est). The example indicates that T_A(max) can be as high as 150.3°C without exceeding T_J(max). However, the T_A(max) rating of the devices is 150°C; the APS12200, APS12210, and APS12230 performance is not guaranteed above T_A = 150°C.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Package LH, 3-Pin (SOT-23W)



For Reference Only; not for tooling use (reference dwg. 802840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

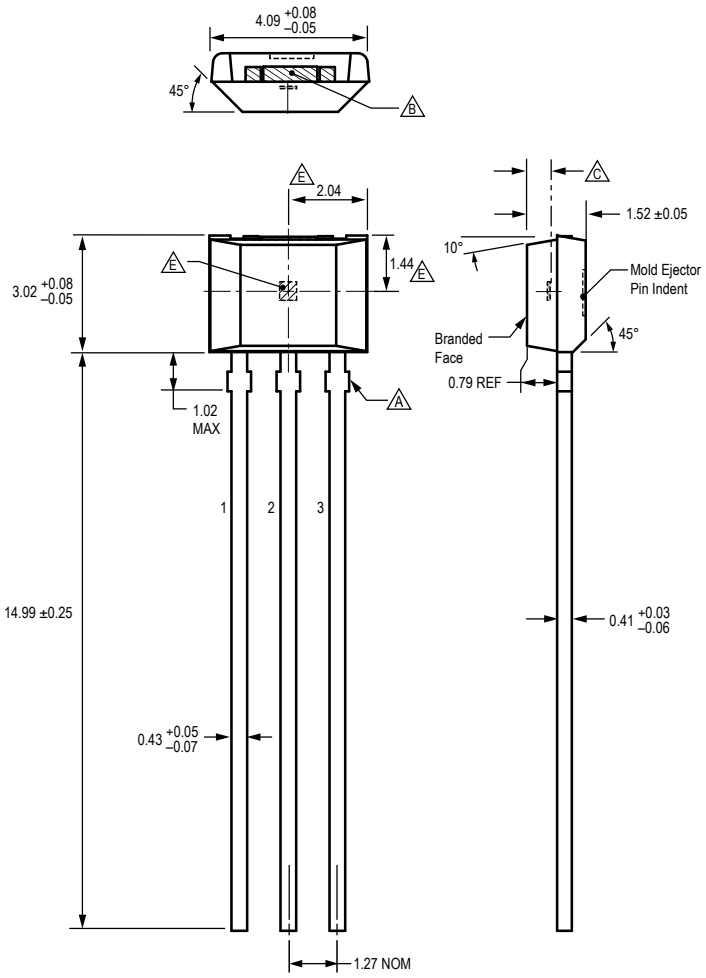
A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

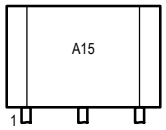
Package UA, 3-Pin SIP



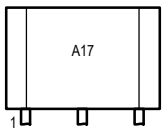
For Reference Only; not for tooling use (reference DWG-9065)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Dambar removal protrusion (6X)
B Gate and tie bar burr area
C Active Area Depth, 0.50 mm REF
D Branding scale and appearance at supplier discretion
E Hall element (not to scale)

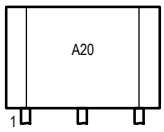
D Standard Branding Reference View



APS12200LUAA



APS12210LUAA



APS12230LUAA

Revision History

Number	Date	Description
–	March 6, 2018	Initial release
1	February 11, 2019	Minor editorial updates

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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
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