19-3026; Rev 1; 11/04

MAXIM

# +2.97V to +5.5V, 125Mbps to 200Mbps Limiting Amplifier with Loss-of-Signal Detector



## General Description

The MAX3645 limiting amplifier functions as a data quantizer and is pin compatible with the Mindspeed MC2045-2 and MC2045-2Y postamplifiers. The amplifier accepts a wide range of input voltages and provides constant-level positive emitter-coupled logic (PECL) output voltages with controlled edge speeds.

The MAX3645 features an integrated power detector with complementary PECL loss-of-signal (LOS) outputs that indicate when the input power level drops below a programmable threshold. An optional squelch function holds the data outputs at static levels during a LOS condition.

The MAX3645 operates from a single +3.3V or +5.0V power supply over a -40°C to +85°C temperature range. It is available in 16-pin SO and 16-pin QSOP packages.

## Applications

SONET 155Mbps Transceivers

Fast Ethernet Receivers

FDDI 125Mbps Receivers

FTTx Receivers

ESCON Receivers

## Features

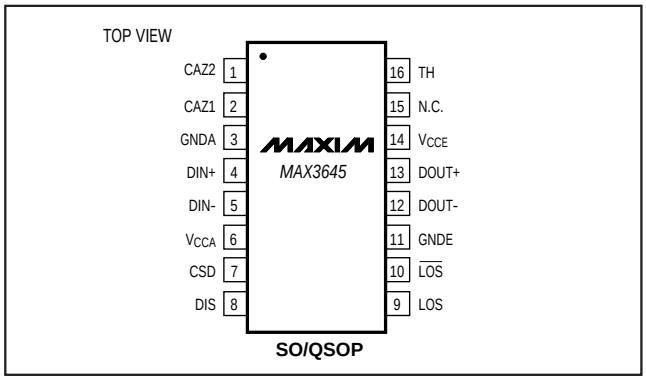
- **Pin Compatible with the Mindspeed MC2045-2/MC2045-2Y**
- **500µV Input Sensitivity (BER = $10^{-12}$)**
- **Compatible with 4B/5B Data Coding**
- **Programmable LOS Threshold**
- **Stable LOS Threshold Over Supply Range**
- **Output Disable Function and Automatic Squelch**
- **Single +3.3V or +5.0V Power Supply**
- **18mA Supply Current**

## Ordering Information

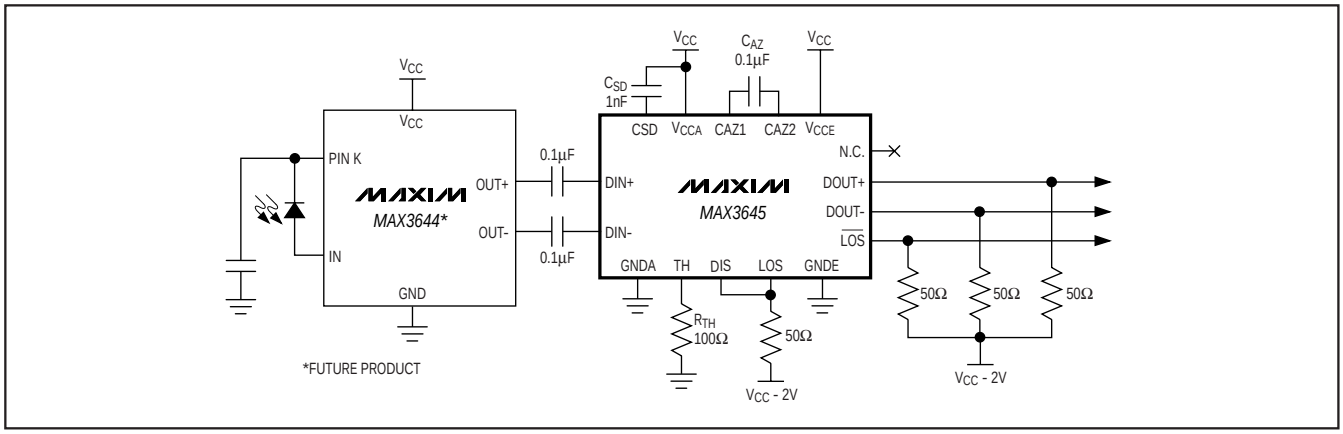
| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX3645ESE | -40°C to +85°C | 16 SO |
| MAX3645EEE | -40°C to +85°C | 16 QSOP |
| MAX3645EEE+ | -40°C to +85°C | 16 QSOP |

*+Denotes lead-free package.*

## Pin Configuration




## Typical Application Circuit






***For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.***

# +2.97V to +5.5V, 125Mbps to 200Mbps Limiting Amplifier with Loss-of-Signal Detector

## ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage ($V_{CCA}$, $V_{CCE}$) .....-0.5V to +7.0V
Voltage at CAZ1, CAZ2, DIN+,
DIN-, CSD, DIS, TH .....-0.5V to ($V_{CC}$ + 0.5V)
PECL Output Current (DOUT+, DOUT-, LOS, $\overline{LOS}$) .....50mA
Differential Voltage between CAZ1 and CAZ2.....-1.5V to +1.5V
Differential Voltage between DIN+ and DIN- .....-1.5V to +1.5V

Continuous Power Dissipation ($T_A$ = +85°C)
16-Pin SO (derate 8.7mW/°C above +85°C).....565mW
16-Pin QSOP (derate 8.3mW/°C above +85°C).....540mW
Storage Ambient Temperature Range ($T_S$).....-65°C to +160°C
Lead Temperature (soldering, 10s).....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +2.97V to +5.5V, PECL outputs are terminated with 50Ω to $V_{CC}$ - 2V, $R_{TH}$ = 100Ω, $C_{AZ}$ = 0.1µF, $C_{SD}$ = 1nF, $T_A$ = -40°C to +85°C. Typical values are at $V_{CC}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Supply Current | $I_{CC}$ | Excludes PECL termination currents | | 18 | 27 | mA |
| **INPUT SPECIFICATIONS** | | | | | | |
| Input Resistance | $R_{IN}$ | Single ended; $V_{IN}$ = ±200mV | 3.3 | 4.8 | 6.4 | kΩ |
| Input Sensitivity (Note 1) | $V_{IN-MIN}$ | Single ended | | | 0.5 | $mV_{P-P}$ |
| | | Differential | | | 1.0 | |
| Input Overload (Note 1) | $V_{IN-MAX}$ | Single ended | 750 | | | $mV_{P-P}$ |
| | | Differential | 1500 | | | |
| Input-Referred Offset Voltage | | Unterminated input, output offset divided by DC gain (Note 2) | | 2 | 40 | µV |
| Input Common-Mode Voltage | $V_{CMM}$ | | | $V_{CC}$ - 0.87 | | V |
| Input-Referred RMS Noise | $V_{IN-NOISE}$ | (Notes 2, 3) | | 36 | 50 | $µV_{RMS}$ |
| DIS Input High | $V_{IH}$ | PECL or CMOS logic | $V_{CC}$ - 1160 | | $V_{CC}$ | mV |
| DIS Input Low | $V_{IL}$ | PECL or CMOS logic | 0 | | $V_{CC}$ - 1480 | mV |
| DIS Input Current | $I_{IL}$, $I_{IH}$ | 0V ≤ $V_{DIS}$ ≤ $V_{CC}$ | -10 | | +10 | µA |
| **OUTPUT SPECIFICATIONS** | | | | | | |
| PECL Output-Voltage High | | (Notes 1, 2) | $V_{CC}$ - 1085 | | $V_{CC}$ - 880 | mV |
| PECL Output-Voltage Low | | (Notes 1, 2) | $V_{CC}$ - 1830 | | $V_{CC}$ - 1555 | mV |
| Data Output Transition Time | $t_R$, $t_F$ | 20% to 80% (Notes 1, 2, 4) | | 0.7 | 1.4 | ns |
| Pulse-Width Distortion | PWD | (Notes 1, 2, 4, 5) | | 30 | 200 | ps |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +2.97V to +5.5V, PECL outputs are terminated with 50Ω to $V_{CC}$ - 2V, $R_{TH}$ = 100Ω, $C_{AZ}$ = 0.1µF, $C_{SD}$ = 1nF, $T_A$ = -40°C to +85°C. Typical values are at $V_{CC}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **TRANSFER CHARACTERISTICS** | | | | | | |
| Bandwidth | | Gain = 60dB | 150 | 250 | | MHz |
| Low-Frequency Cutoff | | $C_{AZ}$ = open | | 500 | | kHz |
| | | $C_{AZ}$ = 0.1µF | | 0.5 | | |
| **LOSS-OF-SIGNAL SPECIFICATIONS** (Notes 2, 4, 6) | | | | | | |
| LOS Sensitivity Range | | 0Ω ≤ $R_{TH}$ ≤ 2kΩ | 2 | | 20 | $mV_{P-P}$ |
| LOS Hysteresis | | 10log ($V_{DEASSERT}/V_{ASSERT}$) | 1.4 | 2 | | dB |
| LOS Assert/Deassert Time | | (Note 7) | 2.3 | | 80.0 | µs |
| LOS Assert Level | | $R_{TH}$ = 0Ω, low setting | 0.5 | 0.9 | 1.3 | $mV_{P-P}$ |
| | | $R_{TH}$ = 1kΩ, medium setting | 4.8 | 6.6 | 8.3 | |
| | | $R_{TH}$ = 2kΩ, high setting | 12 | 17 | 22 | |
| LOS Deassert Level | | $R_{TH}$ = 0Ω, low setting | 1.1 | 1.5 | 1.9 | $mV_{P-P}$ |
| | | $R_{TH}$ = 1kΩ, medium setting | 8.0 | 10.8 | 13.5 | |
| | | $R_{TH}$ = 2kΩ, high setting | 20 | 28 | 36 | |
| Signal-Dectect Filter Resistance | $R_{SD}$ | Pin 7 | 14 | 20 | 26 | kΩ |

**Note 1:** Between sensitivity and overload, the output amplitude is >95% of the fully limited amplitude and all AC specifications are met.
**Note 2:** Guaranteed by design and characterization.
**Note 3:** Noise is derived from BER measurement.
**Note 4:** The data input transition time is controlled by a 4th-order Bessel filter with $f_{-3dB}$ = 0.75 × data rate.
**Note 5:** PWD = [(width of wider pulse) - (width of narrower pulse)] / 2, measured with 155Mbps 0011 pattern.
**Note 6:** All LOS specifications are measured using a 155Mbps $2^{23}$ - 1 PRBS pattern.
**Note 7:** The signal at the input is switched between two amplitudes, SIGNAL_ON and SIGNAL_OFF, as shown in Figure 1.

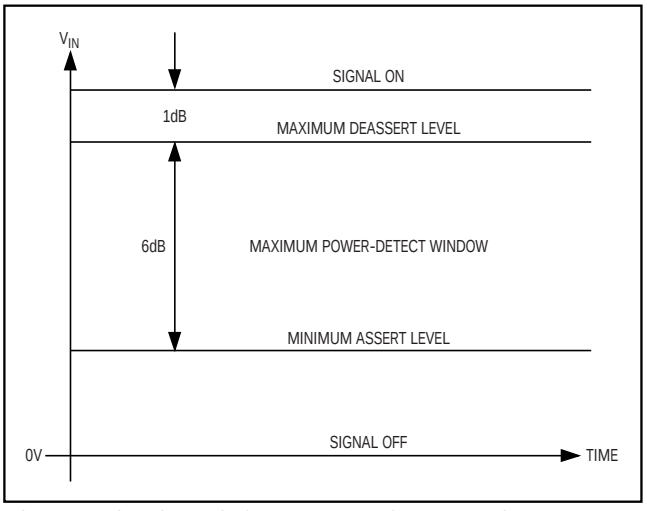


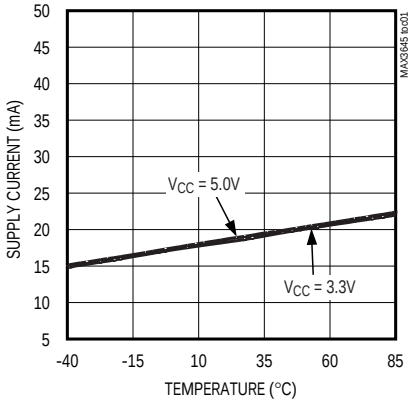

*Figure 1. Signal Levels for LOS Assert/Deassert Time Measurement*

# +2.97V to +5.5V, 125Mbps to 200Mbps Limiting Amplifier with Loss-of-Signal Detector

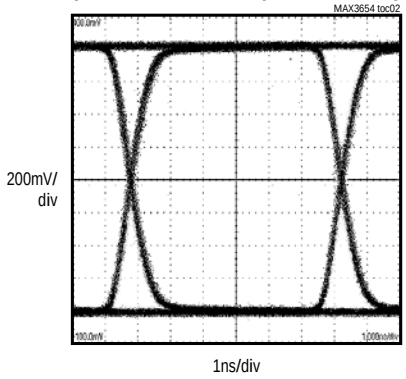
## Typical Operating Characteristics

($V_{CC}$ = 3.3V, PECL outputs terminated with 50Ω to $V_{CC}$ - 2V, $R_{TH}$ = 100Ω, $C_{AZ}$ = 0.1µF, $C_{SD}$ = 1nF, $T_A$ = +25°C, unless otherwise noted.)

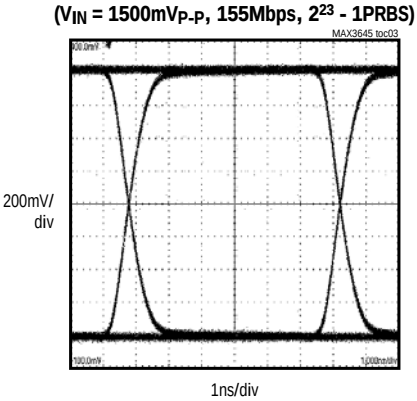
**SUPPLY CURRENT vs. TEMPERATURE (EXCLUDES PECL OUTPUT CURRENTS)**



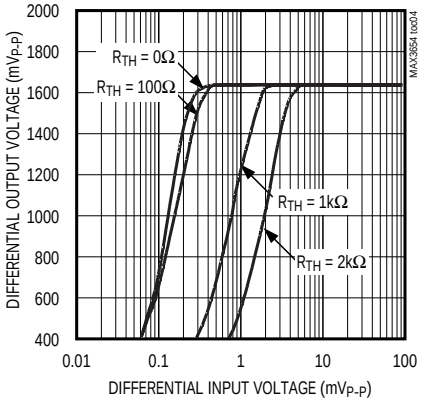

**OUTPUT EYE DIAGRAM ($V_{IN}$ = 1mV$_{P-P}$, 155Mbps, $2^{23}$ - 1PRBS)**



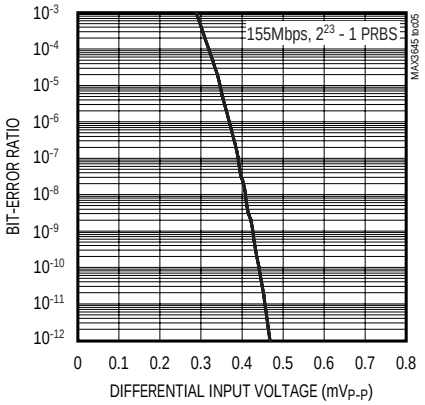

**OUTPUT EYE DIAGRAM ($V_{IN}$ = 1500mV$_{P-P}$, 155Mbps, $2^{23}$ - 1PRBS)**



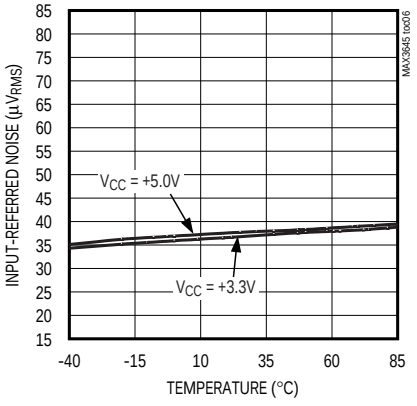

**TRANSFER FUNCTION**



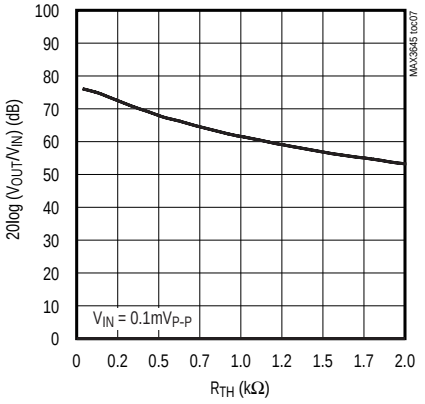

**BIT-ERROR RATIO vs. DIFFERENTIAL INPUT VOLTAGE**



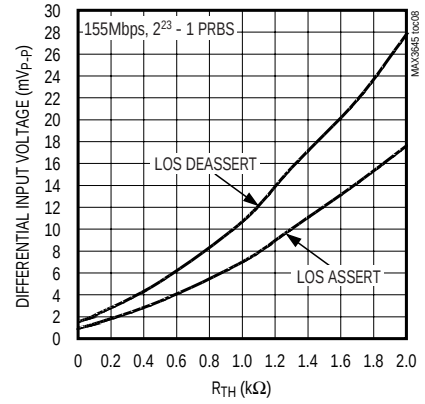

**INPUT-REFERRED RMS NOISE vs. TEMPERATURE**



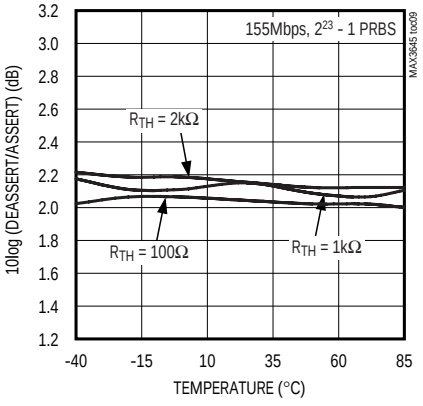

**SMALL-SIGNAL GAIN vs. $R_{TH}$**




**LOSS-OF-SIGNAL THRESHOLD vs. $R_{TH}$ ($V_{CC}$ = +3.3V AND +5.0V)**



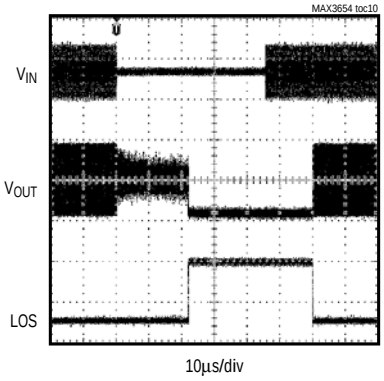

**LOSS-OF-SIGNAL HYSTERESIS vs. TEMPERATURE**



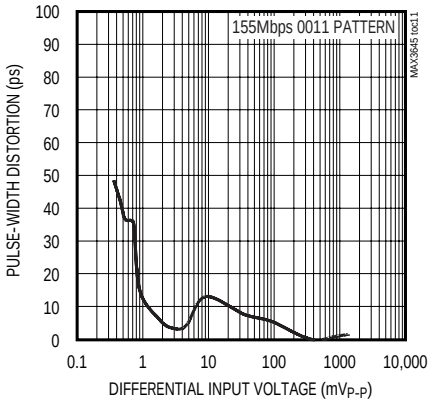
## Typical Operating Characteristics (continued)

($V_{CC}$ = 3.3V, PECL outputs terminated with 50Ω to $V_{CC}$ - 2V, $R_{TH}$ = 100Ω, $C_{AZ}$ = 0.1µF, $C_{SD}$ = 1nF, $T_A$ = +25°C, unless otherwise noted.)

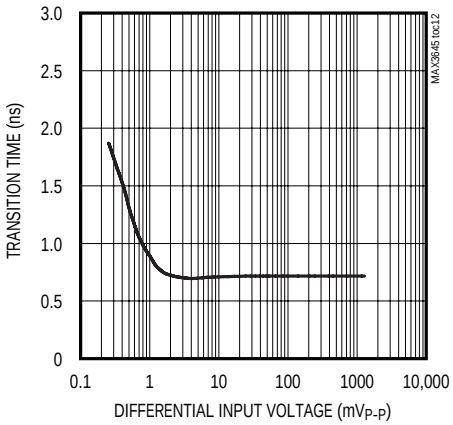
**LOSS-OF-SIGNAL WITH SQUELCH (155Mbps, $2^{23}$ - 1PRBS)**




**PULSE-WIDTH DISTORTION vs. DIFFERENTIAL INPUT VOLTAGE**




**DATA OUTPUT TRANSITION TIME vs. DIFFERENTIAL INPUT VOLTAGE**



# +2.97V to +5.5V, 125Mbps to 200Mbps Limiting Amplifier with Loss-of-Signal Detector

## Pin Description

| PIN | MINDSPEED MC2045-2 MC2045-2Y PIN NAME | MAXIM MAX3645 PIN NAME | FUNCTION |
|---|---|---|---|
| 1 | CAZ- | CAZ2 | Offset-Correction-Loop Capacitor Connection. A capacitor connected between this pin and CAZ1 sets the time constant of the offset correction loop. The offset correction is disabled when the CAZ1 and CAZ2 pins are shorted together. |
| 2 | CAZ+ | CAZ1 | Offset-Correction-Loop Capacitor Connection. A capacitor connected between this pin and CAZ2 sets the time constant of the offset correction loop. The offset correction is disabled when the CAZ2 and CAZ1 pins are shorted together. |
| 3 | GNDA | GNDA | Analog Supply Ground. Must be at the same potential as the GNDE pin. |
| 4 | $D_{IN}$ | DIN+ | Positive Data Input |
| 5 | $\overline{D_{IN}}$ | DIN- | Negative Data Input |
| 6 | $V_{CCA}$ | $V_{CCA}$ | +2.97V to +5.5V Analog Supply Voltage. Must be at same potential as the $V_{CCE}$ pin. |
| 7 | $C_F$ | CSD | Signal-Detect-Filter Capacitor Connection. Connect the $C_{SD}$ capacitor between CSD and $V_{CCA}$. |
| 8 | JAM | DIS | Disable Input, PECL or CMOS Compatible. Data outputs are held to a static logic 0 when DIS is asserted high. The LOS function remains active when the outputs are disabled. When connected to the LOS pin, an automatic squelch function is enabled. |
| 9 | $\overline{ST}$ | LOS | Positive Loss-of-Signal Output, PECL. LOS is high when the level of the input signal drops below the threshold set by the TH input. LOS is low when the signal level is above the threshold. LOS can be connected directly to DIS for automatic squelch. |
| 10 | ST | $\overline{LOS}$ | Negative Loss-of-Signal Output, PECL. $\overline{LOS}$ is low when the level of the input signal drops below the threshold set by the TH input. $\overline{LOS}$ is high when the signal level is above the threshold. |
| 11 | GNDE | GNDE | Digital Supply Ground. Must be at the same potential as the GNDA pin. |
| 12 | $\overline{D_{OUT}}$ | DOUT- | Negative Data Output, PECL. A high at DIS forces DOUT- high. |
| 13 | $D_{OUT}$ | DOUT+ | Positive Data Output, PECL. A high at DIS forces DOUT+ low. |
| 14 | $V_{CCE}$ | $V_{CCE}$ | +2.97V to +5.5V Digital Supply Voltage. Must be at the same potential as the $V_{CCA}$ pin. |
| 15 | NC | N.C. | No Connection |
| 16 | $V_{SET}$ | TH | Loss-of-Signal Threshold Pin. Resistor ($R_{TH}$) to ground sets the LOS threshold. This pin cannot be left open. |

## Detailed Description

The MAX3645 consists of gain stages, offset correction, power detector, LOS indicators, and PECL output buffers. See Figure 2 for the functional diagram.

### Data Input

The data inputs have a single-ended input resistance of 4.8kΩ and are internally DC-biased to $V_{CC}$ - 0.87V (see Figure 3). External capacitors are required to AC-couple the data signals. Pattern-dependent jitter is minimized by using coupling capacitor values large enough to pass the lowest frequencies of interest (consecutive ones and zeros) with the given input resistance.

Typically, 0.1µF coupling capacitors yield a -3dB frequency of 354Hz. Capacitor tolerance and input resistance variation (3.3kΩ to 6.4kΩ) must be considered to accurately calculate the -3dB frequency. Capacitor values should be chosen that set the -3dB frequency at least a factor of 10 below the lowest frequency of interest. A capacitor value of 0.1µF is recommended.

### Gain Stage and Offset Correction

The limiting amplifier provides approximately 74dB ($R_{TH}$ = 100Ω) of gain. This large gain makes the amplifier susceptible to small DC offsets in the signal path. To correct DC offsets, the amplifier has an internal feedback loop that acts as a DC autozero circuit. By correcting the DC offsets, the limiting amplifier improves receiver sensitivity and power-detector accuracy.

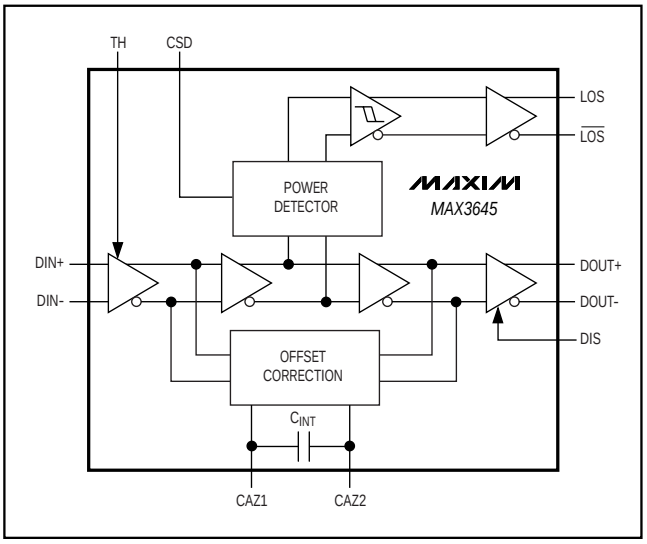



*Figure 2. Functional Diagram*

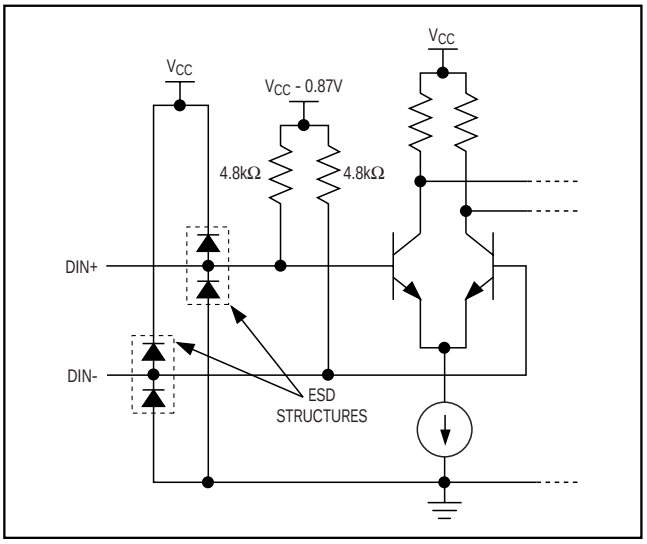



*Figure 3. Equivalent Data Input Circuit*

The external autozero capacitor ($C_{AZ}$), in parallel with internal capacitance ($C_{INT}$), determines the time constant of the DC offset correction loop. With $C_{AZ}$ = 0.1µF (recommended), the -3dB frequency cutoff of the signal path is typically 0.5kHz.

### *Power Detector and LOS Indicators*

The external resistor $R_{TH}$ sets the gain of the first limiting stage. This gain setting controls the threshold at which the power detector indicates an LOS condition. Power detection is accomplished by rectifying and lowpass filtering the data signal, then comparing it to the programmed threshold voltage. A hysteresis of 2dB prevents the LOS output from chattering when the input signal is near the threshold.

### *PECL Output Buffer*

The data outputs (DOUT+, DOUT-) and the loss-of-signal outputs (LOS+, LOS-) are PECL outputs. The equivalent PECL output circuit is shown in Figure 4.

## Applications Information

### *Programming LOS Assert/Deassert Levels*

The appropriate value of $R_{TH}$ is determined by using the Loss-Of-Signal Threshold vs. $R_{TH}$ graph in the *Typical Operating Characteristics.*

### *LOS Time Constant*

The lowpass filter of the power detector comprises a 20kΩ on-chip resistor ($R_{SD}$) and an external capacitor ($C_{SD}$). The $C_{SD}$ capacitor value determines the power-detector time constant, which determines the LOS assert/deassert time. With $C_{SD}$ = 1nF the assert/deassert time is in the range of 2.3µs to 80µs. This provides a long enough time constant to avoid false triggering due to variations in mark density.

### *Disable Function*

When the DIS input is forced high, the disable function is enabled, which holds DOUT+ low and DOUT- high. The disable function is used to prevent the data outputs from toggling due to noise when no signal is present. The LOS output can be connected to the DIS input for automatic squelch.

### *PECL Output Terminations*

The proper termination for a PECL output is 50Ω to ($V_{CC}$ - 2V), but other standard termination techniques can be used. For more information on PECL terminations and how to interface with other logic families, refer to Maxim Application Note *HFAN-01.0: Introduction to LVDS, PECL, and CML.*

### *Layout Considerations*

For best performance, use good high-frequency layout techniques. Filter power supplies, keep ground connections short, and use multiple vias where possible. Power-supply decoupling should be placed close to the $V_{CC}$ pins. Minimize the distance from the preamplifier and use controlled-impedance transmission lines to interface with the outputs when possible.

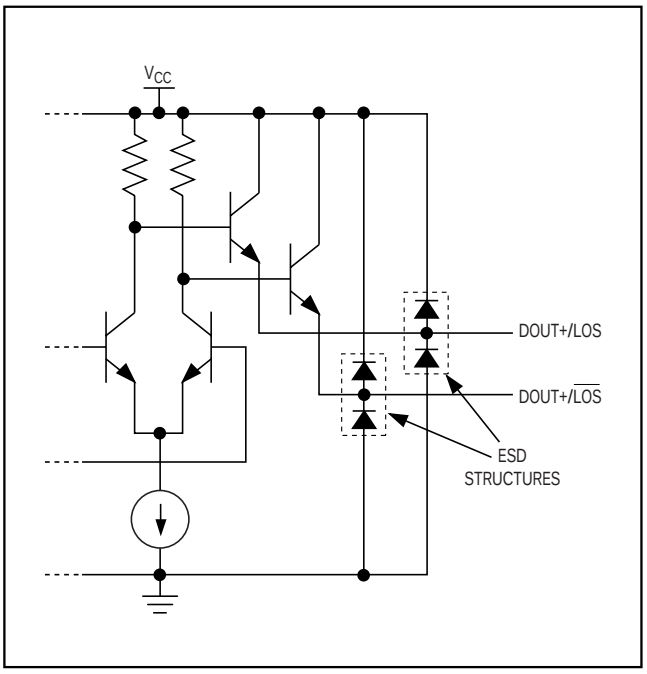



*Figure 4. Equivalent PECL Output Circuit*

## Chip Information

TRANSISTOR COUNT: 1026

PROCESS: Silicon bipolar

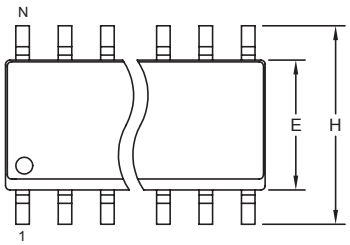
# +2.97V to +5.5V, 125Mbps to 200Mbps Limiting Amplifier with Loss-of-Signal Detector

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

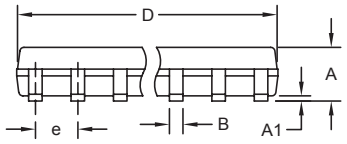
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |



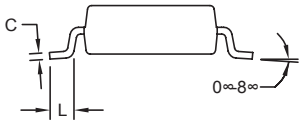

TOP VIEW

VARIATIONS:

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | N | MS012 |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

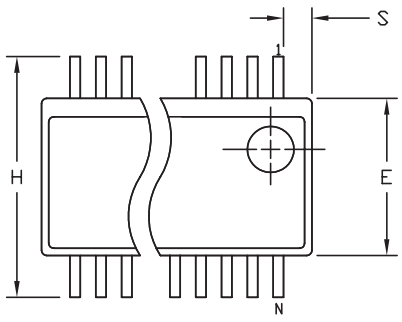
| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0041 | B | 1/1 |

# +2.97V to +5.5V, 125Mbps to 200Mbps Limiting Amplifier with Loss-of-Signal Detector

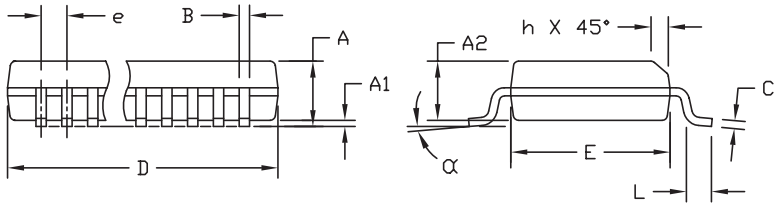
## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | .061 | .068 | 1.55 | 1.73 |
| A1 | .004 | .0098 | 0.102 | 0.249 |
| A2 | .055 | .061 | 1.40 | 1.55 |
| B | .008 | .012 | 0.20 | 0.30 |
| C | .0075 | .0098 | 0.191 | 0.249 |
| D | SEE VARIATIONS | | | |
| E | .150 | .157 | 3.81 | 3.99 |
| e | .025 BSC | | 0.635 BSC | |
| H | .230 | .244 | 5.84 | 6.20 |
| h | .010 | .016 | 0.25 | 0.41 |
| L | .016 | .035 | 0.41 | 0.89 |
| N | SEE VARIATIONS | | | |
| α | 0° | 8° | 0° | 8° |




VARIATIONS:

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | N | |
| D | .189 | .196 | 4.80 | 4.98 | 16 | AB |
| S | .0020 | .0070 | 0.05 | 0.18 | | |
| D | .337 | .344 | 8.56 | 8.74 | 20 | AD |
| S | .0500 | .0550 | 1.270 | 1.397 | | |
| D | .337 | .344 | 8.56 | 8.74 | 24 | AE |
| S | .0250 | .0300 | 0.635 | 0.762 | | |
| D | .386 | .393 | 9.80 | 9.98 | 28 | AF |
| S | .0250 | .0300 | 0.635 | 0.762 | | |

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0055 | E | 1/1 |

*Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.*



© 2004 Maxim Integrated Products Printed USA MAXIM is a registered trademark of Maxim Integrated Products.