

# SANYO Semiconductors DATA SHEET

**Bi-CMOS LSI** 

# LV5743V — 2-channel Step-down Switching Regulator

#### Overview

The LV5743V is a 2-channel step-down switching regulator.

#### **Features**

- Provides dual switching regulator control circuits integrated on the chip.
- Output-stage push-pull structure enabling high efficient operation.
- Provides power supply (V<sub>CC</sub>-5V) for protecting the external P channel MOS gate.
- Built-in timer latch type SCP (short-circuit protection circuit)
- Built-in UVLO (Low voltage malfunction prevention circuit)
- Built-in reference voltage circuit
- Max\_On\_Duty is adjustable.

#### **Specifications**

#### **Absolute Maximum Ratings** at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
Maximum supply voltage		V <sub>CC</sub> max		35	V
Output voltage		V <sub>O</sub> max		33	V
Allowable power dissipation		Pd max	Mounted on a specified board *	0.74	W
Operating temperature		Topr		-20 to +85	°C
Storage temperature		Tstg		-55 to +150	°C
Allowable pin voltage					
1	CT, NON1, NON2, INV1, INV2, FB1, FB2, DT1, DT2, SCP, VREF			7	V
2	V <sub>CC</sub> -5V			30	V
3	GND, OUT1, OUT2,			35	V

<sup>\* :</sup> Specified board : 114.3×76.1×1.6mm³, glass epoxy board

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# LV5743V

# Allowable Operating Ratings at $Ta=25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc		8 to 33	٧
Error amplifier input voltage	VIN		0 to 3.3	V
Timing capacitance	C <sub>CT</sub>		50 to 5000	pF
Oscillation frequency	FCT		20k to 1M	Hz

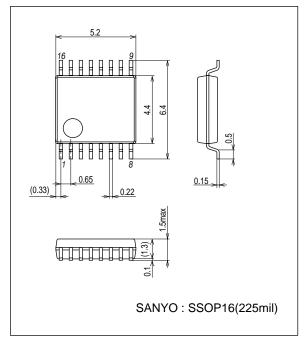
#### **Electrical Characteristics** at Ta = 25°C, $V_{CC} = 12V$

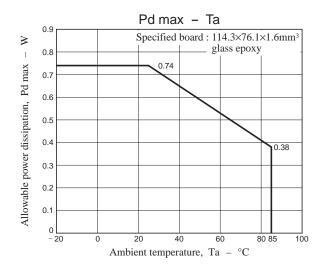
Reference voltage block         min         typ         mex           Output voltage         Vrief         Iref = 1mA         2.4948         2.520         2.5452         V           nput stability         VDLD         VCC = 8 to 33V         1         10         mV           Long Stability         VDLD         Iref = 0 to 5mA         VCC*5.         VCC*5.         VCC*6.5         VCC*4.5         V           Viney Systeph voltage         Vps         I/OUT = 5mA         VCC*5.         VCC*5.         VCC*6.5	Darameter	Cumbal	Conditions		Ratings			
Output voltage         Vrief         Iref = 1mA         2.4948         2.520         2.5452         V put put stability         VpLI         VCC = 8 to 33V         1         1         10         mV           Vight Stability         VpLI         VpC = 8 to 5mA         1         1         10         mV           Vight Strong by Voltage         Vpls         10 Upt = 5mA         VpCe-5.         VpCe-5.0         VpCe-4.5         V           Transplar wave oscillator block           Transplar wave oscillator block <th colspan<="" th=""><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>min</th><th>typ</th><th>max</th><th>Unit</th></th>	<th>Parameter</th> <th>Symbol</th> <th>Conditions</th> <th>min</th> <th>typ</th> <th>max</th> <th>Unit</th>	Parameter	Symbol	Conditions	min	typ	max	Unit
Post stability   V_DL   V_CC = 8 to 33V   1   1   10   mV	Reference voltage block							
Load stability   Vo   Tef = 0 to 5mA   1   10   mV	Output voltage	Vref	Iref = 1mA	2.4948	2.520	2.5452	V	
V <sub>INT</sub> SV supply voitage         V <sub>NS</sub> I <sub>QUT</sub> = -5mA         V <sub>CC</sub> -5.5         V <sub>CC</sub> -5.0         V <sub>CC</sub> -4.5         V           VITrianguar wave oscillator block         Trianguar wave oscillator block           Protection (ircuit block)         Tranguar wave oscillator block           Threshold voltage         V <sub>IT</sub> 1.5         1.7         1.9         V           Standby voltage         V <sub>IT</sub> 5.0         100         mV           Source current         Iscape         1.6         2.1         2.6         μA           Comparator threshold voltage         V <sub>CT</sub> 1.6         2.1         2.6         μA           Comparator threshold voltage         V <sub>CT</sub> 1.4         1.5         1.6         2.1         2.6         μA           Comparator threshold voltage         V <sub>CT</sub> 1.4         1.5         1.6         2.1         2.6         μA           Undescent time adjustment circuit block         1.5         1.7         1.9         V         1.6         2.1         2.6         μA           Upont threshold voltage         V <sub>OT</sub> Duty cycle = 0%         0.45         0.5         0.55         V           fosc = 20kHz)         V <sub>IT</sub> DT1, DT2	Input stability	$V_{DLI}$	V <sub>CC</sub> = 8 to 33V		1	10	mV	
Principal array   Property   P	Load stability	V <sub>DLO</sub>	Iref = 0 to 5mA		1	10	mV	
Scillation frequency   FOSC   CCT = 220pF   320   400   480   kHz	V <sub>IN</sub> -5V supply voltage	V <sub>N5</sub>	I <sub>OUT</sub> = -5mA	V <sub>CC</sub> -5.5	V <sub>CC</sub> -5.0	V <sub>CC</sub> -4.5	V	
Ferguency fluctuation   FDV   VCC = 8 to 33V   1	Triangular wave oscillator block		•					
Protection circuit block         ViT         1.5         1.7         1.9         V           Standby voltage         VSTB         50         100         mV           Standby voltage         VSTB         50         100         mV           Source current         ISCP         1.6         2.1         2.6         μA           Comparator threshold voltage         VCT         1.4         1.5         1.6         V           Quiescent time adjustment circuit block         ***Open protection timeshold voltage         VID         Duty cycle = 0%         0.45         0.5         0.55         V           Quiescent time adjustment circuit block         ****Open protection timeshold voltage         VID         Duty cycle = 100%         0.95         1.0         1.05         V           Plosc = 20kHz)         V100         Duty cycle = 100%         0.95         1.0         1.05         V           Plosc = 20kHz)         V100         Duty cycle = 100%         0.95         1.0         1.05         V           Low voltage malfunction prevention circuit block         Threshold voltage         VUT         6.5         7         7.5         V           Error ampliffer         Total Control of the control of the control of the control of	Oscillation frequency	Fosc	C <sub>CT</sub> = 220pF	320	400	480	kHz	
Threshold voltage	Frequency fluctuation	F <sub>DV</sub>	V <sub>CC</sub> = 8 to 33V		1		%	
Standby voltage	Protection circuit block							
Sauce current   Sace   V_LT	Threshold voltage	VIT		1.5	1.7	1.9	V	
Source current   SoCP   1.6   2.1   2.6   μA	Standby voltage	V <sub>STB</sub>			50	100	mV	
Comparator threshold voltage   VCT   1.4   1.5   1.6   V	Latch voltage				30	100	mV	
Duly cycle = 0%   0.45   0.5   0.55   V	Source current	I <sub>SCP</sub>		1.6	2.1	2.6	μА	
Duty threshold voltage   V10   Duty cycle = 0%   0.45   0.5   0.55   V     (fosc = 20kHz)   Vt100   Duty cycle = 100%   0.95   1.0   1.05   V     (fosc = 20kHz)   DT1, DT2 = 0V   0.1   1   μA     Low voltage malfunction prevention circuit block     Threshold voltage   VUT   6.5   7   7.5   V     Error amplifier	Comparator threshold voltage			1.4	1.5	1.6	V	
Total Common mode input voltage range   V_OM   V_CC = 8 to 33V   V_OM   V_CC = 8 to 33V   V_OM	Quiescent time adjustment circuit l	olock						
No.   No.	Input threshold voltage	Vt0	Duty cycle = 0%	0.45	0.5	0.55	V	
Low voltage malfunction prevention circuit block           Threshold voltage         V <sub>UT</sub> 6.5         7         7.5         V           Error amplifier         nput offset voltage         V <sub>IO</sub> 6         mV           nput offset current         I <sub>IO</sub> 30         nA           nput bias current         I <sub>IB</sub> 15         100         nA           Open gain         AV         85         dB           Common mode input voltage range         V <sub>OM</sub> V <sub>CC</sub> = 8 to 33V         0         3.3         V           Common mode rejection ratio         CMRR         80         dB         dB           Maximum output voltage         V <sub>OH</sub> 2.6         V           Minimum output voltage         V <sub>OL</sub> 0.2         0.4         V           Output sink current         I <sub>OI</sub> FB = 1.25V         1         mA           PWM comparator         10         FB = 1.25V         85         µA           PWM comparator         10         Duty cycle = 0%         0.45         0.5         0.55         V           f(scc = 20kHz)         V100         Duty cycle = 100%         0.95         1.0         1.05         V	(fosc = 20kHz)	Vt100	Duty cycle = 100%	0.95	1.0	1.05	V	
Threshold voltage	Input bias current	I <sub>BDT</sub>	DT1, DT2 = 0V		0.1	1	μА	
Common mode input voltage   Void	Low voltage malfunction prevention	n circuit block						
Note	Threshold voltage	V <sub>U</sub> T		6.5	7	7.5	V	
Note	Error amplifier							
1	Input offset voltage	V <sub>IO</sub>				6	mV	
Open gain         AV         85         dB           Common mode input voltage range         VOM         V <sub>CC</sub> = 8 to 33V         0         3.3         V           Common mode rejection ratio         CMRR         80         dB           Maximum output voltage         VOH         2.6         V           Minimum output voltage         VOL         0.2         0.4         V           Output sink current         IOI         FB = 1.25V         1         mA           Output source current         IOO         FB = 1.25V         85         μA           PWM comparator         PWM comparator         0.45         0.5         0.55         V           Input threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           Output block         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output stage on resistance (upper)         RONL         7         Ω           Overall device characteristics         2         Ω	Input offset current	IIO				30	nA	
Common mode input voltage range         VOM         VCC = 8 to 33V         0         3.3         V           Common mode rejection ratio         CMRR         80         dB           Maximum output voltage         VOH         2.6         V           Minimum output voltage         VOL         0.2         0.4         V           Output sink current         IOI         FB = 1.25V         1         mA           Output source current         IOO         FB = 1.25V         85         μA           PWM comparator         nput threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output block           Output stage on resistance (lower)         RONH         7         Ω           Overall device characteristics	Input bias current	I <sub>IB</sub>			15	100	nA	
Common mode rejection ratio         CMRR         80         dB           Maximum output voltage         VOH         2.6         V           Minimum output voltage         VOL         0.2         0.4         V           Output sink current         I OI         FB = 1.25V         1         mA           Output source current         I OO         FB = 1.25V         85         μA           PWM comparator         nput threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           (fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output block         Dutput stage on resistance (upper)         RONH         7         Ω         Ω           Overall device characteristics         Deverall device characteristics         0.25         0.2         Ω	Open gain	AV			85		dB	
Maximum output voltage         VOH         2.6         V           Winimum output voltage         VOL         0.2         0.4         V           Output sink current         IOI         FB = 1.25V         1         mA           Output source current         IOO         FB = 1.25V         85         μA           PWM comparator         nput threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           (fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output block         Output stage on resistance (upper)         RONH         7         Ω         Ω           Output stage on resistance (lower)         RONL         2         Ω           Overall device characteristics	Common mode input voltage range	VOM	V <sub>CC</sub> = 8 to 33V	0		3.3	V	
Minimum output voltage $V_{OL}$ 0.2 0.4 V Output sink current $I_{OI}$ FB = 1.25V 1 1 mA Output source current $I_{OO}$ FB = 1.25V 85 $\mu$ A  PWM comparator Input threshold voltage Vt0 Duty cycle = 0% 0.45 0.5 0.55 V Input threshold voltage Vt100 Duty cycle = 100% 0.95 1.0 1.05 V  Output block Output stage on resistance (upper) RONH 7 $\Omega$ Output stage on resistance (lower) RONL 0 $\Omega$ Overall device characteristics	Common mode rejection ratio	CMRR			80		dB	
Output sink current     IQI     FB = 1.25V     1     mA       Output source current     IQO     FB = 1.25V     85     μA       PWM comparator       Input threshold voltage     Vt0     Duty cycle = 0%     0.45     0.5     0.55     V       Vfosc = 20kHz)     Vt100     Duty cycle = 100%     0.95     1.0     1.05     V       Output block       Output stage on resistance (upper)     RONH     7     Ω       Output stage on resistance (lower)     RONL     2     Ω       Overall device characteristics	Maximum output voltage	VOH			2.6		V	
Output source current         I <sub>OO</sub> FB = 1.25V         85         μA           PWM comparator           Input threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           (fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output block           Dutput stage on resistance (upper)         RONH         7         Ω           Dutput stage on resistance (lower)         RONL         2         Ω           Overall device characteristics	Minimum output voltage	V <sub>OL</sub>			0.2	0.4	V	
PWM comparator           Input threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           (fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Dutput block           Dutput stage on resistance (upper)         RONH         7         Ω           Dutput stage on resistance (lower)         RONL         2         Ω           Description of the color	Output sink current	IOI	FB = 1.25V		1		mA	
Note	Output source current	100	FB = 1.25V		85		μΑ	
Output block         Output stage on resistance (upper)         R <sub>ONH</sub> 7         Ω           Output stage on resistance (lower)         R <sub>ONL</sub> 2         Ω           Overall device characteristics         2         Ω	PWM comparator							
Output block       Output stage on resistance (upper)     R <sub>ONH</sub> 7     Ω       Output stage on resistance (lower)     R <sub>ONL</sub> 2     Ω       Overall device characteristics	Input threshold voltage	Vt0	Duty cycle = 0%	0.45	0.5	0.55	V	
Output stage on resistance (upper)     R <sub>ONH</sub> 7     Ω       Output stage on resistance (lower)     R <sub>ONL</sub> 2     Ω       Overall device characteristics	(fosc = 20kHz)	Vt100	Duty cycle = 100%	0.95	1.0	1.05	V	
Output stage on resistance (lower) R <sub>ONL</sub> 2 Ω  Overall device characteristics	Output block							
Overall device characteristics	Output stage on resistance (upper)	RONH			7		Ω	
	Output stage on resistance (lower)	R <sub>ONL</sub>			2		Ω	
Standby current I <sub>CCS</sub> When output is off 5 mA	Overall device characteristics							
	Standby current	l <sub>ccs</sub>	When output is off			5	mA	

# **Package Dimensions**

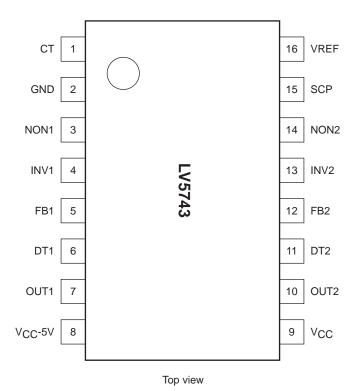
unit: mm (typ)







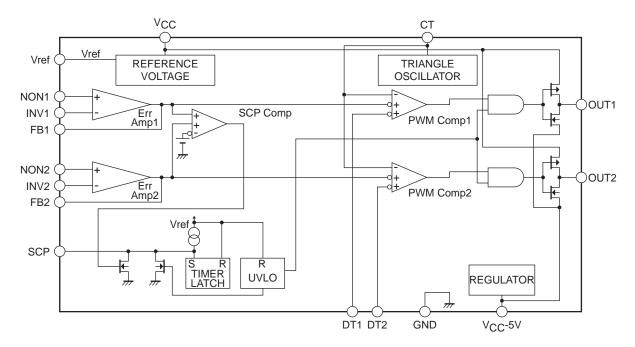
# **Pin Assignment**



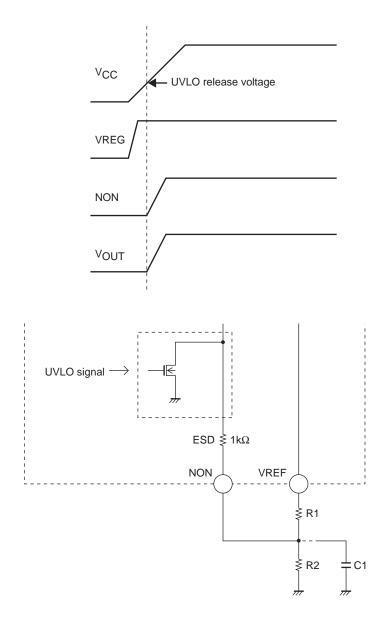
#### **Pin Function**

Pin No.	Pin Name	Description	
1	СТ	External timing capacitor connection pin	
2	GND	Ground	
3	NON1	Error amplifier 1 input (+)	
4	INV1	Error amplifier 1 input (-)	
5	FB1	Error amplifier 1 output	
6	DT1	Output 1 maximum duty setting	
7	OUT1	Output 1	
8	V <sub>CC</sub> -5V	Power supply for output stage drive	
9	V <sub>CC</sub>	Power supply	
10	OUT2	Output 2	
11	DT2	Output 2 maximum duty setting	
12	FB2	Error amplifier 2 input (+)	
13	INV2	Error amplifier 2 input (-)	
14	NON2	Error amplifier 2 output	
15	SCP	Timer latch setting	
16	VREF	Reference voltage output	

# **Block Diagram**

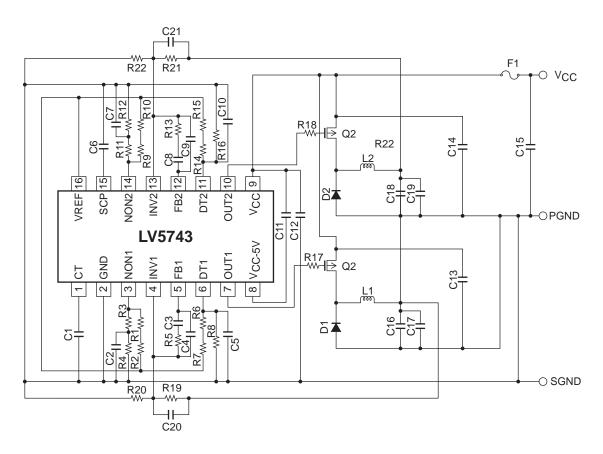


#### **Timing Chart**



<sup>\*</sup> The voltage at the NON pin is  $\{VREF/(R1+1k)\}\times 1k$  in UVLO mode.

#### Sample Application Circuit Diagram



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