1A, Low Noise, Ultra High PSRR, Low-Dropout Linear Regulator

General Description

The RT2519W is a high performance positive low dropout (LDO) regulator designed for applications requiring very low dropout voltage and ultra high Power Supply Ripple Rejection (PSRR) at up to 1A. The input voltage range is from 2.2V to 6V and the output voltage is programmable as low as 0.8V. A P-MOSFET switch provides excellent transient response with just a 4.7µF ceramic output capacitor. The external enable control effectively reduces power dissipation while shutdown and further output noise immunity is achieved through bypass capacitor on NR pin. Additionally, the RT2519W features a precise 3% output regulation over line, load, and temperature variations. The device is available in the VDFN-8AL 3x3 package and is specified from –40°C to 125°C.

Features

- **Very Low Dropout : 170mV Typical at 1A**
- **Ultra High PSRR : 63dB @ 1kHz, 38dB @ 1MHz**
- **Input Voltage Range : 2.2V to 6V**
- **Adjustable Output Voltage : 0.8V to 5.5V**
- **–40°C to 125°C Operating Junction Temperature Range**
- **Excellent Noise Immunity**
- **Fast Response Over Load and Line Transient**
- **Stable with a 4.7µF Output Ceramic Capacitor**
- **Accurate Output Voltage 3% Over Load, Line, Process, and Temperature Variations**
- **Enable Control**
- **Over-Current Protection**
- **Over-Temperature Protection**

Ordering Information

RT2519W □□□

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  QV : VDFN-8AL 3x3 (V-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

***Empty means Pin1 orientation is Quadrant 1

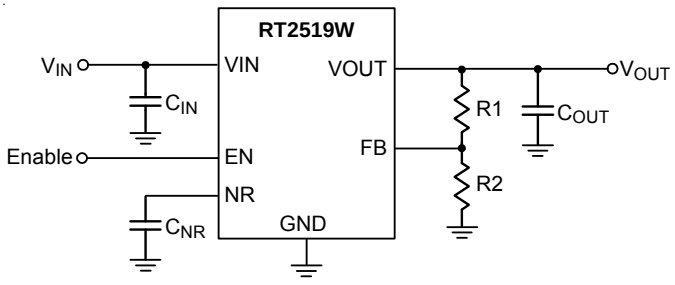
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Applications

- Telecom/Networking Cards
- Motherboards/Peripheral Cards
- Industrial Applications
- Wireless Infrastructures
- Set-Top Boxes
- Medical Equipments
- Notebook Computers
- Battery Powered Systems

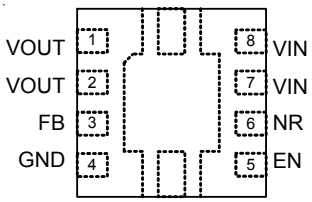
Simplified Application Circuit



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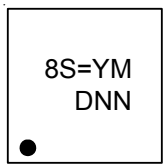
Pin Configuration

(TOP VIEW)



VDFN-8AL 3x3

Marking Information



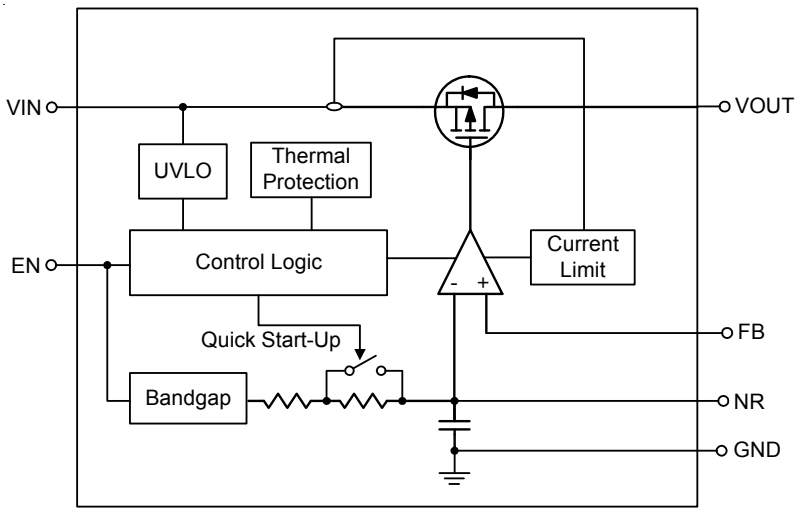
8S= : Product Code

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	VOUT	Output of the regulator. Decouple this pin to GND with at least 4.7μF for stability.
3	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.8V typically.
4	GND	System ground.
5	EN	Enable control input. Connecting this pin to logic high enables the regulator or driving this pin low puts it into shutdown mode. EN can be connected to IN if not used. (EN pin is not allowed to be left floating.)
6	NR	Noise reduction input. Decouple this pin to GND with an external capacitor can not only reduce output noise to very low levels but also slow down the VOUT rise like a soft-start behavior.
7, 8	VIN	Supply input. A minimum of 1μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.

Functional Block Diagram



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Operation

The RT2519W is a low noise, high PSRR LDO which supports very low dropout operation. The operating input range from 2.2V to 6V and the output voltage is programmable as low to 0.8V and the output current can be up to 1A. The internal compensation network is well designed to achieve fast transient response with good stability.

In steady-state operation, the feedback voltage is regulated to the reference voltage by the internal regulator. When the feedback voltage signal is less than the reference, the output current passes through the power MOSFET will be increased. The extra amount of the current is sent to the output until the voltage level of FB pin returns to the reference.

On the other hand, if the feedback voltage is higher than the reference, the power MOSFET current is decreased. The excess charge at the output can be released by the loading current.

Start-Up

The RT2519W has a quick-start circuit to charge the noise reduction capacitor (C_{NR}). The switch of the quick-start circuit is closed at start up.

To reduce the noise from bandgap, there is a low-pass (RC) filter consist of the C_{NR} and the resistance which is connected with bandgap, as Functional Block Diagrams present.

At the start-up, the quick-start switch is closed, with only 35kΩ resistance between bandgap and NR pin. The quick-start switch opens approximate 2ms after the device is enabled, the resistance between NR and bandgap is about 224kΩ to form a very good low pass filter and with great noise reduction performance.

The 35kΩ resistance is used to slow down the reference voltage ramp to avoid inrush current at chip start-up, and the start-up time can be calculated as :

$$t_{SS}\,(sec) = 160000 \times C_{NR}\,(F) \quad (1)$$

It is recommend the C_{NR} value larger than 0.01μF to reduce noise, and low leakage ceramic capacitors are suitable. However, with too large C_{NR} will extend the start-up time very long if the C_{NR} is not fully charged during 2ms and opens the quick-start switch, the C_{NR} will be charged through higher resistance 224kΩ and takes much longer time to finish the start up process.

Enable and Shutdown Operation

The RT2519W goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and bandgap are all turned off, reducing the supply current to only 2μA (max.). If the shutdown mode is not required, the EN pin can be directly tied to VIN pin to keep the LDO on.

Current Limit

The RT2519W continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range. By reason of the build-in body diode, the pass transistor conducts current when the output voltage exceeds input voltage. Since the current is not limited, external current protection should be added if device may work at reverse voltage state.

Over-Temperature Protection (OTP)

The RT2519W has an over-temperature protection. When the device triggers the OTP, the device shuts down until the temperature back to normal state.

Under Voltage Lock-Out (UVLO)

The RT2519W utilizes an under voltage lock-out circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 30μs duration.

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Absolute Maximum Ratings (Note 1)

- All Pins ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  VDFN-8AL 3x3 ---------- 3.31W
- Package Thermal Resistance (Note 2)
  VDFN-8AL 3x3, θ_{JA} ---------- 30.2°C/W
  VDFN-8AL 3x3, θ_{JC} ---------- 5.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 2.2V to 6V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 0.5V or 2.2V, V_{OUT} = 0.8V and 5.5V, I_{OUT} = 1mA, V_{EN} = 2.2V, C_{NR} = 10nF, C_{OUT} = 4.7µF, T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Operating Voltage	V_{IN}		2.2	--	6	V
Under-Voltage Lockout Threshold	V_{UVLO}	R_{OUT} = 1kΩ	1.86	2	2.1	V
Under-Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}	R_{OUT} = 1kΩ	--	200	--	mV
Shutdown Current	I_{SHDN}	$V_{EN} \le 0.4V$, $V_{IN} \ge 2.2V$, R_{OUT} = 1kΩ, 0°C ≤ T_J ≤ 85°C	--	0.2	2	µA
Quiescent Current	I_Q		--	190	350	µA
Output Voltage						
Output Supply Voltage	V_{OUT}		0.8	--	5.5	V
Output Supply Voltage Accuracy (Note 5)		V_{OUT} + 0.5V ≤ V_{IN} ≤ 6V, V_{IN} ≥ 2.5V, 100mA ≤ I_{OUT} ≤ 500mA, 0°C ≤ T_J ≤ 85°C	–2	--	+2	%
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 6V, V_{IN} ≥ 2.2V, 100mA ≤ I_{OUT} ≤ 1A	–3	±0.3	+3	
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} + 0.5V ≤ V_{IN} ≤ 6V, V_{IN} ≥ 2.2V, I_{OUT} = 100mA	--	0.2	--	%
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	100mA ≤ I_{OUT} ≤ 1A	--	0.3	--	%

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Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Enable Voltage							
Enable Threshold Voltage	V_{IH}	V_{EN} rising	2.2V ≤ V_{IN} ≤ 6V, R_{OUT} = 1kΩ	1.2	--	--	V
	V_{IL}	V_{EN} falling, R_{OUT} = 1kΩ		--	--	0.4	
Enable Input Current	I_{IH}	V_{IN} = 6V, V_{EN} = 6V		--	0.02	1	μA
Feedback Input Current	I_{FB}	V_{IN} = 5.5V, V_{FB} = 0.8V		--	0.02	1	μA
Current Limit							
Output Current Limit	I_{LIM}	V_{IN} = 3.3V, V_{OUT} = 0.85 x V_{OUT}		1.1	1.4	2	A
Power-Up Time							
Power-Up Time		V_{OUT} = 3.3V, R_{OUT} = 3.3kΩ, C_{OUT} = 4.7μF	C_{NR} = 1nF	--	0.16	--	ms
			C_{NR} = 10nF	--	1.6	--	
Dropout Voltage							
Dropout Voltage	V_{DROP}	V_{OUT} + 0.5V ≤ V_{IN} ≤ 6V, V_{FB} = 0V	V_{IN} ≥ 2.2V, I_{OUT} = 500mA	--	--	160	mV
			V_{IN} ≥ 2.5V, I_{OUT} = 750mA	--	--	210	
			V_{IN} ≥ 2.5V, I_{OUT} = 1A	--	--	370	
Power Supply Ripple Rejection and Noise							
Power Supply Ripple Rejection	PSRR	V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 750mA	f = 100Hz	--	48	--	dB
			f = 1kHz	--	63	--	
			f = 10kHz	--	63	--	
			f = 1MHz	--	38	--	
Output Noise Voltage		BW = 100Hz to 100kHz, V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 100mA	C_{NR} = 1nF	--	15.6 x V_{OUT}	--	μV_{RMS}
			C_{NR} = 10nF	--	15.6 x V_{OUT}	--	
			C_{NR} = 0.1μF	--	15.1 x V_{OUT}	--	
Over-Temperature Protection							
Thermal Shutdown	T_{SD}			--	160	--	°C
Thermal Shutdown Recovery				--	140	--	

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Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

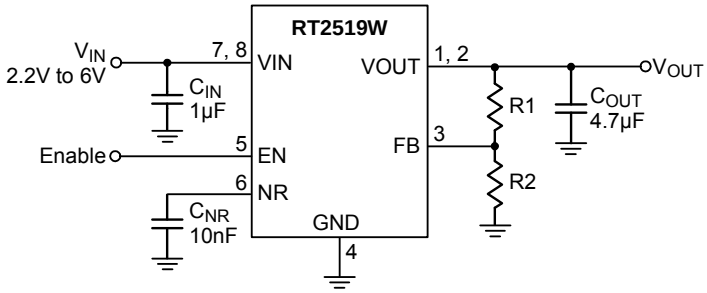
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The spec. doesn't cover the tolerances from external resistors, and which is not tested at condition of V_{OUT} = 0.8V, 4.5V ≤ V_{IN} ≤ 6V, and 750mA ≤ I_{OUT} ≤ 1A since the power dissipation of the device is totally higher than the maximum rating of the package to lead a thermal shutdown issue.

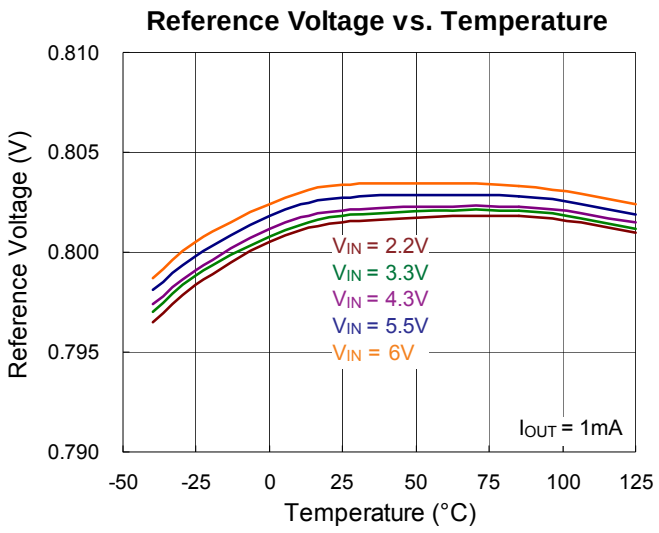
Typical Application Circuit

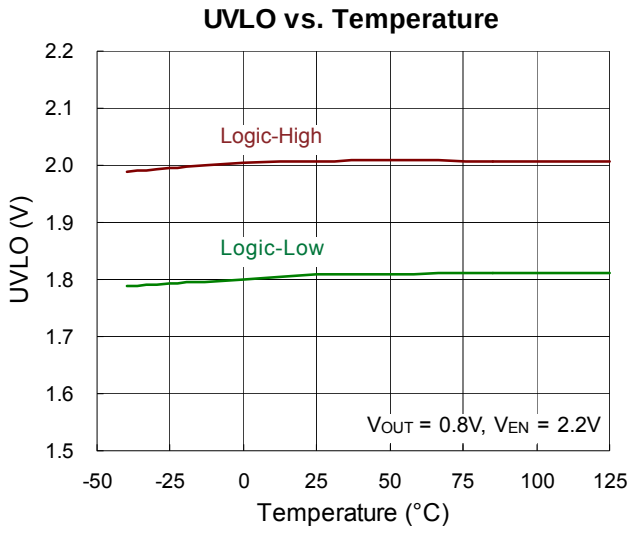


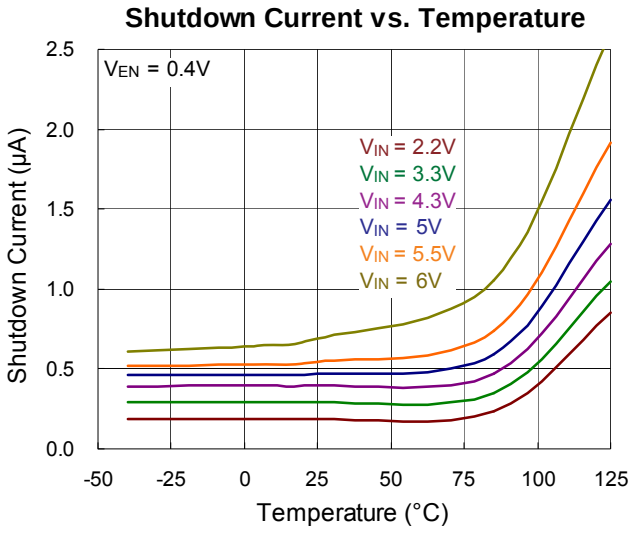
Note : All input and output capacitance in the suggested parameter mean the effective capacitance. The effective capacitance needs to consider any De-rating Effect like DC bias.

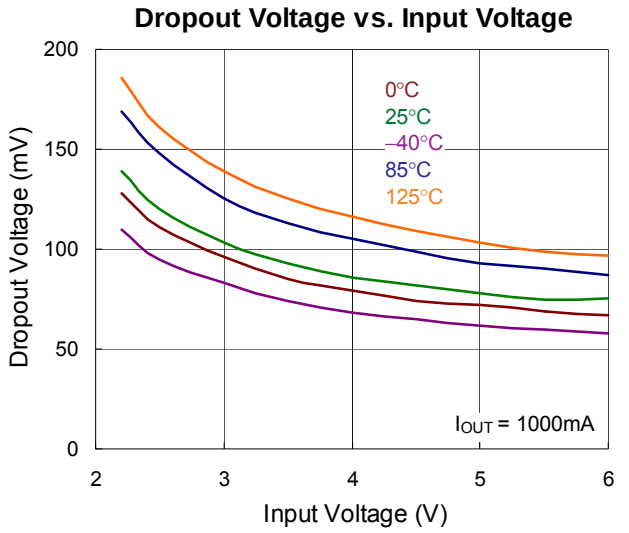
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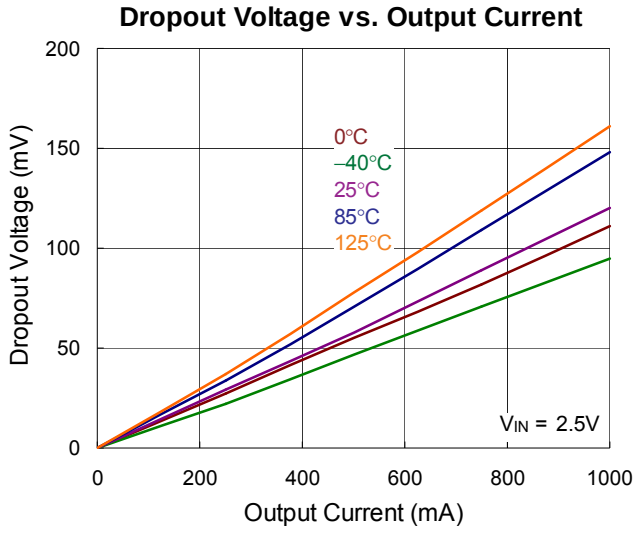
Typical Operating Characteristics

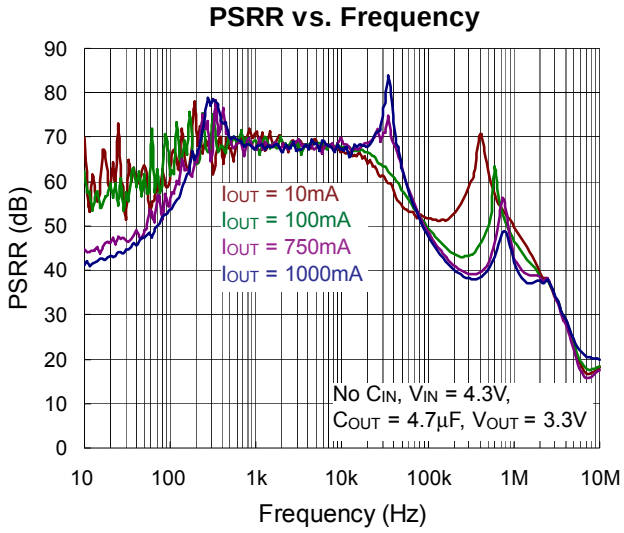






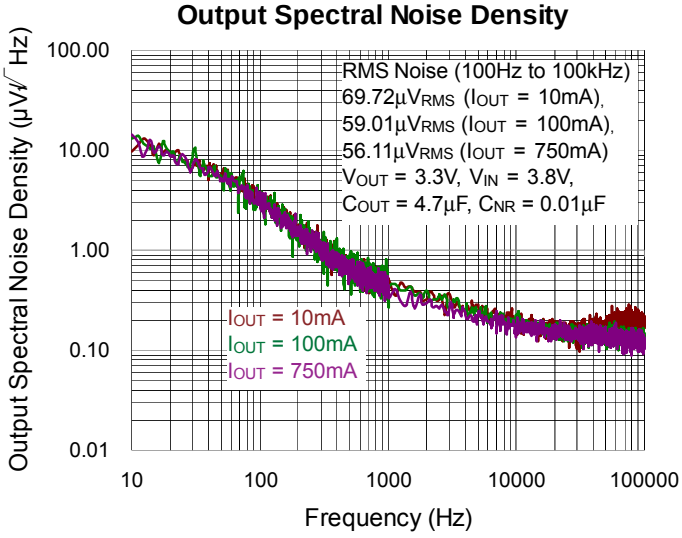




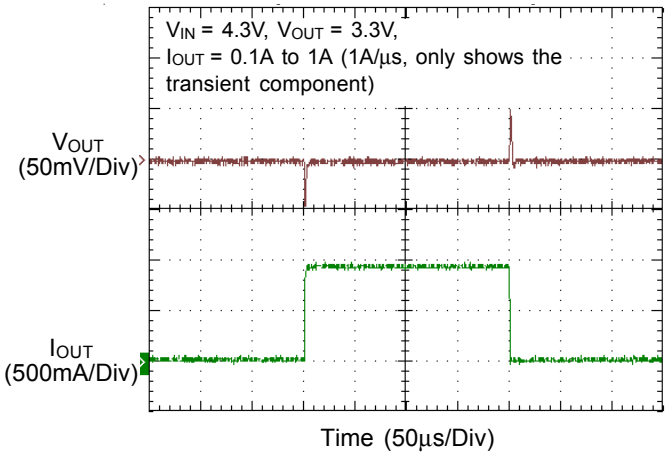


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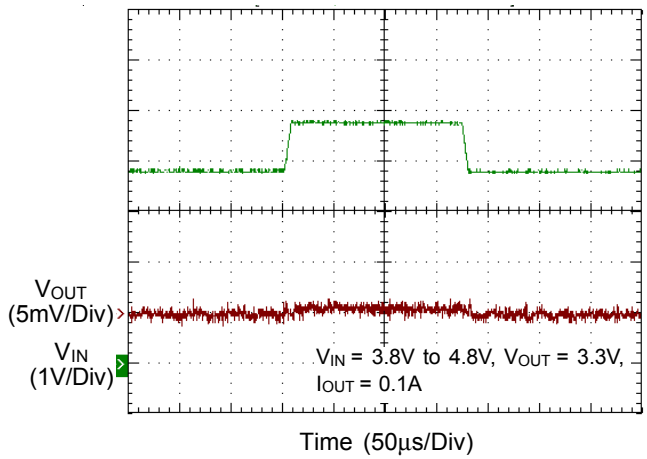
Output Spectral Noise Density



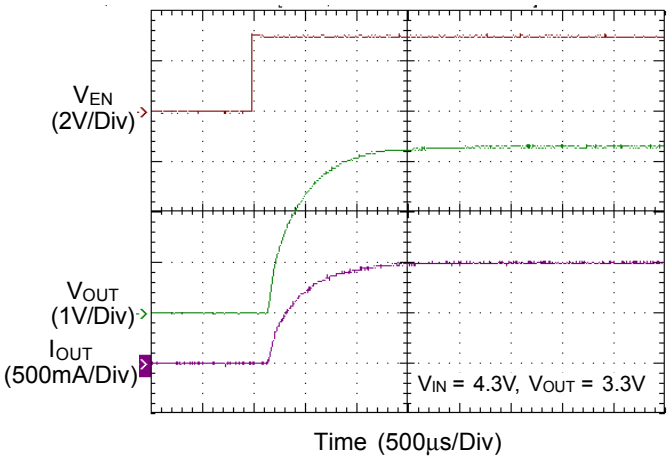
Load Transient Response



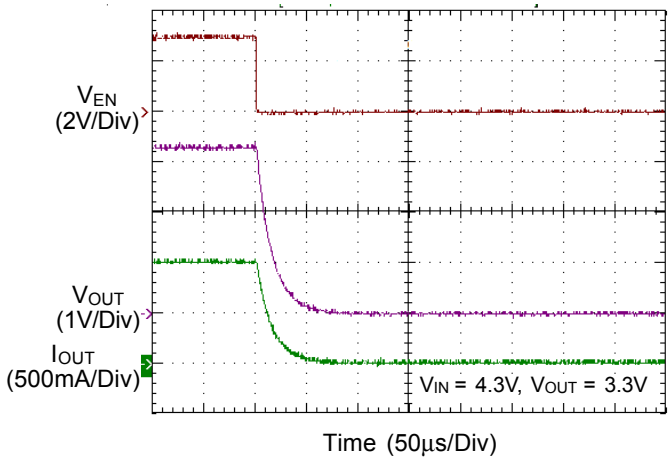
Line Transient Response



Power On from EN



Power Off from EN



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Application Information

The RT2519W is a low voltage, low dropout linear regulator with input voltage from 2.2V to 6V and a fixed output voltage from 0.8V to 5.5V.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DO} also can be expressed as the voltage drop on the pass-FET at specific output current(I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as ($V_{DO} = V_{VIN} - V_{VOUT} = R_{DS(ON)} \times I_{RATED}$).

For normal operation, the suggested LDO operating range is ($V_{VIN} > V_{VOUT} + V_{DO}$) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade these performance severely.

Output Voltage Setting

For the RT2519W, the voltage on the FB pin sets the output voltage and is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the formula given in Equation :

$$V_{OUT} = \frac{(R1 + R2)}{R2} \times 0.8$$

Using lower values for R1 and R2 is recommended to reduces the noise injected from the FB pin. Note that R1 is connected from VOUT pin to FB pin, and R2 is connected from FB to GND.

Chip Enable Operation

The EN pin is the chip enable input. Pull the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT2519W quiescent current drops to lower than 2μA. Drive the EN pin to high (>1.2V, <6V) will turn on the device again. For external timing control (e.g.RC),the EN pin can also be externally pulled to High by adding a 100kΩ or greater resistor from the VIN pin.

Current Limit

The RT2519W continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range. By reason of the build-in body diode, the pass transistor conducts current when the output voltage exceeds input voltage. Since the current is not limited, external current protection should be added if device may work at reverse voltage state.

C_{IN} and C_{OUT} Selection

Like any low dropout regulator, the external capacitors of the RT2519W must be carefully selected for regulator stability and performance. Using a capacitor of at least 4.7μF is suitable. The input capacitor must be located at a distance of no more than 0.5 inch from the input pin of the chip. Any good quality ceramic capacitor can be used. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response.

The RT2519W is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with capacitance of at least 4.7μF on the RT2519W output ensures stability.

Output Noise

Generally speaking, the dominant noise source is from the internal bandgap for most LDOs. With the noise reduction capacitor connecting to the NR pin of the RT2519W, the noise component contributed from bandgap will not be significantly. Instead, the most noise source comes from the output resistor divider and the error amplifier input. For general application to minimize noise, using a 0.01μF noise-reduction capacitor (C_{NR}) is recommended.

Thermal Considerations

Thermal protection limits power dissipation in the RT2519W. When the operation junction temperature exceeds 160°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools down by 20°C.

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The RT2519W output voltage will be closed to zero when output short circuit occurs as shown in Figure 1. It can reduce the chip temperature and provides maximum safety to end users when output short circuit occurs.

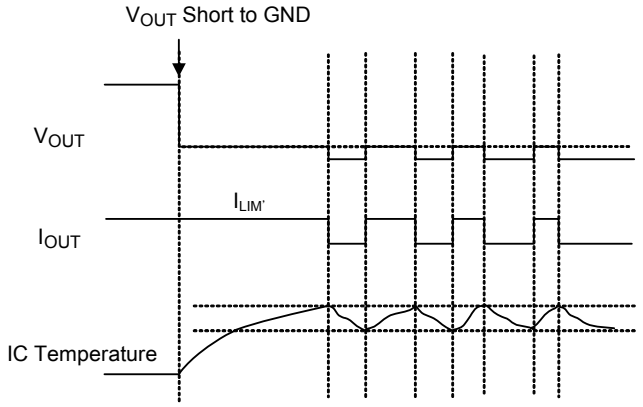


Figure 1. Short-Circuit Protection when Output Short-Circuit Occurs

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VDFN-8AL 3x3 package, the thermal resistance, θ_{JA}, is 30.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (30.2°C/W) = 3.31W for a VDFN-8AL 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

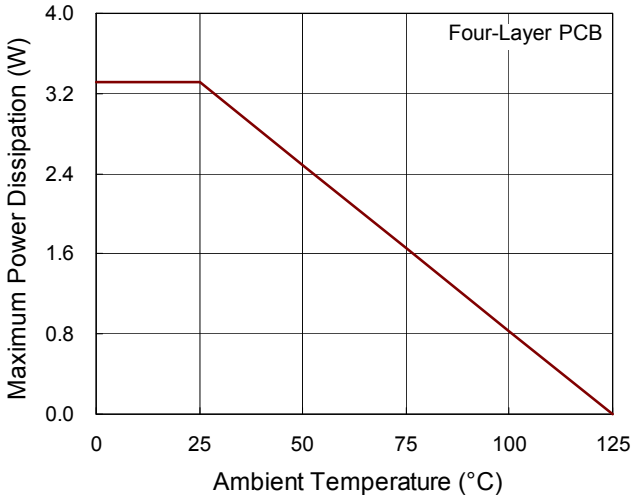


Figure 2. Derating Curve of Maximum Power Dissipation

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Layout Consideration

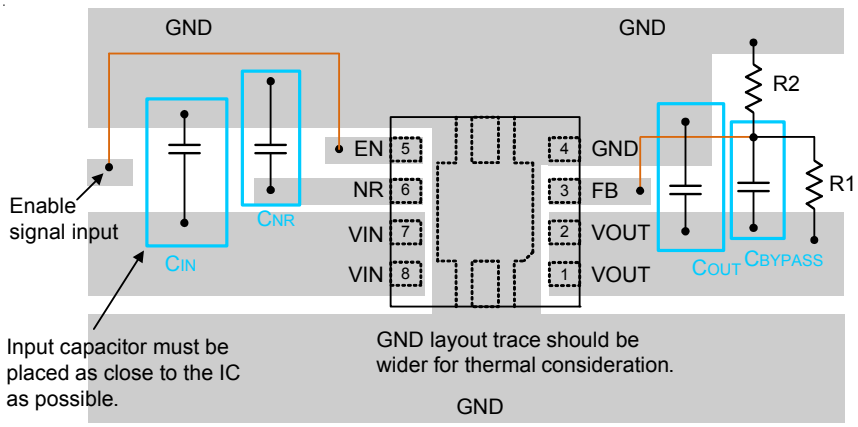
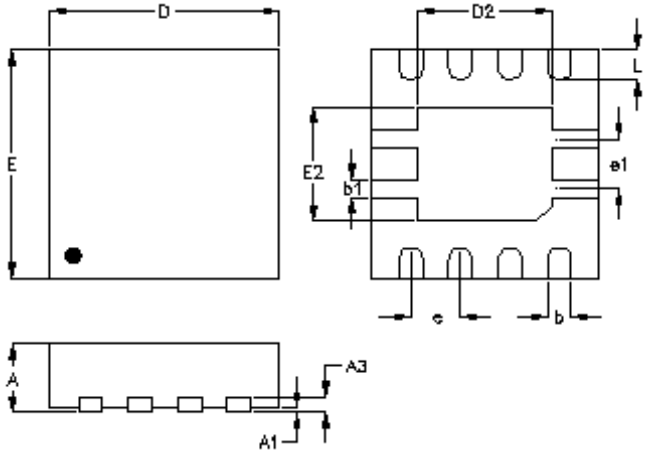
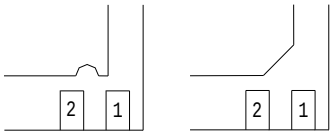


Figure 3. PCB Layout Guide

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Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

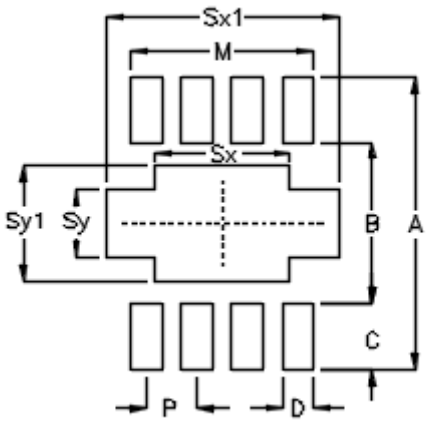
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.370	0.010	0.015
b1	0.230		0.009	
D	2.900	3.100	0.114	0.122
D2	1.700	1.800	0.067	0.071
E	2.900	3.100	0.114	0.122
E2	1.450	1.550	0.057	0.061
e	0.650		0.026	
e1	0.650		0.026	
L	0.350	0.450	0.014	0.018

V-Type 8AL DFN 3x3 Package

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Footprint Information



Package	Number of Pin	Footprint Dimension (mm)										Tolerance
		P	A	B	C	D	Sx	Sx1	Sy	Sy1	M	
V/W/U/XDFN3*3-8A	8	0.65	3.80	2.10	0.85	0.40	1.75	3.00	0.88	1.50	2.35	±0.05

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