

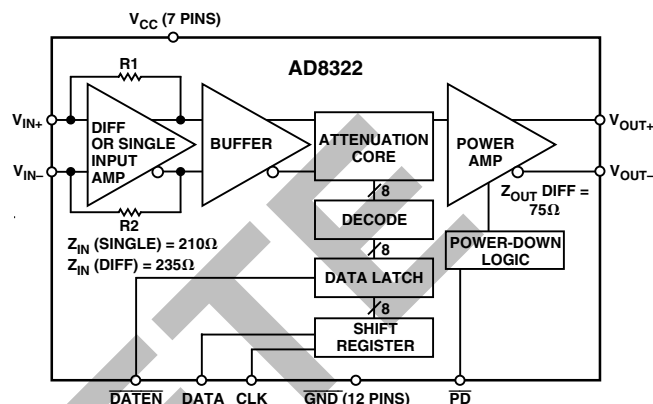
FEATURES

- Supports DOCSIS Standard for Reverse Path Transmission
- Gain Programmable in 6 dB Steps Over a 42 dB Range
- Low Distortion at 60 dBmV Output
 - 58 dBc SFDR at 21 MHz
 - 56 dBc SFDR at 42 MHz
- Output Noise Level
 - 46 dBmV in 160 kHz Bandwidth
- Maintains 75 Ω Output Impedance
- Power-Up and Power-Down Condition
- 180 MHz Bandwidth
- 5 V Supply Operation
- Supports SPI Interfaces

APPLICATIONS

- Gain Programmable Line Driver
- DOCSIS-Compliant Data Modems
- Interactive Set-Top Boxes
- PC Plug-in Modems
- General-Purpose Digitally Controlled Variable Gain Block

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8322 is a low-cost, digitally controlled variable gain amplifier optimized for coaxial line driving applications such as cable modems that are designed to the MCNS-DOCSIS upstream standard. An 8-bit serial word determines the desired output gain over a 42.14 dB range, with gain steps of 6.02 dB/major carry.

The AD8322 comprises a digitally controlled variable attenuator of 0 dB to -42.14 dB, which is preceded by a low-noise, fixed-gain buffer and is followed by a low-distortion, high-power amplifier. The AD8322 accepts a differential or single-ended input signal. The output is specified for driving a 75 Ω load, such as coaxial cable.

Distortion performance of -58 dBc is achieved with an output level up to 60 dBmV at 21 MHz bandwidth. A key performance and cost advantage of the AD8322 results from the ability to maintain a constant 75 Ω output impedance during power-up and power-down conditions. This eliminates the need for external 75 Ω termination resulting in twice the effective output voltage when compared to a standard operational amplifier.

The AD8322 is packaged in a low-cost 28-lead TSSOP, operates from a single 5 V supply, and has an operational temperature range of -40°C to +85°C.

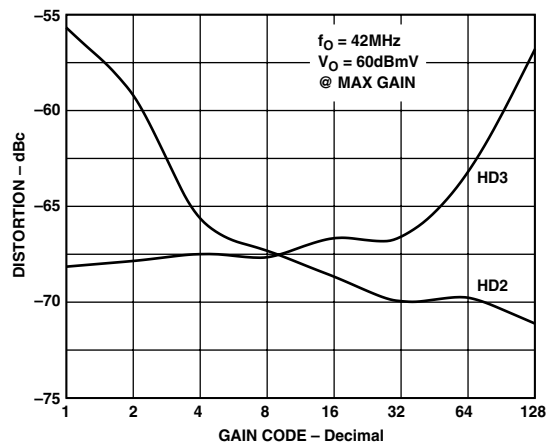


Figure 1. Harmonic Distortion vs. Gain Control

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AD8322—SPECIFICATIONS ($T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = R_{IN} = 75\ \Omega$, $V_{IN} = 92\text{ mV p-p differential}$, V_{OUT} measured through a 1:1 transformer¹ with insertion loss of 0.5 dB @ 10 MHz unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Specified AC Voltage	$P_{OUT} = 60\text{ dBmV}$, Max Gain		92		mV p-p
Noise Figure	Max Gain, $f = 10\text{ MHz}$		11.8		dB
Input Resistance	Single-Ended Input		210		Ω
	Differential Input		235		Ω
Input Capacitance			2		pF
GAIN CONTROL INTERFACE					
Gain Range		41.0	42.14	43.2	dB
Maximum Gain	Gain Code = 1xxxxxxx	27.5	29.5	31.5	dB
Minimum Gain	Gain Code = 00000001	-14.64	-12.64	-10.64	dB
Gain Scaling Factor			6.02		dB/Major Carry
OUTPUT CHARACTERISTICS					
Bandwidth (-3 dB)	All Gain Codes		180		MHz
Bandwidth Roll-Off	$f = 65\text{ MHz}$		0.25		dB
Bandwidth Peaking	$f = 65\text{ MHz}$		0.05		dB
Output Noise	Max Gain, $f = 10\text{ MHz}$		-32		dBmV in 160 kHz BW
	Min Gain, $f = 10\text{ MHz}$		-46		dBmV in 160 kHz BW
	Power-Down Mode, $f = 10\text{ MHz}$		-68		dBmV in 160 kHz BW
1 dB Compression Point	Max Gain, $f = 10\text{ MHz}$		19		dBm
Differential Output Impedance	Power-Up and Power-Down		$75 \pm 20\%$		Ω
OVERALL PERFORMANCE					
Second Order Harmonic Distortion ²	$f = 5\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-64		dBc
	$f = 14\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-60		dBc
	$f = 21\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-58		dBc
	$f = 32\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-57		dBc
	$f = 42\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-56		dBc
	$f = 65\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-52		dBc
Third Order Harmonic Distortion	$f = 5\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-67		dBc
	$f = 14\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-64		dBc
	$f = 21\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-61		dBc
	$f = 32\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-58		dBc
	$f = 42\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-56		dBc
	$f = 65\text{ MHz}$, $P_{OUT} = 60\text{ dBmV @ Max Gain}$		-53		dBc
Gain Linearity Error	$f = 10\text{ MHz}$, Code to Code		± 0.2		dB
Output Settling to 1 mV					
Due to Gain Change	Min to Max Gain		60		ns
Due to Input Change	Max Gain, $V_{IN} = 0\text{ V}$ to 0.09 V p-p		30		ns
Signal Feedthrough	Max Gain, Power-Down, $f = 42\text{ MHz}$, $V_{IN} = 0.09\text{ V p-p}$		-24		dBc
POWER CONTROL					
Power-Up Settling Time to 1 mV	Max Gain, $V_{IN} = 0$		300		ns
Power-Down Settling Time to 1 mV	Max Gain, $V_{IN} = 0$		40		ns
Between Burst Transients ³	Equivalent $P_{OUT} = 17.6$ to 35.67 dBmV		3		mV p-p
	Equivalent $P_{OUT} = 60\text{ dBmV}$		16		mV p-p
POWER SUPPLY					
Operating Range		4.75	5	5.25	V
Quiescent Current	Power-Up Mode	100	113	126	mA
	Power-Down Mode	44	54	60	mA
OPERATING TEMPERATURE RANGE					
		-40		+85	$^\circ\text{C}$

NOTES

¹TOKO # 617 DB-A0070 used for above specifications. MACOM ETC-1-IT-15 can be substituted.

²All distortion measurements taken with differential input signal and represent worst distortion across all gain codes.

³Between burst transients measured at the output of PULSE B5008 42 MHz diplexer.

Specifications subject to change without notice.

LOGIC INPUTS (TTL/CMOS Compatible Logic) ($\overline{\text{DATEN}}$, CLK, SDATA, $\overline{\text{PD}}$, $V_{CC} = 5\text{ V}$: Full Temperature Range)

Parameter	Min	Typ	Max	Unit
Logic "1" Voltage	2.1		5.0	V
Logic "0" Voltage	0		0.8	V
Logic "1" Current ($V_{INH} = 5\text{ V}$) CLK, SDATA, $\overline{\text{DATEN}}$	0		20	nA
Logic "0" Current ($V_{INL} = 0\text{ V}$) CLK, SDATA, $\overline{\text{DATEN}}$	-600		-100	nA
Logic "1" Current ($V_{INH} = 5\text{ V}$) $\overline{\text{PD}}$	50		190	μA
Logic "0" Current ($V_{INL} = 0\text{ V}$) $\overline{\text{PD}}$	-250		-30	μA

TIMING REQUIREMENTS (Full Temperature Range, $V_{CC} = 5\text{ V}$, $T_R = T_F = 4\text{ ns}$, $f_{CLK} = 8\text{ MHz}$ unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
Clock Pulsewidth (T_{WH})	16.0			ns
Clock Period (T_C)	32.0			ns
Setup Time SDATA vs. Clock (T_{DS})	5.0			ns
Setup Time $\overline{\text{DATEN}}$ vs. Clock (T_{ES})	15.0			ns
Hold Time SDATA vs. Clock (T_{DH})	5.0			ns
Hold Time $\overline{\text{DATEN}}$ vs. Clock (T_{EH})	3.0			ns
Input Rise and Fall Times, SDATA, $\overline{\text{DATEN}}$, Clock (T_R , T_F)			10	ns

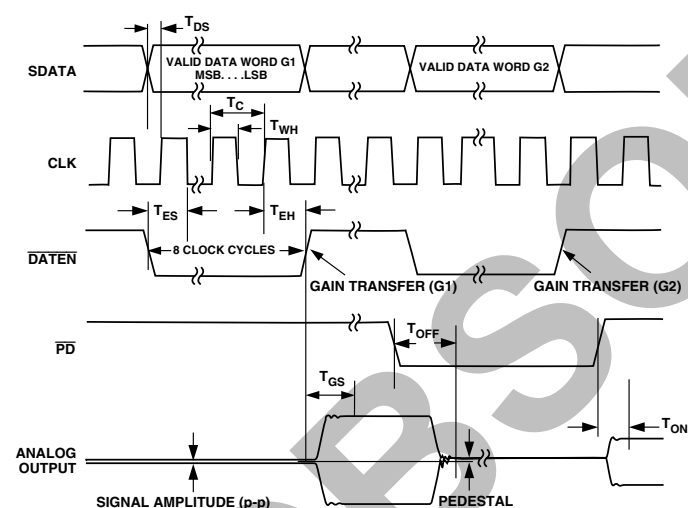


Figure 2. Serial Interface Timing

Table 1. Gain vs. Gain Code

Decimal Gain Code	8-Bit SPI Data Word MSB LSB	Nominal Gain (dB)
1	0 0 0 0 0 0 0 1	-12.64
2	0 0 0 0 0 0 1 0	-6.62
4	0 0 0 0 0 1 0 0	-0.60
8	0 0 0 0 1 0 0 0	5.42
16	0 0 0 1 0 0 0 0	11.44
32	0 0 1 0 0 0 0 0	17.46
64	0 1 0 0 0 0 0 0	23.48
128	1 x x x x x x x	29.50

0 = low, 1 = high, x = don't care.

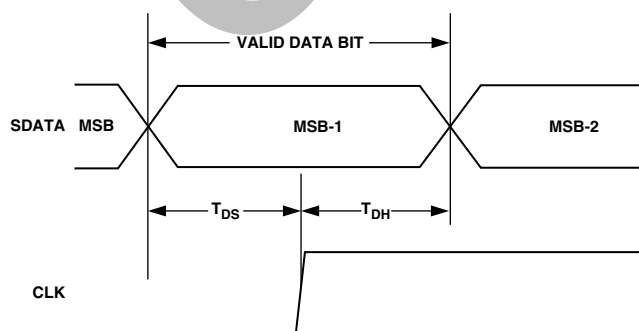


Figure 3. SDATA Timing

AD8322

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage +V_S

Pins 6, 8, 9, 20, 21, 23, 27 6 V

Input Voltages

Pins 25, 26 ±0.5 V

Pins 1, 2, 3, 7 –0.8 V to +5.5 V

Internal Power Dissipation

TSSOP (RU) 0.90 W

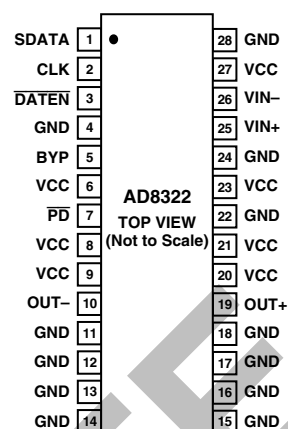
Operating Temperature Range –40°C to +85°C

Storage Temperature Range –65°C to +150°C

Lead Temperature, Soldering 60 seconds 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	θ_{JA}	Package Option
AD8322ARU	–40°C to +85°C	28-Lead TSSOP	67.7°C/W*	RU-28
AD8322ARU-REEL	–40°C to +85°C	28-Lead TSSOP	67.7°C/W*	RU-28
AD8322-EVAL		Evaluation Board		

*Thermal Resistance measured on SEMI standard 4-layer board.

CAUTION

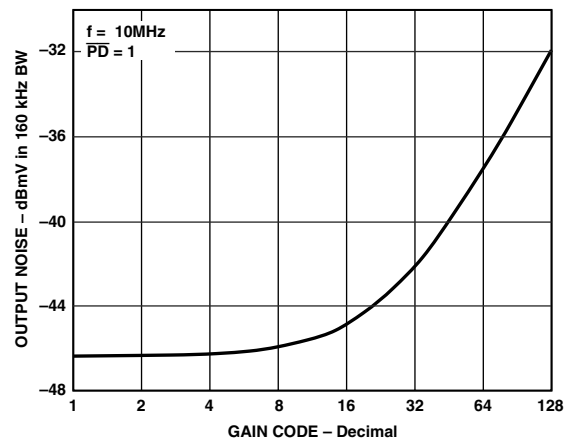
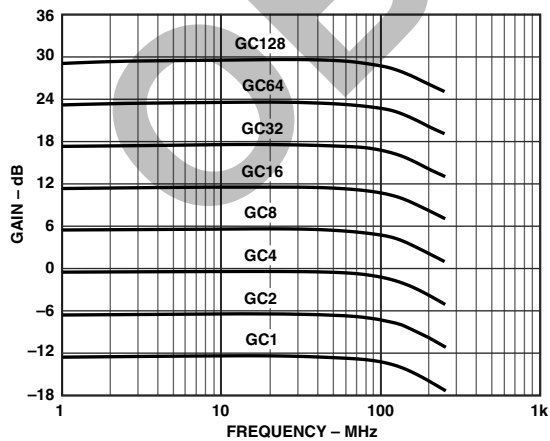
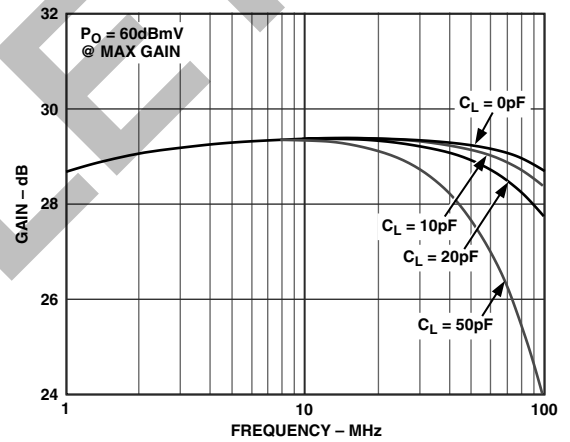
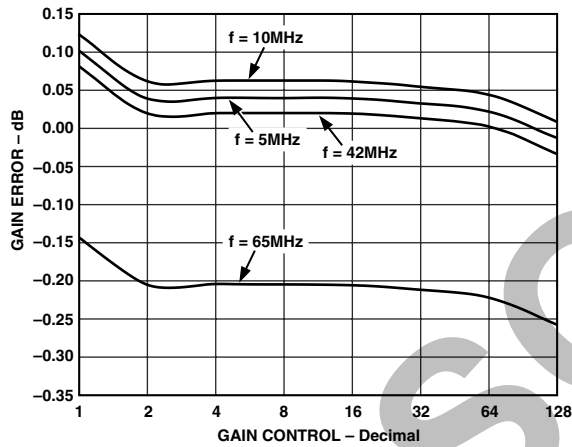
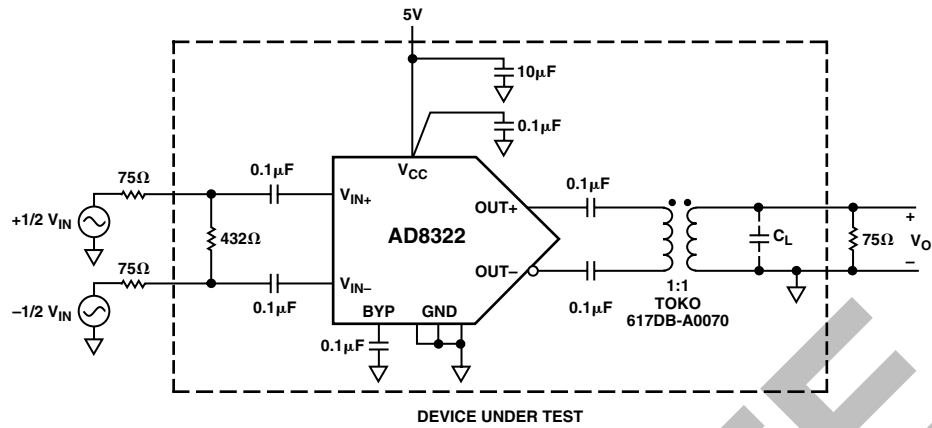
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8322 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

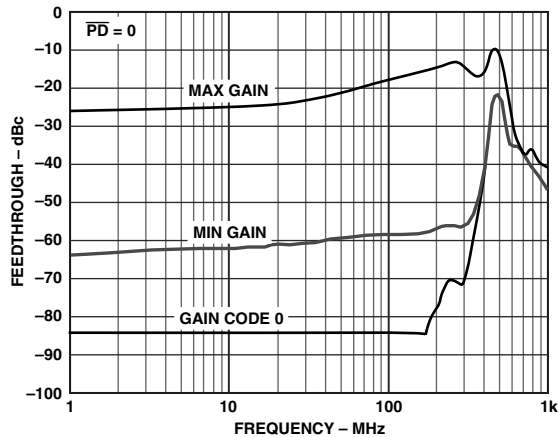


PIN FUNCTION DESCRIPTIONS

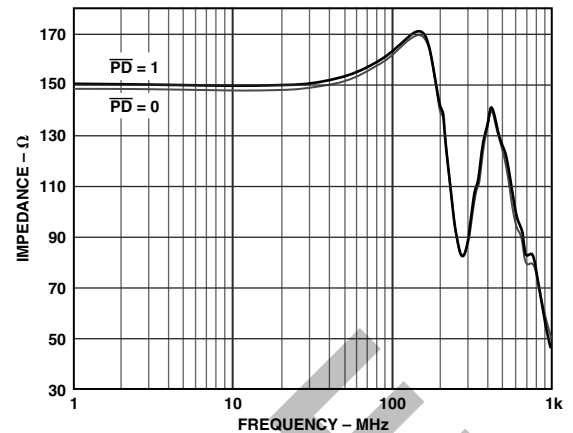
Pin No.	Mnemonic	Description
1	SDATA	Serial Data Input. This digital input allows for an 8-bit serial (gain) word to be loaded into the internal register with the MSB (Most Significant Bit) first.
2	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave register. A Logic 0-to-1 transition latches the data bit and a 1-to-0 transfers the data bit to the slave. This requires the input serial data word to be valid at or before this clock transition.
3	DATEN	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0-to-1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A 1-to-0 transition inhibits the data latch (holds the previous gain state) and simultaneously enables the register for serial data load.
4, 11, 12, 13, 14, 15, 16, 17, 18, 22, 24, 28	GND	Common External Ground Reference.
5	BYP	Internal Bypass. This pin must be externally ac-decoupled (0.1 µF capacitor).
6, 8, 9, 20, 21, 23, 27	VCC	Common Positive External Supply Voltage. A 0.1 µF capacitor must decouple each pin.
7	PD	Logic “0” powers down the part. Logic “1” powers up the part.
10	OUT–	Negative Output Signal.
19	OUT+	Positive Output Signal.
25	VIN+	Noninverting Input. DC-biased to approximately V _{CC} /2. Refer to Applications section for proper termination.
26	VIN–	Inverting Input. DC-biased to approximately V _{CC} /2. Refer to Applications section for proper termination.

Typical Performance Characteristics—AD8322

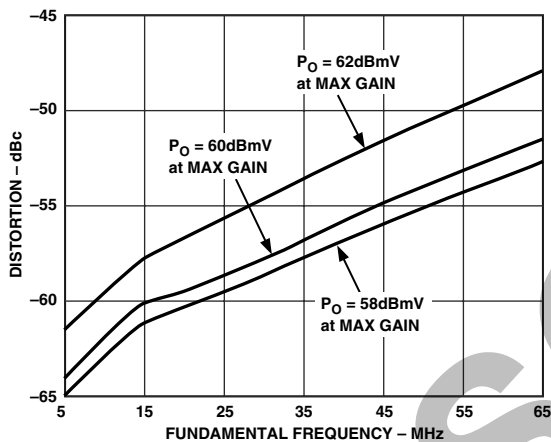




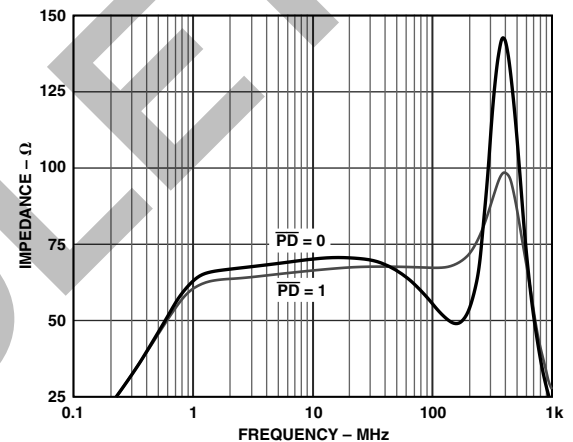
TPC 6. Input Signal Feedthrough vs. Frequency



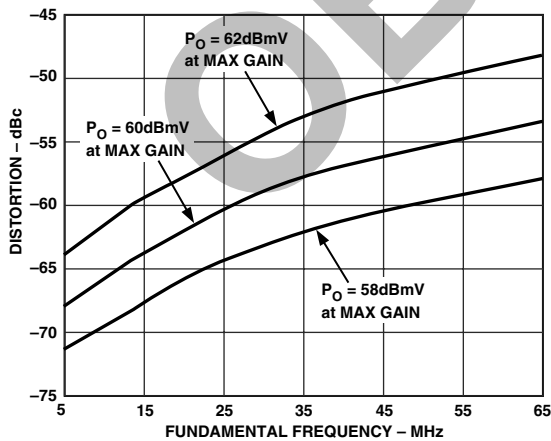
TPC 9. Input Impedance vs. Frequency (Inputs Shunted with 432 Ω)



TPC 7. Second Order Harmonic Distortion vs. Frequency for Various Output Levels



TPC 10. Output Impedance vs. Frequency



TPC 8. Third Order Harmonic Distortion vs. Frequency for Various Output Levels

AD8322

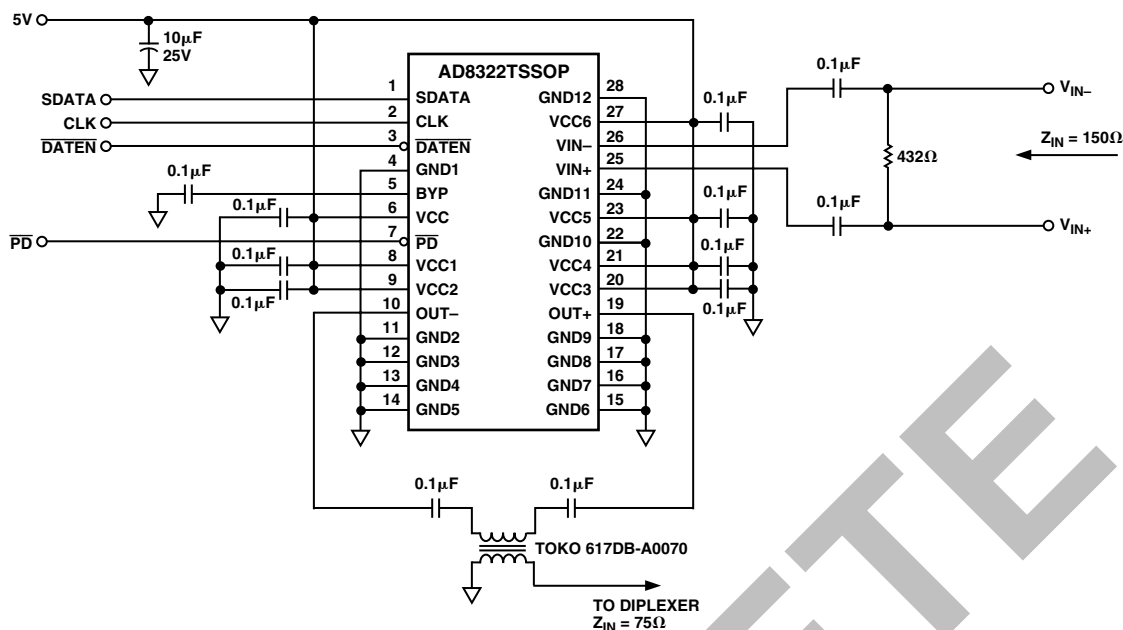


Figure 6. Typical Applications Circuit

Output Bias, Impedance, and Termination

The differential output pins V_{OUT+} and V_{OUT-} are also biased to a dc level of approximately $V_{CC}/2$. Therefore, the outputs should be ac-coupled before being applied to the load. This may be accomplished by connecting 0.1 μ F capacitors in series with the outputs as shown in the typical applications circuit of Figure 6. The differential output impedance of the AD8322 is internally maintained at 75 Ω , regardless of whether the amplifier is in forward transmit mode or reverse power-down mode, eliminating the need for external back termination resistors. A 1:1 transformer (TOKO #617DB-A0070) is used to couple the amplifier's differential output to the coaxial cable while maintaining a proper impedance match. If the output signal is being evaluated on standard 50 Ω test equipment, a 75 Ω to 50 Ω pad must be used to provide the test circuit with the correct impedance match.

Power Supply Decoupling, Grounding, and Layout Considerations

Careful attention to printed circuit board layout details will prevent problems due to associated board parasitics. Proper RF design technique is mandatory. The 5 V supply power should be delivered to each of the VCC pins via a low impedance power bus to ensure that each pin is at the same potential. The power bus should be decoupled to ground with a 10 μ F tantalum capacitor located in close proximity to the AD8322. In addition to the 10 μ F capacitor, each VCC pin should be individually decoupled to ground with a 0.1 μ F ceramic chip capacitor located as close to the pin as possible. The pin labeled BYP (Pin 5) should also be decoupled with a 0.1 μ F capacitor. The PCB should have a low impedance ground plane covering all unused portions of the component side of the board, except in the area of the input and output traces (see Figure 11). It is important to connect all of the AD8322 ground pins to ensure proper grounding of all internal nodes. The differential input and output traces should be kept as short and as symmetrical as possible. In addition, the input and output traces should be kept far apart in order to

minimize coupling (crosstalk) through the board. Following these guidelines will improve the overall performance of the AD8322 in all applications.

Initial Power-Up

When the 5 V supply is first applied to the VCC pins of the AD8322, the gain setting of the amplifier is indeterminate. Therefore, as power is first applied to the amplifier, the $\overline{PD}$ pin should be held low (Logic 0) thus preventing forward signal transmission. After power has been applied to the amplifier, the gain can be set to the desired level by following the procedure in the SPI Programming and Gain Adjustment section. The $\overline{PD}$ pin can then be brought from Logic 0 to 1, enabling forward signal transmission at the desired gain level.

Asynchronous Power-Down

The asynchronous $\overline{PD}$ pin is used to place the AD8322 into "Between Burst" mode while maintaining a differential output impedance of 75 Ω . Applying a Logic 0 to the $\overline{PD}$ pin activates the on-chip reverse amplifier, providing a 52% reduction in consumed power. The supply current is reduced from approximately 113 mA to approximately 54 mA. In this mode of operation, between burst noise is minimized and the amplifier can no longer transmit in the upstream direction.

Distortion, Adjacent Channel Power, and DOCSIS

In order to deliver 58 dBmV of high-fidelity output power required by DOCSIS, the PA should be able to deliver about 60 to 61 dBmV in order to make up for losses associated with the transformer and diplexer. It should be noted that the AD8322 was characterized with the TOKO 617DB-A0070 transformer. TPC 7 and TPC 8 show the AD8322 second and third harmonic distortion performance versus fundamental frequency for various output power levels. These figures are useful for determining the in-band harmonic levels from 5 MHz to 65 MHz. Harmonics higher in frequency will be sharply attenuated by the low-pass filter function of the diplexer. Another measure of signal integrity is adjacent channel power or ACP. DOCSIS section 4.2.9.1.1 states, "Spurious emissions from a transmitted carrier may occur

in an adjacent channel which could be occupied by a carrier of the same or different symbol rates.” Figure 7 shows the measured ACP, for a 16 QAM, 60 dBmV signal, taken at the output of the AD8322 evaluation board (see Figure 13 for evaluation board schematic). The transmit channel width and adjacent channel width in Figure 7 correspond to symbol rates of 160 K_{SYM/SEC}. Table II shows the ACP results for the AD8322 for all conditions in DOCSIS Table 4-7 “Adjacent Channel Spurious Emissions.”

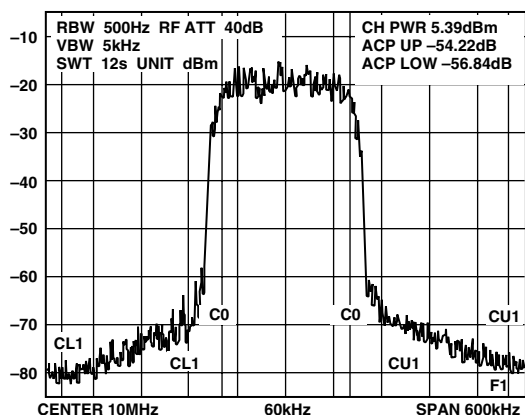


Figure 7. Adjacent Channel Power

Table II. ACP Performance for All DOCSIS Conditions
(All Values in dBc)

TRANSMIT CHANNEL SYMBOL RATE	ADJACENT CHANNEL SYMBOL RATE				
	160 K _{SYM/SEC}	320 K _{SYM/SEC}	640 K _{SYM/SEC}	1280 K _{SYM/SEC}	2560 K _{SYM/SEC}
160 K _{SYM/SEC}	-54.2	-54.7	-55.4	-56.6	-55.9
320 K _{SYM/SEC}	-53.8	-54.6	-54.6	-55.1	-54.8
640 K _{SYM/SEC}	-54.0	-54.1	-54.5	-54.4	-54.1
1280 K _{SYM/SEC}	-53.9	-54.1	-53.9	-54.3	-53.7
2560 K _{SYM/SEC}	-54.2	-54.2	-54.2	-53.8	-53.5

Noise and DOCSIS

At minimum gain, the AD8322's output noise spectral density is 12 nV/√Hz measured at 10 MHz. DOCSIS Table 4-8, “Spurious Emissions in 5 MHz to 42 MHz” specifies the output noise for various symbol rates. The calculated noise power in dBmV for 160 K_{SYM/SEC} is:

$$\left(20 \log \left(\sqrt{\left(\frac{12 \text{ nV}}{\sqrt{\text{Hz}}} \right)^2 \times 160 \text{ kHz}} \right) \right) + 60 = -46.4 \text{ dBmV}$$

Comparing the computed noise power of -46.4 dBmV to the 8 dBmV signal yields -54.4 dBc, which meets the required level of -53 dBc set forth in DOCSIS Table 4-8. As the AD8322's gain is increased from this minimum value, the output signal increases at a faster rate than the noise, resulting in a signal-to-noise ratio that improves with gain. In transmit disable mode the output noise spectral density computed over 160 K_{SYM/SEC} is 1.0 nV/√Hz or -68 dBmV.

Evaluation Board Features and Operation

The AD8322 evaluation board (Part # AD8322-EVAL) and control software can be used to control the AD8322 upstream cable driver via the parallel port of a PC. A standard printer cable connected between the parallel port and the evaluation board is used to feed all the necessary data to the AD8322 by means of the Windows® based, Microsoft Visual Basic control software. This package provides a means of evaluating the amplifier by providing a convenient way to program the gain/attenuation as well as offering easy control of the amplifiers asynchronous $\overline{\text{PD}}$ pin. With this evaluation kit the AD8322 can be evaluated with either a single-ended or differential input configuration. The amplifier can also be evaluated with or without the PULSE diplexer in the output signal path. To remove the diplexer from the signal path, move the two 0 Ω chip resistors R18 and R10 to locations R11 and R20. A schematic of the evaluation board is provided in Figure 13.

Overshoot on PC Printer Ports

The data lines on some PC parallel printer ports have excessive overshoot that may cause communications problems when presented to the CLK pin of the AD8322 (TP5 on the evaluation board). The evaluation board was designed to accommodate a series resistor and shunt capacitor (R1 and C15) to filter the CLK signal if required.

Transformer and Diplexer

A 1:1 transformer is needed to couple the differential outputs of the AD8322 to the cable while maintaining a proper impedance match. The specified transformer is available from TOKO (Part # 617DB-A0070), however, MA/COM part # ETC-1-1T-15 can also be used. The evaluation board is equipped with the TOKO transformer, but is also designed to accept the MA/COM transformer. The PULSE diplexer included on the evaluation board provides a high-order low-pass filter function, typically used in the upstream path. The ability of the PULSE diplexer to achieve DOCSIS compliance is neither expressed nor implied by Analog Devices Inc. Data on the diplexer should be obtained from PULSE.

Differential Inputs

The AD8322-EVAL evaluation board is designed to accommodate a Mini-Circuits T1-6T-KK81 1:1 transformer for the purpose of converting a single-ended (ground referenced) input signal to differential inputs. Figure 8 and the following paragraphs identify three options for providing differential input signals to the AD8322 evaluation board.

AD8322

Single-Ended-to-Differential Input (Figure 8 Option 1)

Install the Mini-Circuits T1-6T-KK81 1:1 transformer in the T1 location of the evaluation board. Install 0 Ω chip resistors in R12, R13, and R17, and leave R14, R16, and R19 open. For 75 Ω input impedance, install a 110 Ω resistor in R7 located on the back side of the evaluation board and leave R5 and R6 open. In this configuration the input signal must be applied to the V_{IN+} port of the evaluation board from a single-ended 75 Ω signal source. For input impedances other than 75 Ω , use the following equation to compute the correct value for R7.

$$\text{Desired Input Impedance} = R7 \parallel 235$$

Single-Ended-to-Differential Input (Figure 8 Option 2)

Install the Mini-Circuits T1-6T-KK81 1:1 transformer in the T1 location of the evaluation board. Install 0 Ω chip resistors in R12, R13, R17, and R19, and leave R14 and R16 open. For 75 Ω input impedance, install 55 Ω resistors in R5 and R6 located on the back side of the evaluation board and leave R7 open. In this configuration the input signal must be applied to the V_{IN+} port of the evaluation board from a single-ended 75 Ω signal source. For input impedances other than 75 Ω , use the following equation to compute the correct values for R5 and R6.

$$R5 = R6 = R, \text{Desired Input Impedance} = 2 \times (R \parallel 117.5)$$

Differential Input (Figure 8 Option 3)

If a differential signal source is available, it may be applied directly to both the V_{IN+} and V_{IN-} input ports of the evaluation board. In this case, install 0 Ω chip resistors in R8, R14, R15, and R16, and leave R12, R13, and R19 open. Referring to Figure 8 Option 3 and the AD8322 evaluation board, a differential input impedance of 150 Ω can be achieved by installing a 432 Ω resistor in R7, leaving R5 and R6 open. If another input impedance is desired, the following equation can be used to compute the correct value for R7.

$$\text{Desired Input Impedance} = R7 \parallel 235$$

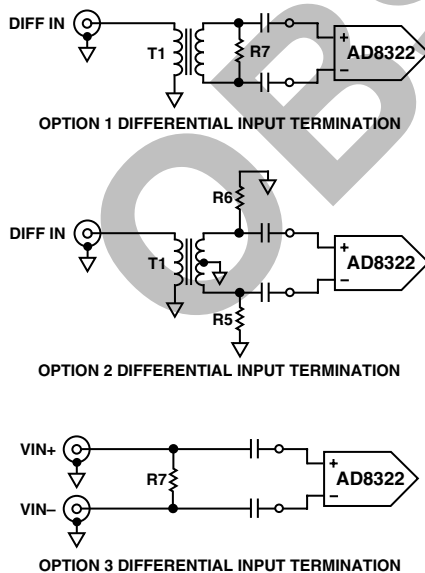


Figure 8. Differential Input Termination Options

Installing the Visual Basic Control Software

To install the "CABDRIVE_22" evaluation board control software, first close all Windows applications and run "SETUP.EXE" located on Disk 1 of the AD8322 Evaluation Software. Follow the on-screen instructions and insert Disk 2 when prompted to do so. Enter the path of the directory into which the software will be installed and select the button in the upper left corner to complete the installation.

Running the Software

To invoke the control software, go to START -> PROGRAMS -> CABDRIVE_22, or select the AD8322.EXE icon from the directory containing the software.

Controlling the Gain/Attenuation of the AD8322

The slide bar controls the AD8322's gain/attenuation, which is displayed in dB and in V/V. Although the AD8322 is designed for use at the eight gain codes described in the SPI Programming and Gain Adjustment section, all of the intermediate codes are included in the software. Code 0 is also included because of the high isolation it provides. The gain code (i.e., position of the slide bar) is displayed in decimal, binary, and hexadecimal (see Figure 9).

POWER-UP AND POWER-DOWN

The "Power-Up" and "Power-Down" buttons select the mode of operation of the AD8322 by controlling the logic level on the asynchronous $\overline{PD}$ pin. The "Power-Up" button applies a Logic 1 to the $\overline{PD}$ pin putting the AD8322 in forward transmit mode. The "Power-Down" button applies a Logic 0 to the $\overline{PD}$ pin selecting reverse mode, where the forward signal transmission is disabled while a back termination of 75 Ω is maintained.

Memory Section

The "MEMORY" section of the software provides a convenient way to alternate between two gain settings. The "X->M1" button stores the current value of the gain slide bar into memory while the "RM1" button recalls the stored value, returning the gain slide bar to that level. The "X->M2" and "RM2" buttons work in the same manner.

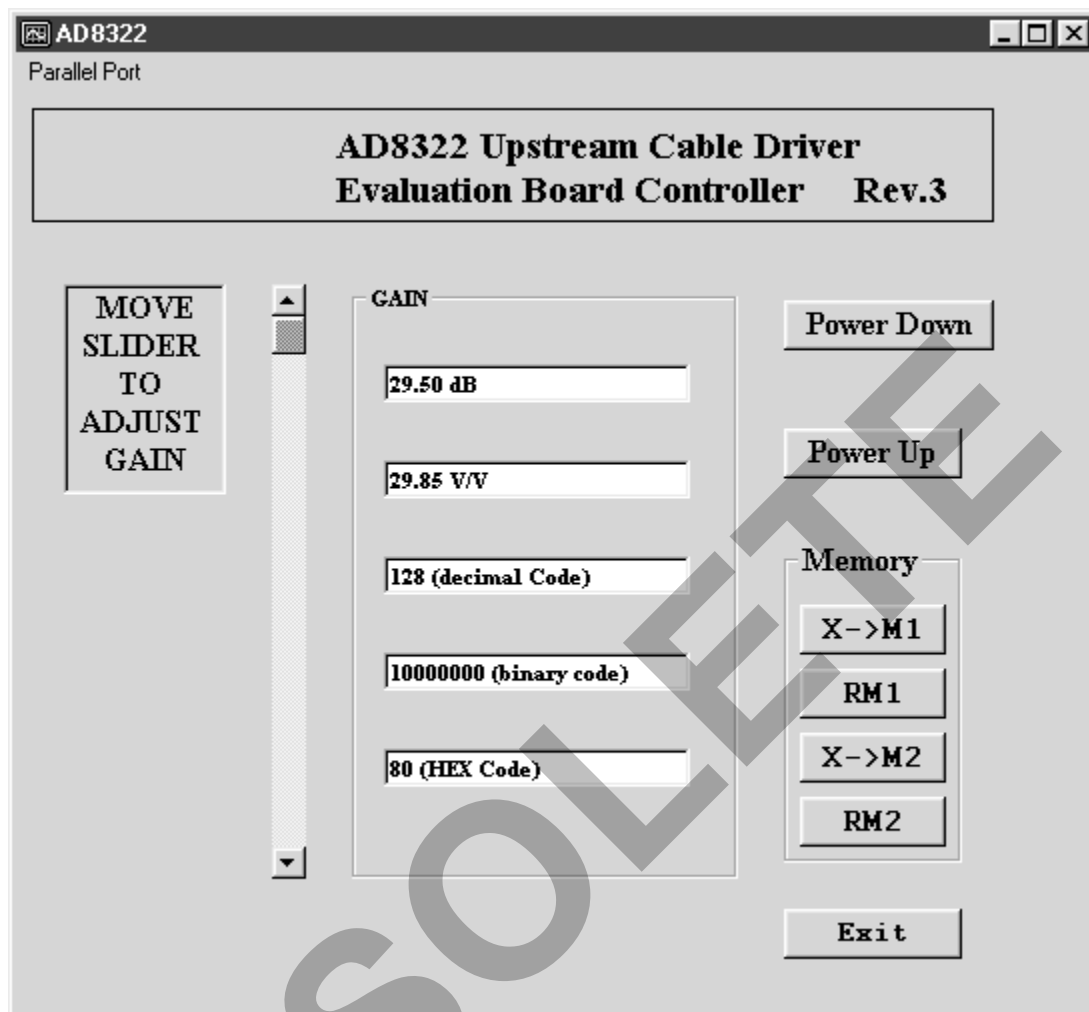


Figure 9. Screen Display of Windows-Based Control Software

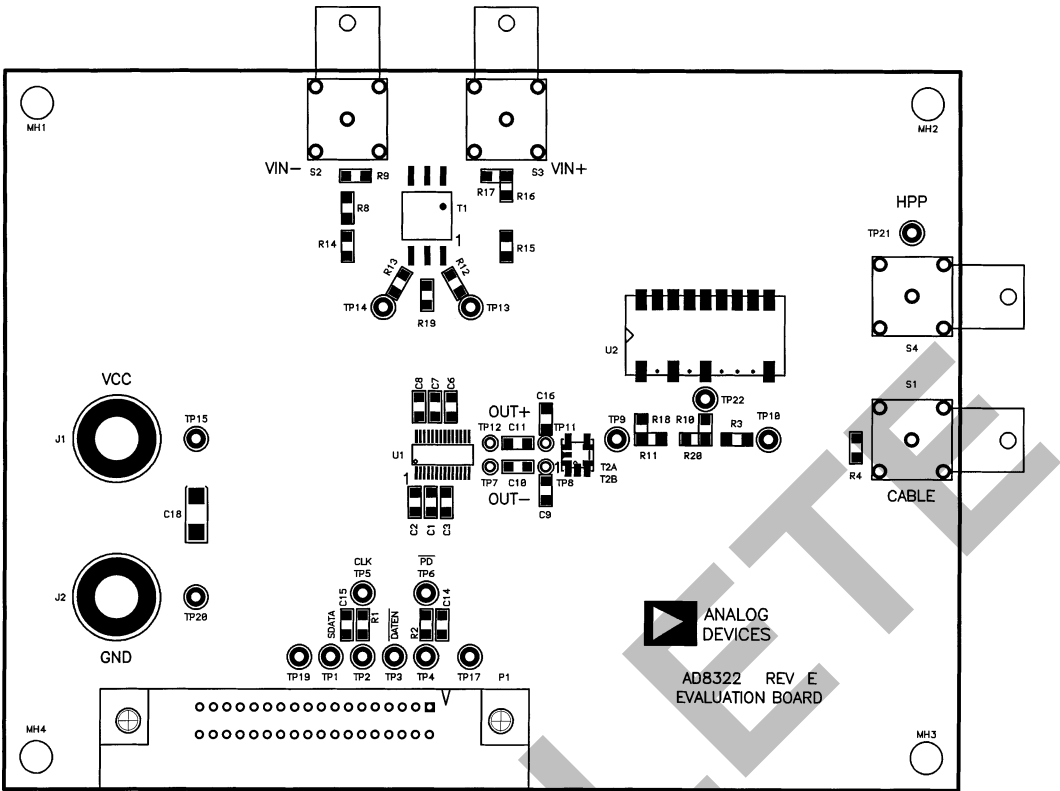


Figure 10. Evaluation Board—Assembly (Component Side)

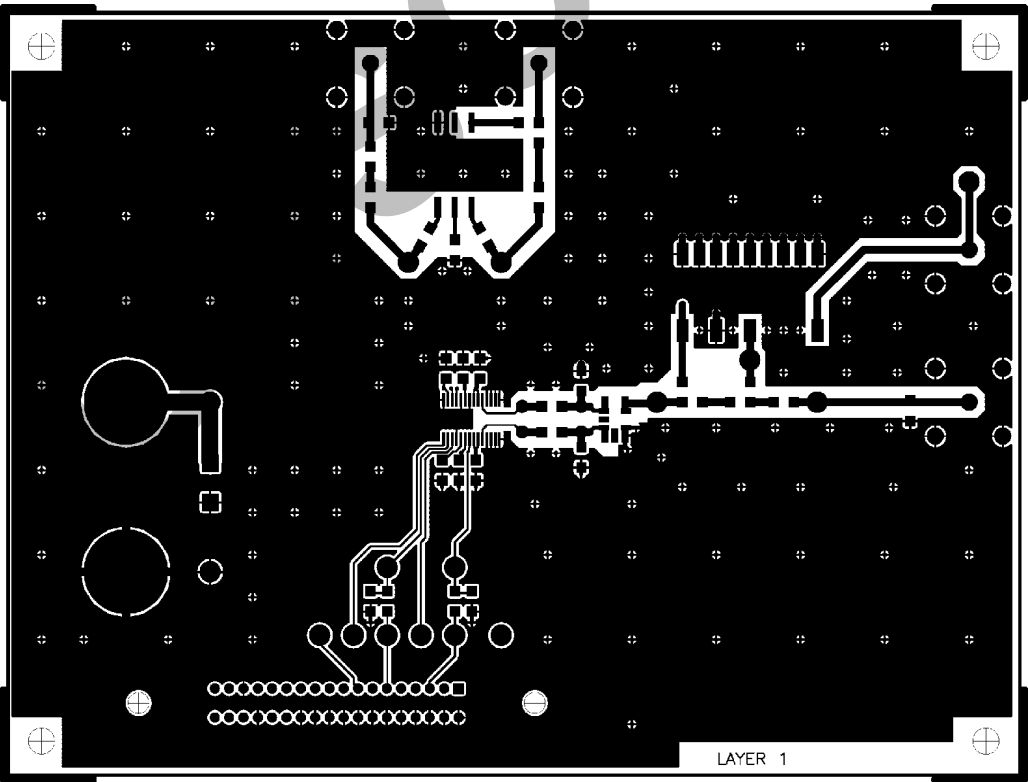


Figure 11. Evaluation Board Layout (Component Side)

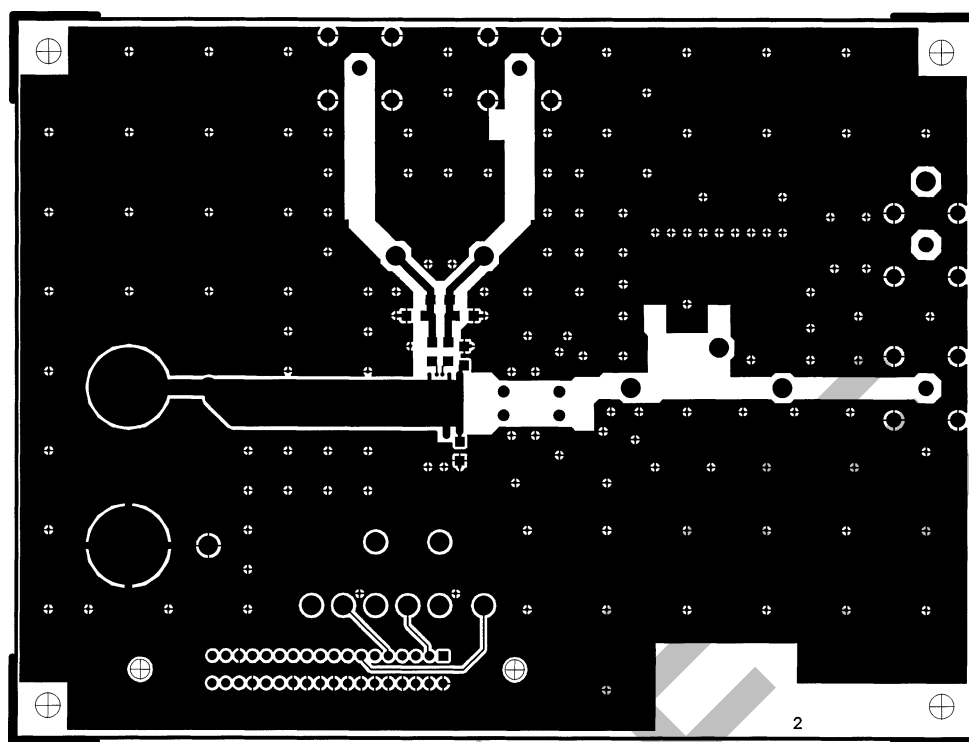


Figure 12. Evaluation Board—Solder Side

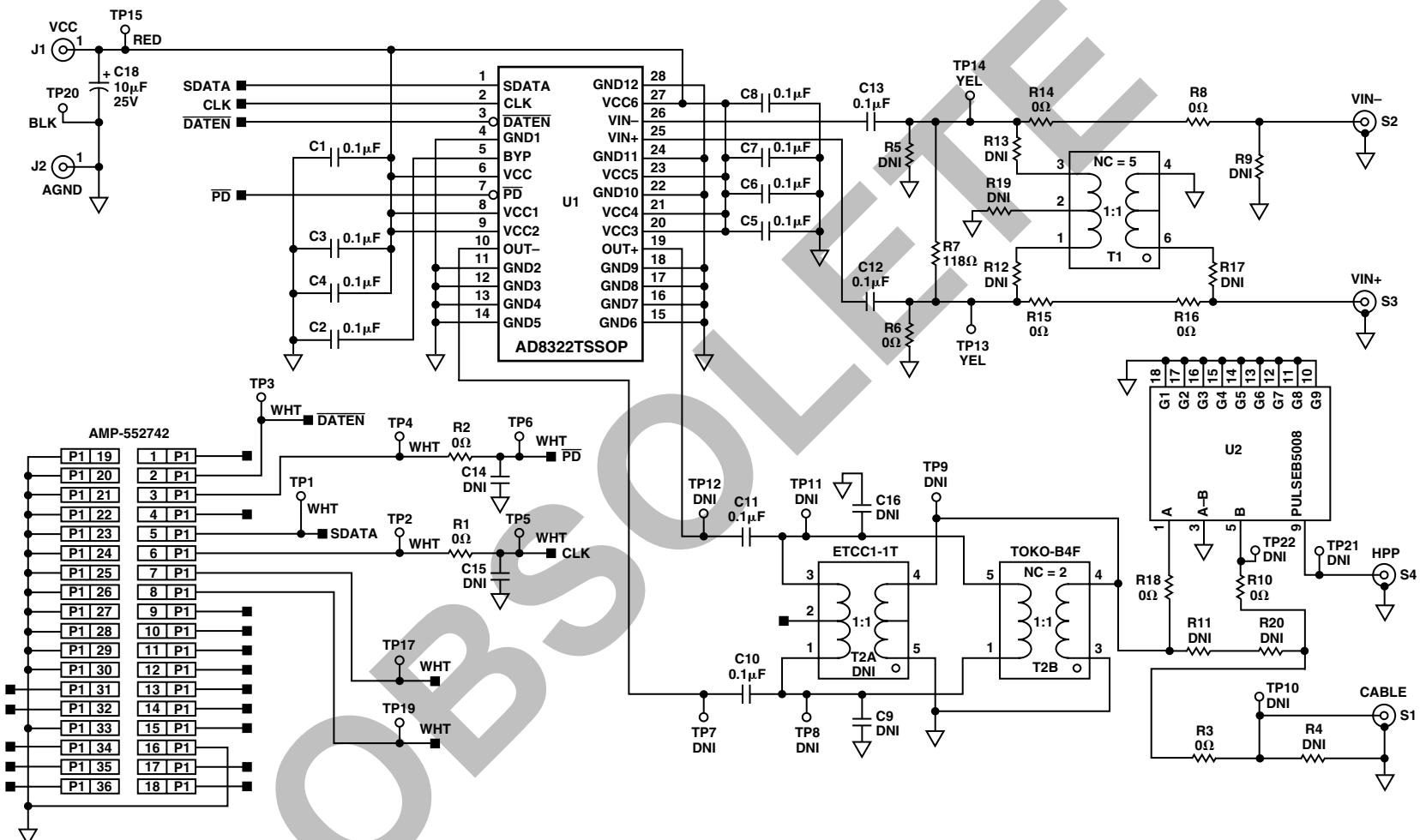


Figure 13. Evaluation Board Schematic

EVALUATION BOARD BILL OF MATERIALS

AD8322 Evaluation Board Rev. DC SINGLE-ENDED INVERTING INPUT – Revised – June 22, 2000

Qty.	Description	Vendor	Ref Desc.
1	10 μ F 16 V. 'C' size tantalum chip capacitor	ADS# 4-7-6	C18
12	0.1 μ F 50 V. 1206 size ceramic chip capacitor	ADS# 4-5-18	C1-8, 10-13
10	0 Ω 1/8 W. 1206 size chip resistor	ADS# 3-18-88	R1, 2, 3, 6, 8, 10, 14-16, 18
1	118 Ω 1% 1/8 W. 1206 size chip resistor	ADS# 3-18-106	R7
8	White Test Point (CLK, $\overline{\text{PD}}$, CP, SDATA, $\overline{\text{DATEN}}$)	ADS# 12-18-42	TP1-6, 17, 19
1	Black Test Point (GND)	ADS# 12-18-44	TP20
1	Red Test Point (VCC)	ADS# 12-18-43	TP15
2	Yellow Test Point (+/- INPUT)	ADS# 12-18-32	TP13 & TP14
4	75 Ω right-angle BNC Telegartner # J01003A1949	ADS# 12-6-28	S1-4 (INPUT, OUTPUT)
1	Centronics type 36-pin Right-Angle female connector	ADS# 12-3-50	P1
2	5-way Metal Binding Post	ADS# 12-7-7	J1, 2 (VCC, GND)
1	TOKO # 617 DB-A0070 transformer	Toko # 617DB-A0070	T2B
1	Diplexer PULSE*	PULSE	U2
1	AD8322 (TSSOP)	ADS# AD8322	D.U.T. (U1)
1	AD8322 REV. E Evaluation PC board	D.S.C.	Evaluation PC board
4	#4 – 40 $\times$ 1/4 inch ss panhead machine screw	ADS# 30-1-1	
4	#4 – 40 $\times$ 3/4 inch long aluminum round stand-off	ADS# 30-16-3	
2	# 2 – 56 $\times$ 3/8 inch ss panhead machine screw	ADS# 30-1-17	(p1 hardware)
2	# 2 steel flat washer	ADS# 30-6-6	(p1 hardware)
2	# 2 steel internal tooth lockwasher	ADS# 30-5-2	(p1 hardware)
2	# 2 ss hex. machine nut	ADS# 30-7-6	(p1 hardware)

DO NOT INSTALL C9, C14-C16, TP7-TP12, TP21, TP22, R4, R5, R9, R11-R13, R17, R19, R20, T1, T2A.

*PULSE Diplexer Part #'s B5008 (42 MHz), CX6002 (42 MHz), B5009 (65 MHz).

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

28-Lead TSSOP
(RU-28)

