DATA SHEET



TDA8722

I²C-bus programmable modulator for negative video modulation and FM sound

Product specification
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Philips
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PHILIPS

I²C-bus programmable modulator for negative video modulation and FM sound

TDA8722

FEATURES

- Video amplifier with clamp and white clip circuits
- FM sound modulator
- Asymmetrical and symmetrical RF outputs available
- Symmetrical RF oscillator using only a few external components
- External adjusting of modulation depth and level of the sound subcarrier
- I²C-bus receiver for frequency setting and test-mode selection
- One I²C programmable output port
- On-chip Phase-Locked Loop (PLL) frequency synthesizer
- On-chip power supply regulator
- Bus switchable oscillator
- On-chip Test Pattern Signal Generator (TPSG).

GENERAL DESCRIPTION

The TDA8722 is a programmable modulator which generates an RF TV channel from a baseband video signal and a baseband audio signal in the event of negative video and FM sound standards (PAL B/G, I, D/K and NTSC).

It is especially suited for satellite receivers, video recorders and cable converters. The video carrier frequency is set exactly to the correct channel frequency by a PLL synthesizer which is programmed in accordance with the I²C-bus format.

APPLICATIONS

- Video recorders
- Cable converters
- Satellite receivers.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8722T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA8722M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

QUICK REFERENCE DATA

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C after the IC has reached thermal equilibrium; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DD}	total supply current	normal mode	41	52	63	mA
Δm	typical modulation depth range	video level (pin 19) = 0.5 V (p-p); note 1; see Fig.10	65	–	90	%
$\Delta P/S$	typical picture-to-sound level range	note 2; see Fig.11	−18	–	−10	dB
V_{RF}	RF output voltage level asymmetrical on a 75 Ω load	frequency between 471.25 and 855.25 MHz	77	80	83	dBμV
δf	FM deviation on audio subcarrier	$f_i = 400$ Hz; $V_1 = 0.5$ V (RMS); before pre-emphasis filter	20	25	30	kHz

Notes

1. Value depends on value of resistor R17 (see Fig.7).
2. Value depends on value of capacitor C17 (see Fig.7).

BLOCK DIAGRAM

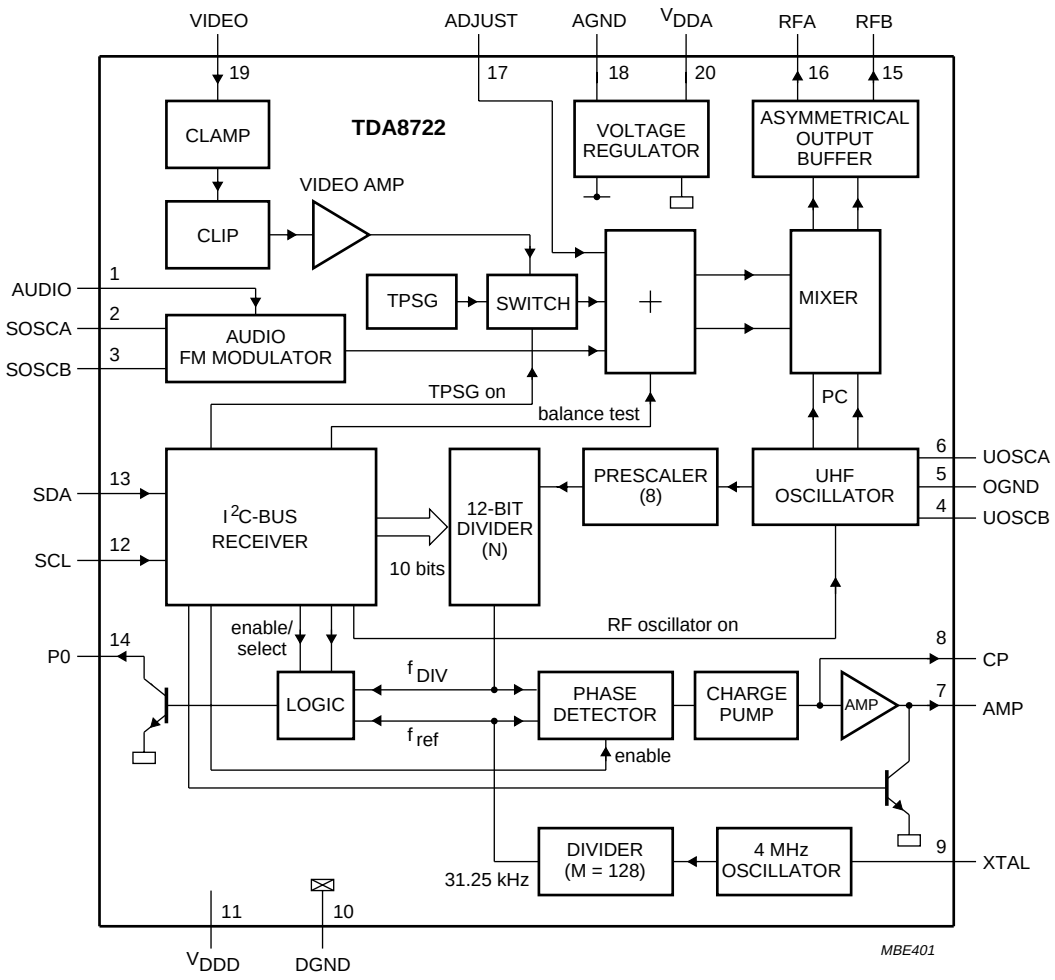


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AUDIO	1	audio input
SOSCA	2	sound oscillator A
SOSCB	3	sound oscillator B
UOSCB	4	UHF oscillator B
OGND	5	RF oscillator ground
UOSCA	6	UHF oscillator A
AMP	7	tuning amplifier output
CP	8	charge pump output
XTAL	9	crystal oscillator
DGND	10	digital ground
V_{DDD}	11	digital supply voltage
SCL	12	serial clock input (I²C-bus)
SDA	13	serial data input (I²C-bus)
P0	14	NPN open-collector output Port
RFB	15	asymmetrical RF output B
RFA	16	asymmetrical RF output A
ADJUST	17	modulation depth and picture-to-sound distance adjustment pin
AGND	18	analog ground
VIDEO	19	video input
V_{DDA}	20	analog supply voltage

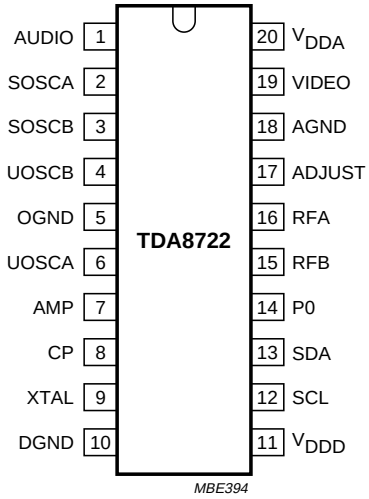


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8722 is a programmable modulator which can be divided into two main blocks:

- A modulator for negative video modulation and FM sound TV standards
- A programmable PLL frequency synthesizer.

The video part of the modulator consists of a clamping circuit which sets the internal reference voltage to the bottom of the synchronizing pulse, followed by a white clip which avoids over modulation in case the video signal is too strong. Typically, the IC starts to clip the video signal when the voltage at the video input (pin 19) is >560 mV (p-p) while the normal voltage at the video input is 500 mV (p-p). This clipping function ensures that the video modulation depth is not too high. The modulation depth is adjusted in the application between at least 65 and 90% by changing the resistor value between pin 17 and ground (R17). The value can change between 47 kΩ and infinite (R17 removed); see Fig.10.

The video part also contains a test pattern signal generator to simplify the adjustment of the receiving channel of the TV set to the required channel of the modulator. The pattern consists of a synchronization pulse and two vertical white bars on screen (see Fig.3).

The audio part of the modulator contains an FM sound modulator. The frequency of the sound subcarrier is set in the application by external components (C3, L3 and R3). The difference between the video carrier level and the sound subcarrier level is adjusted in the application by changing the value of the capacitor between pin 17 and ground (C17). The value can change between 0 and 47 pF. The distance between the video carrier and the sound subcarrier can be adjusted between at least −10 and −18 dB (see Fig.11).

To bias the audio input it is necessary to put a resistor in the application between pin 1 and ground. The resistor has a typical value of 12 kΩ.

The RF part of the oscillator consists of:

- An oscillator which operates at the required video carrier frequency. The range of the oscillator is determined in the application by C5, C6, L5 and D5.
- An RF mixer. It first combines the video signal and the sound subcarrier to build a baseband TV channel. Then the baseband signal is mixed with the oscillator signal to get the RF TV channel. The mixer has two outputs which can be used as two independent asymmetrical outputs, or as one symmetrical output. In the event of asymmetrical use, the unused output must be loaded with a 75 Ω resistor (see Fig.7).

The oscillator frequency is set by a programmable PLL frequency synthesizer in accordance with equation:

$f_{osc} = 8 \times N \times f_{ref}$

Where:

f_{osc} is the local oscillator frequency.

N is a 12-bit dividing number (10 bits are programmable by the I²C-bus).

f_{ref} is the crystal frequency (4 MHz) divided by 128 (31.25 kHz).

The circuit allows a step of 250 kHz but because only 10 bits are programmable, the programming steps are 1 MHz.
When the PLL loop is locked, both inputs of the phase comparator are equal, which gives equation:

$$f_{DIV} = \frac{f_{osc}}{8 \times N} = \frac{f_{xtal}}{128} = f_{ref}$$

During the test mode operation, f_{DIV} and f_{ref} can be monitored on the output Port pin (pin 14).

Software information

The synthesizer is controlled via a two-wire I²C-bus receiver. For programming, the address byte (C8 HEX) has to be sent first. Then one or two data bytes are used to set the 10 programmable bits of the dividing number N, the test bits (see Table 1) and the output Port state. Note that after power-up of the IC, the two data bytes must be sent.

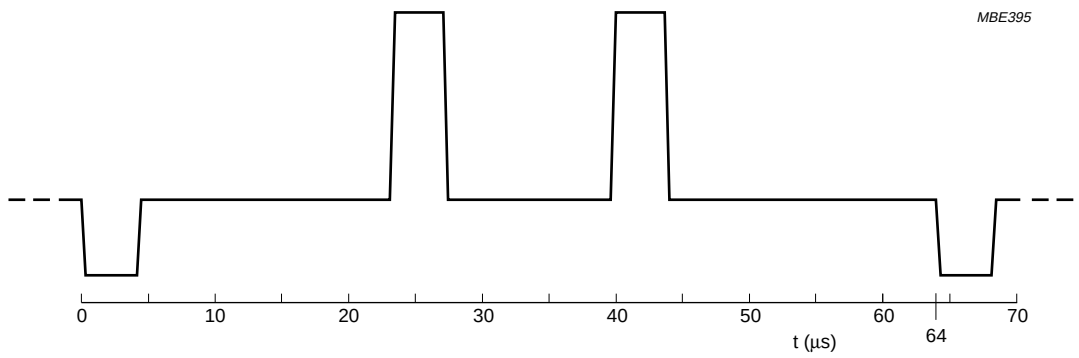


Fig.3 Test pattern signal.

Table 1 Data format; notes 1 and 2

BYTE	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	ACKNOWLEDGE BIT
Address byte C8	1	1	0	0	1	0	0	0	ACK
Data byte 1	0	b11	b10	b9	b8	b7	b6	b5	ACK
Data byte 2	1	T0(3)	T1(3)	T2(3)	P0(4)	b4	b3	b2	ACK

Notes

1. The 10 programmable bits of N are: b2 to b11.
2. Internal hardware sets: b1 = 0 and b0 = 1.
3. T0, T1 and T2 are bits used for test purposes (see Table 5).
4. P0 is a bit used for controlling the state of the output Port (see Table 6).

Table 2 Structure of the dividing number N

RESULT	BITS(1)											
	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1(2)	b0(2)
Frequency (MHz)(3)	512	256	128	64	32	16	8	4	2	1	0.5	0.25

Notes

1. Bits b2 to b11 are programmable and represent the integer part of the frequency in MHz. Bits b1 and b0 are fixed internally to b1 = 0 and b0 = 1 to get the added 0.25 MHz, common for most TV channels.
2. Bits b1 and b0 are not programmable.
3. f_{osc} = 512b11 + 256b10 + 128b9 + 64b8 + 32b7 + 16b6 + 8b5 + 4b4 + 2b3 + b2 + 0.25 (MHz).

Table 3 Dividing number N for programming channel 21 (471.25 MHz)

RESULT	BITS											
	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1(1)	b0(1)
Value	0	1	1	1	0	1	0	1	1	1	0	1
Frequency (MHz)(2)	0	256	128	64	0	16	0	4	2	1	0	0.25

Notes

1. Bits b1 and b0 are not programmable.
2. f_{osc} = 0 + 256 + 128 + 64 + 0 + 16 + 0 + 4 + 2 + 1 + 0.25 (MHz) = 471.25 MHz.

Table 4 Content of the data bytes to program channel 21 (471.25 MHz)

BYTE	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	ACKNOWLEDGE BIT
Address byte C8	1	1	0	0	1	0	0	0	ACK
Data byte 1	0	0	1	1	1	0	1	0	ACK
Data byte 2	1	0	0	0	0	1	1	1	ACK

It is possible to change only one data byte. The circuit will recognize which one is received with the value of MSB (0 for data byte 1 and 1 for data byte 2). It is possible to change the frequency by 1 MHz with data byte 2. It is easy to increment the channel frequency when its frequency width is 8 MHz by simply incrementing data byte 1.

The bits T0 to T2 are available for test purposes and the possibilities are shown in Table 5.

Table 5 Test modes

T0	T1	T2	OPERATIONAL MODE
0	0	0	normal operation
0	0	1	Test Pattern Signal Generator (TPSG) on; note 1
0	1	0	RF oscillator off; note 2
0	1	1	balance test; note 3
1	0	0	f_{ref} out (if p0 = 0); note 4
1	0	1	high-impedance test; note 5
1	1	0	f_{DIV} out (if p0 = 0); note 4
1	1	1	phase detector disabled; baseband signals on RF outputs; note 6

Notes

1. In ‘TPSG on’ mode the video carrier is modulated by the test signal consisting of a synchronization pulse and two vertical white bars on a black screen. This mode should be selected to adjust the TV set receiving the modulated signal to the right frequency.
2. In ‘RF oscillator off’ mode, the RF oscillator and the RF mixer are switched-off and there is no RF carrier coming out of the device. This mode can be selected to avoid RF radiation to other parts when the modulator output is not used.
3. In ‘balance test’, the video carrier is over modulated. This simplifies residual carrier measurements.
4. In ‘f_{ref}’ and ‘f_{DIV}’ modes, the reference frequency f_{ref} in the phase comparator or the divided RF oscillator frequency f_{DIV} is available on the output Port pin. This mode requires that bit P0 = 0.
5. The ‘high-impedance test’ mode may be used to inject an external tuning voltage to the RF tank circuit, to test the oscillator. In this mode, the phase detector is disabled and the external transistor of the tuning amplifier is switched-off. The AMP output (pin 7) is LOW (<200 mV).
6. In the ‘phase detector disabled’ mode, it is possible to measure the leakage current at the input of the tuning amplifier, on the CP pin. In this mode the RF oscillator is off, and the baseband TV channel signal is present on the RF outputs for testing the audio and video parts.

The possibilities of bit P0, which controls the output Port (pin 14) are given in Table 6.

The Port is an NPN open-collector type. For monitoring the f_{ref} or f_{DIV} frequency on the output Port, the P0 bit must be logic 0 to let the output Port free.

Table 6 Output Port programming

P0	OUTPUT PORT STATE
0	off; high impedance
1	on; sinking current

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	−0.3	+6	V
V_{DDD}	digital supply voltage	−0.3	+6	V
V_{DD}	operating supply voltage	4.5	5.5	V
V_{max}	maximum voltage on all pins	−0.3	V_{DD}	V
T_{stg}	IC storage temperature	−40	+125	°C
T_{amb}	operating ambient temperature	−20	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits. Every pin withstands the ESD test in accordance with *"MIL-STD-883C category B"* (2000 V). Every pin withstands the ESD test in accordance with Philips Semiconductors Machine Model (MM) 0 Ω, 200 pF (200 V).

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO20; SOT163-1	85	K/W
	SSOP20; SOT266-1	120	K/W

CHARACTERISTICS

V_{DDA} = V_{DDD} = 5 V; T_{amb} = 25 °C; valid over the whole UHF band; measured in circuit of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{DD}	supply current	normal mode	41	52	63	mA
		RF off test mode	30	38	46	mA
Video characteristics						
I_{19}	input current (AC)	V_{19} = 3.2 V	–	0.5	2.0	μA
z_{19}	video input impedance	V_{19} = 3.2 V	30	–	–	kΩ
m	modulation depth	V_{19} = 500 mV (p-p) EBU colour bars; R17 = 120 kΩ; see Fig.7	77	82	87	%
		during clipping condition; note 1	85	–	98	%
		TPSG mode; R17 = 120 kΩ	72	82	92	%
		balance test mode; R17 = 120 kΩ	110	–	–	%
Δm	modulation depth range	V_{19} = 500 mV (p-p) EBU colour bars; 47 kΩ ≤ R17 ≤ ∞	65	–	90	%
Δm_{APL}	variation of modulation depth with change of APL between 10 and 90%	referenced to the value for APL = 50%; V_{19} = 500 mV (p-p)	–2	–	+2	%
$V_{clip(p-p)}$	video input level where clipping starts (peak-to-peak value)	video level on pin 19; note 2	–	0.56	–	V
S/N video	video signal-to-noise ratio	f_{RF} < 700 MHz; note 3	48	52	–	dB
		f_{RF} > 700 MHz; note 3	46	50	–	dB
G_{diff}	differential gain	note 4	–8	–	+8	%
ϕ_{diff}	differential phase	note 4	–8	–	+8	deg
V/S	video-to-sync ratio	V_{19} = 500 mV (p-p); V/S = 7/3	6.9/3.1	7/3	7.1/2.9	
f_{video}	frequency response for the video signal	note 5	–1	–	+1	dB
Audio characteristics (for PAL G standard; audio subcarrier at 5.5 MHz)						
Z_1	audio input impedance		30	–	–	kΩ
δm	modulation deviation	f_1 = 400 Hz; V_1 = 0.5 V (RMS) before pre-emphasis filter	20	25	30	kHz
δm_{max}	maximum modulation deviation	f_1 = 400 Hz; V_1 = 2.0 V (RMS) before pre-emphasis filter	60	85	–	kHz
THD	total harmonic distortion	f_1 = 1 kHz; V_1 = 0.5 V (RMS) before pre-emphasis filter	–	0.4	1.5	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N audio	audio signal-to-noise ratio	note 6	45	50	–	dB
f_{audio}	frequency response of the audio signal	note 7	–1	–	+1	dB
P/S	picture-to-sound ratio	no audio signal; FM = 5.5 MHz; C17 = 15 pF	–16	–13	–10	dB
ΔP/S	picture-to-sound ratio range	no audio signal; FM = 5.5 MHz; 0 pF ≤ C17 ≤ 39 pF	–18	–	–10	dB
Channel characteristics						
f_{RF}	RF frequency range	using tank circuit of Fig.7	471.25	–	855.25	MHz
V_{RF}	output level on RFA and RFB	asymmetrical output loaded with 75 Ω; f = 471.25 to 855.25 MHz	77	80	83	dBμV
ΔV_{RF}	difference between the level of modulated carrier and the level of the unmodulated carrier	measurement is made during synchronization pulse for the modulated carrier	0	1	2	dB
SPO	spurious outside channel	note 8	–	–62	–	dBc
RF_{sh}	RF second harmonic level on asymmetrical output	f_{RF} = 471.25 MHz	–	–30	–25	dBc
		f_{RF} = 855.25 MHz	–	–20	–15	dBc
SC_{sh}	sound carrier second harmonic level	f_s = 5.5 MHz; C17 = 15 pF; f_{RF} < 700 MHz	–	–65	–60	dBc
		f_s = 5.5 MHz; C17 = 15 pF; f_{RF} > 700 MHz	–	–63	–58	dBc
SC_{th}	sound carrier third harmonic level	f_s = 5.5 MHz; C17 = 15 pF	–	–65	–60	dBc
	video signal harmonics	note 9	–	–60	–55	dBc
f_{ref}	reference frequency spurious	f_p + 31.25 kHz	–	–65	–60	dBc
IM	chrominance beat	note 10	–	–65	–60	dBc
Charge pump output (CP)						
I_8	output current		–	±100	–	μA
V_7	output voltage	in lock	1.5	–	2.5	V
I_{OZ}	OFF-state leakage current	V_{CP} = 2 V; T0 = 1; T1 = 1; T2 = 1	–	–	10	nA
Amplifier output (AMP)						
G	amplifier current gain	V_{CP} = 2 V; I_{AMP} = 10 μA	–	4000	–	
V_{7sat}	output saturation voltage	V_{CP} = 0 V; T0 = 1; T1 = 0; T2 = 1	–	140	200	mV
Crystal oscillator characteristics (XTAL)						
Z_9	oscillator input impedance		–	–	–500	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Port characteristics (P0)						
V_{OL}	LOW level output voltage	P0 = 1; I_{14} = 5 mA	–	150	400	mV
I_{OZ}	OFF-state leakage current	P0 = 0; V_{DD} = 5.5 V	–	–	10	µA
$I_{14(max)}$	maximum Port current	P0 = 1	–	–	10	mA
I²C-bus receiver characteristics (SDA and SCL)						
V_{IH}	HIGH level input voltage		3	–	5.5	V
V_{IL}	LOW level input voltage		0	–	1.5	V
I_{IH}	HIGH level input current	V_{IH} = 5 V; V_{DD} = 0 or 5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V; V_{DD} = 0 or 5 V	–10	–	–	µA
V_o	output voltage on SDA	during acknowledge pulse; I_{IL} = 3 mA	–	–	0.4	V

Notes

1. Modulation depth when the video signal is between 560 and 1000 mV (peak-to-peak value) at pin 19. R17 = 120 kΩ in the application.
2. For application information only.
3. Ratio between the CCIR 17 line bar amplitude (corresponding to the level difference between black and white; see Fig.4 and the RMS value of the noise on a black line (line 22 or 335) measured on the video signal after demodulation for PAL G standard. Measurement is unweighted, done between 200 kHz and 5 MHz.
4. Measured for PAL G standard on 4 first steps of CCIR 330 line, corresponding to a 5 step staircase with 300 mV (peak-to-peak value) chrominance carrier when the level between synchronization pulse and white is 1 V; see Fig.5.
5. Measured with a spectrum analyzer with ‘peak hold’ function, applying a 500 mV (peak-to-peak value) sine wave at the video input of the IC, with a frequency of 0.5, 2.0, 4.0 and 4.8 MHz. The reference is the value measured for 1.0 MHz.
6. Measured using CCIR 468-3 weighting filter and quasi-peak detection, with an audio frequency of 1 kHz and a deviation of 50 kHz. Video signal is EBU colour bars of 500 mV (peak-to-peak value) on pin 19.
7. Measured in PAL G standard with no pre-emphasis on the audio input and no de-emphasis in the receiver. Audio input level is adjusted for having a deviation of 25 kHz at 1 kHz audio frequency. Measurement is done for frequencies between 50 Hz and 15 kHz, reference is the level measured for 1 kHz.
8. Except for the harmonics of the RF oscillator frequency and for the combinations between the RF oscillator frequency and the sound oscillator frequency ($f_{RF} + 2f_s$, $2f_{RF} + f_s$, etc.). This measurement includes the spurious at the $\frac{1}{4}f_{RF}$, $\frac{1}{2}f_{RF}$ and $\frac{3}{4}f_{RF}$.
9. Corresponding to the harmonics of the video signal. Measured by putting a 1 MHz sine wave of 500 mV (peak-to-peak value) at the video input (pin 19) and checking the level at f_{RF} + 2 MHz, f_{RF} + 3 MHz, etc.
10. Measured with a 4.43 MHz sine wave of 350 mV (peak-to-peak value) at the video input. Measurement is the difference between the level of the unmodulated picture carrier and the level of the spike appearing at the frequency of the picture carrier plus 1.07 MHz. C17 = 15 pF in the application diagram of Fig.7.

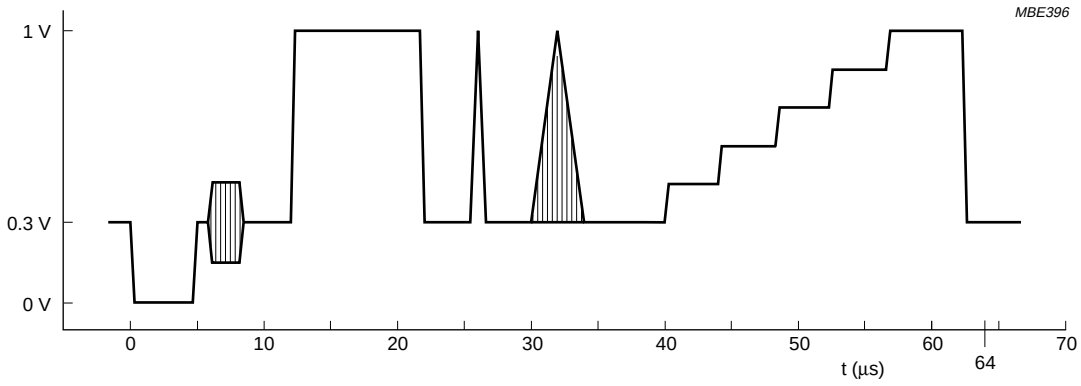


Fig.4 CCIR insertion line N.17.

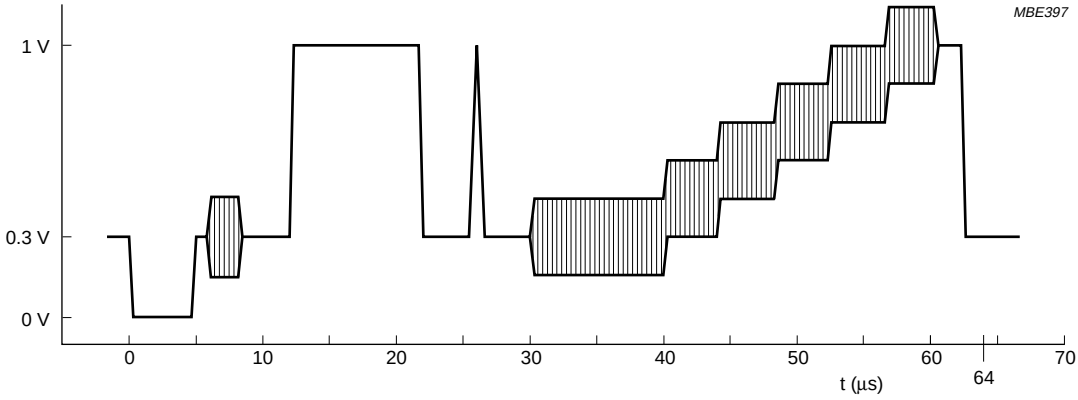
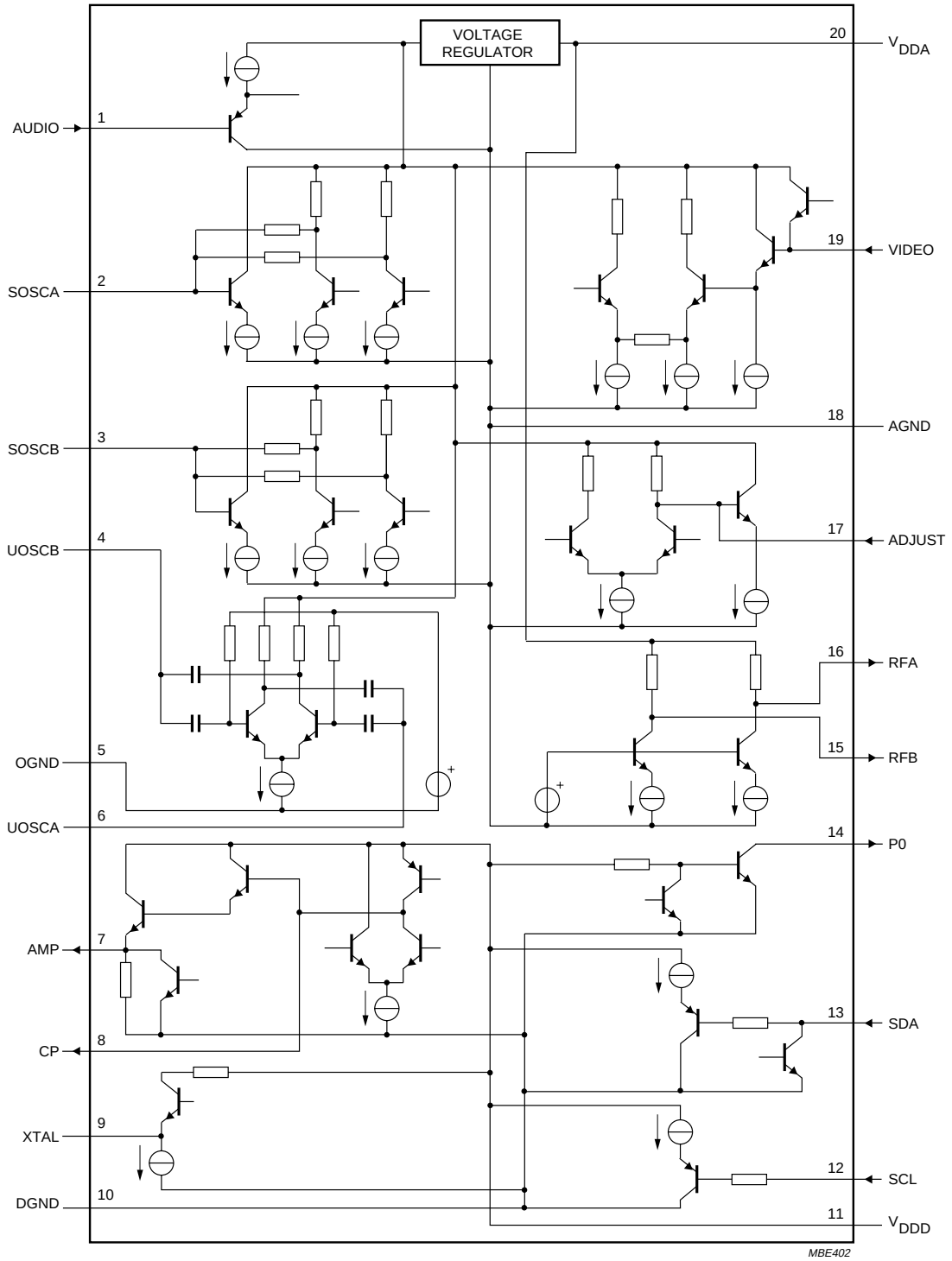


Fig.5 CCIR insertion line N.330.

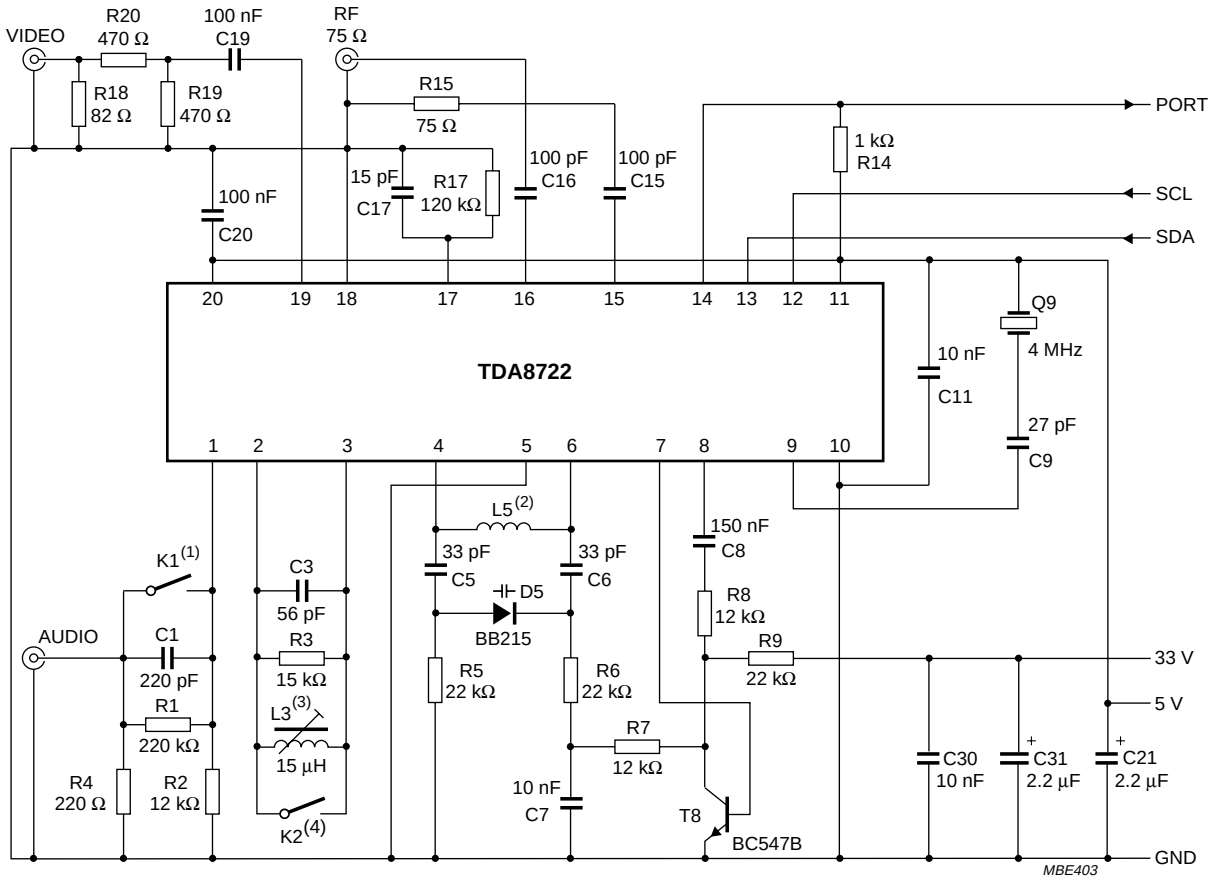
INTERNAL PIN CONFIGURATION



ESD protection components are not shown in the diagram.

Fig.6 Pin equivalent circuit for each pin.

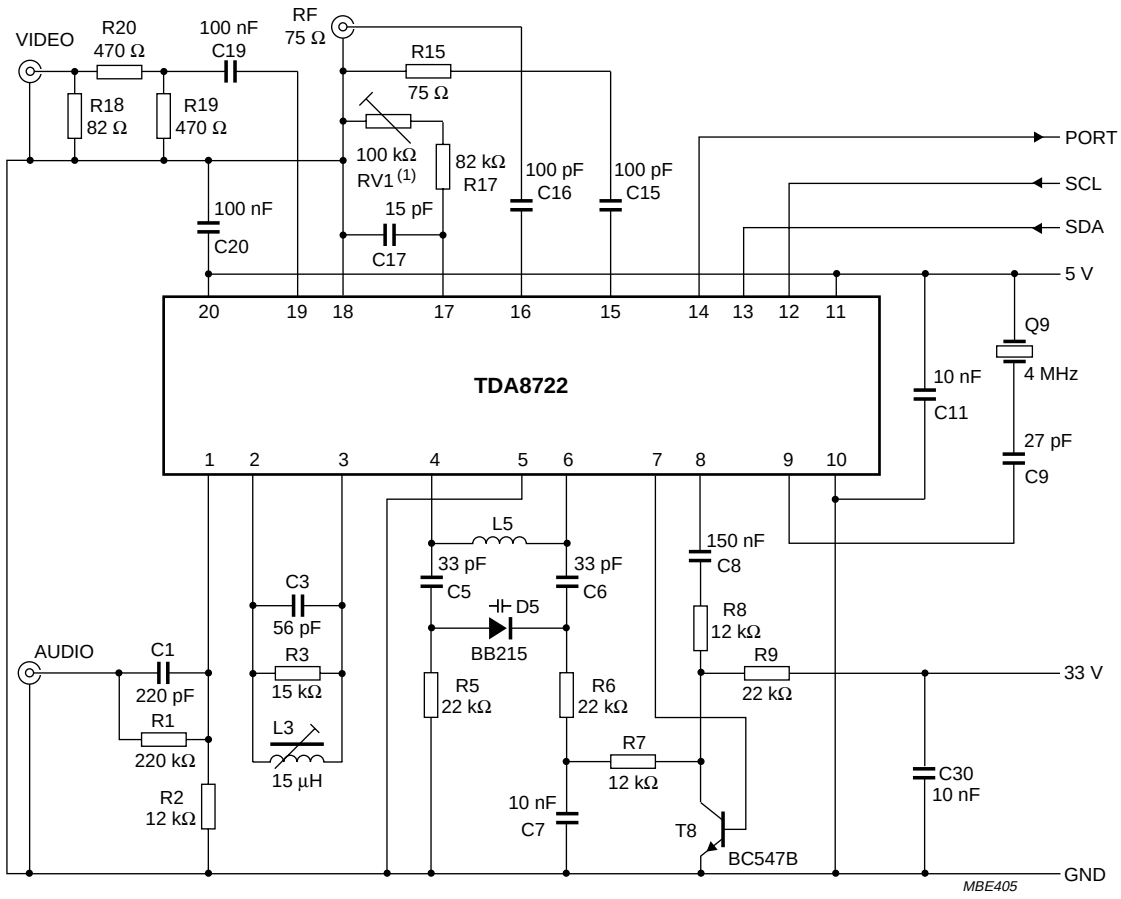
APPLICATION INFORMATION



(1) K1: switches the pre-emphasis filter on or off.
(2) L5: air coil; 1.5 turns; diameter of 2 mm.
(3) L3: to adjust the application to the right sound carrier frequency (5.5 MHz for PAL G).
(4) K2: Switches the FM sound oscillator on or off.

Fig.7 Reference measuring set-up.

Application design



(1) RV1 allows fine adjustment of the modulation depth between 70 and 90%.

Fig.8 Application using an asymmetrical output.

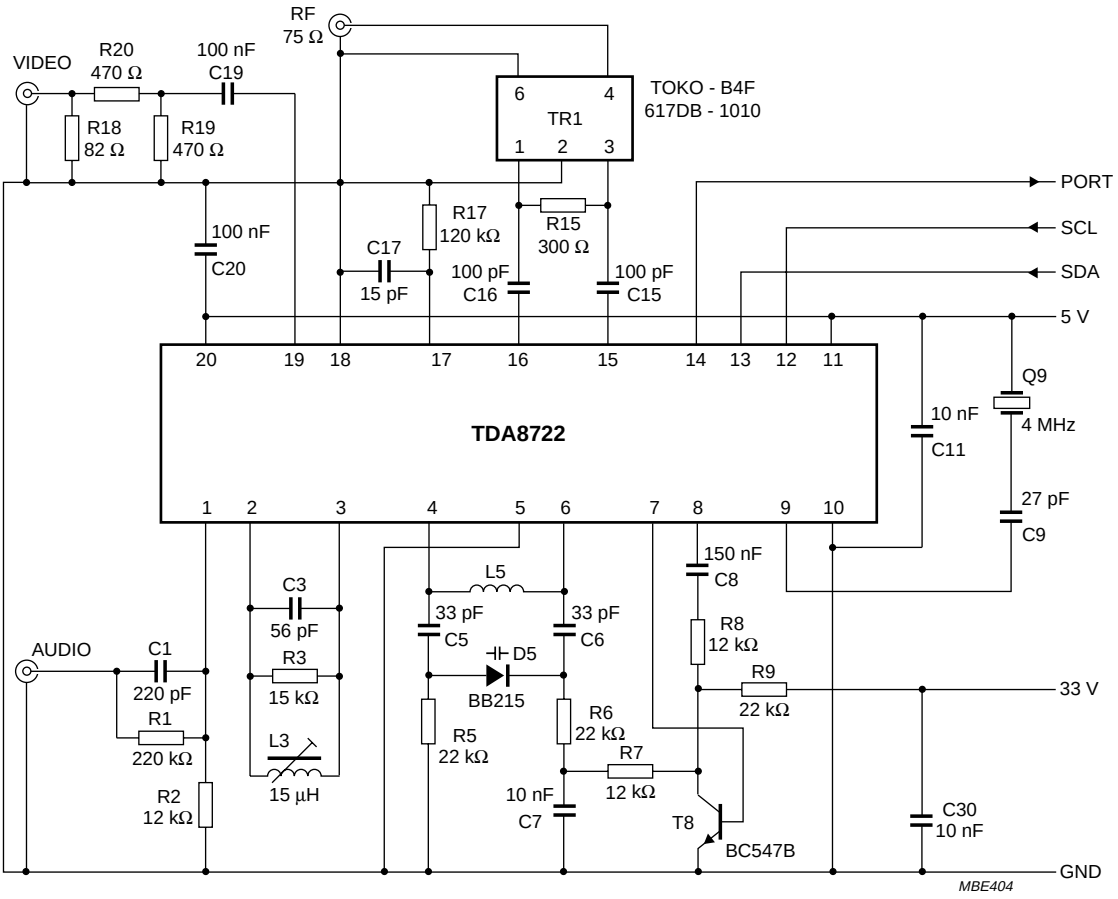


Fig.9 Application using a symmetrical output with a balun transformer.

In the design of the application, it is highly recommended to separate the part of the RF oscillator as much as possible from the part of the RF outputs in order to avoid parasitic coupling between these two parts.

A good solution is shielding the RF oscillator part to avoid radiation from and to this part. The pin 5 (OGND) must be connected to the shielding box and to ground.

RF outputs

For inexpensive applications, it is possible to use the IC with an asymmetrical output (pins 15 or 16). In this event, the unused output pin must be loaded with a load as similar as possible to the load connected to the used pin, see Fig.8.

A good improvement in performance is obtained using a 1 : 4 symmetrical to asymmetrical transformer (balun; balance-to-unbalance) connected between the two outputs. In this event both outputs have their loads matched. The level of the RF second harmonic, and the spurious outside channel is decreasing. The parasitic coupling between RF outputs and RF oscillator is also reduced (see Fig.9).

Modulation depth

With 500 mV (peak-to-peak value) video input signal, the wanted modulation depth must be set by the value of R17 (resistor between pin 17 and ground) as shown Fig.10. For a good accuracy, it is recommended to use a 1% type resistor.

It is also possible to use an adjustable resistor, see Fig.8.

Depending on the layout of the PCB, it may be necessary to slightly change the value of R17 from the one given in Fig.10 to get the wanted modulation depth.

Sound oscillator design

The frequency of the sound subcarrier is fixed by the tank circuit connected between pins 2 and 3. This frequency can be adjusted between 4.5 and 6.5 MHz covering all existing standards in the world.

The damping resistor R3 between pins 2 and 3 is necessary to decrease the quality factor of the tank circuit allowing the frequency to be modulated by the audio signal. The value of this resistor is calculated for several Q factor ranges of the coil for a sound frequency of 5.5 MHz (see Table 7).

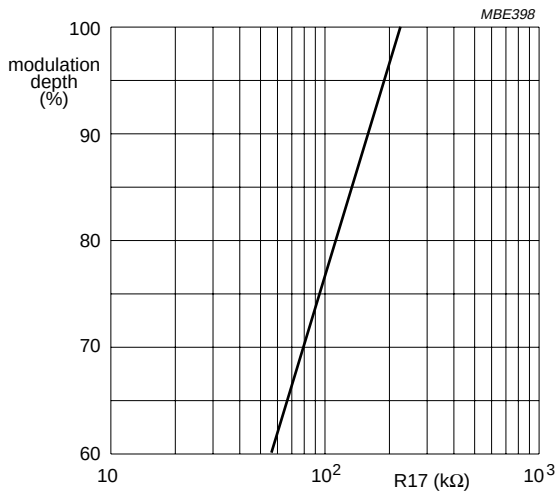


Fig.10 Typical modulation depth as a function of the value of R17.

Table 7 Value of resistor for several Q factor ranges

COIL QUALITY FACTOR	PROPOSED VALUE FOR R3 (kΩ)
30 to 40	82 to 33
40 to 50	33 to 27
50 to 60	27 to 22
60 to 80	22 to 18
80 to >100	18 to 15

The use of a coil with a quality factor <30 may result in a non operating oscillator. For safety, it is recommended to use a coil with a quality factor ≥50.

Picture-to-sound ratio

The picture-to-sound ratio can be adjusted in the application by changing the value of C17 (capacitor between pin 17 and ground); see Fig.11.

Figure 11 shows us that the picture-to-sound ratio will change for a constant value of C17 when the sound subcarrier frequency will change.

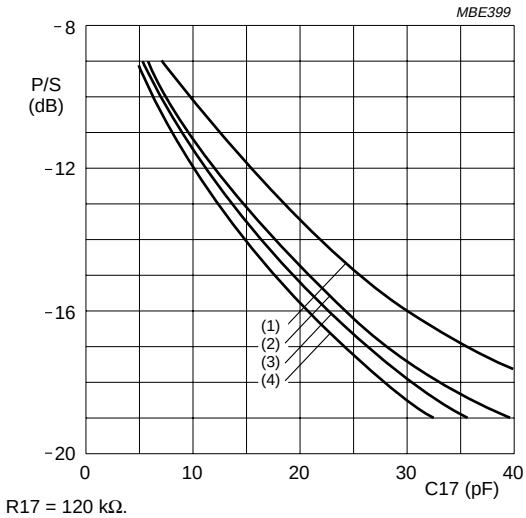
RF harmonics

This IC has been designed to have the lowest level of unwanted RF harmonics at the frequencies where these are the hardest to be filtered out, especially for the second harmonic of the RF carrier at the lowest frequencies of the UHF band.

The level of the second and third RF harmonic is shown in Fig.12 for an asymmetrical application. This chart gives a typical value while the level of these harmonics can vary depending on the design of the application.

It is possible to reduce the level of the second harmonic by using a wide band transformer at the output of the IC and create a symmetrical application (see Fig.9).

To reduce the out-of-band harmonics and especially the third one, it is necessary to use a low-pass filter at the output of the IC.



R17 = 120 kΩ.
(1) 4.5 MHz.
(2) 5.5 MHz.
(3) 6.0 MHz.
(4) 6.5 MHz.

Fig.11 Typical picture-to-sound ratio as a function of the value of C17.

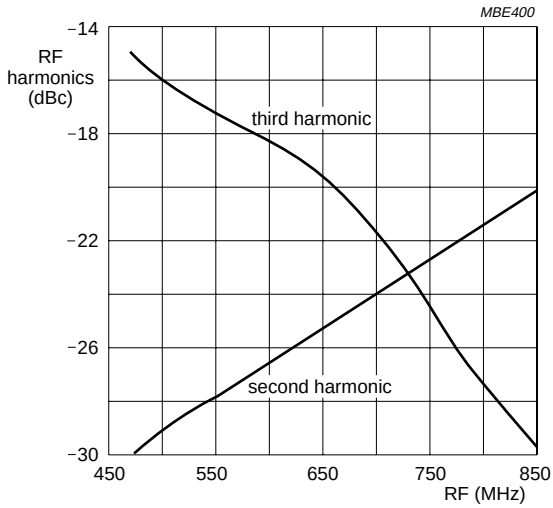


Fig.12 Typical level of RF harmonics for an asymmetrical application.

VHF operation

This IC can operate on frequencies as low as 200 MHz (and especially for VHF 3 band) provided the impedance of the tuned circuit between pins 4 and 6 is >1 kΩ.

NICAM and stereo

Because of the fact that the ADJUST pin (pin 17) is an access point to the RF mixer, it is possible to use this pin to inject an external modulated subcarrier into the IC.

This is especially interesting when it is necessary to transmit a second frequency modulated audio subcarrier for stereo sound (f = 5.72 MHz) or a NICAM QPSK modulated carrier for digital audio transmission (f = 5.85 or 6.552 MHz).

The incoming signal must be externally modulated either in FM with the desired signal corresponding to PAL B/G specification for stereo sound transmission, or in QPSK in accordance with the NICAM transmission system.

The input impedance on pin 17 is approximately 3500 Ω, the incoming signal must be capacitive coupled, the resistor R17 between pin 17 and ground must remain to adjust the modulation depth, the capacitor C17 between pin 17 and ground may be changed depending on the capacitance brought on by the incoming network. If this capacitance is large, it is possible to remove C17. Figure 13 shows a possible application for injecting such kind of signal into the modulator IC.

Following this application, to get a picture-to-second sound carrier ratio of −20 dB, it is necessary to apply a level of approximately 800 mV (peak-to-peak value) at the second carrier input, when the picture-to-first sound carrier ratio is approximately −13 dB.

In addition, the internal FM sound modulator can be switched off by short-circuiting pins 2 and 3.

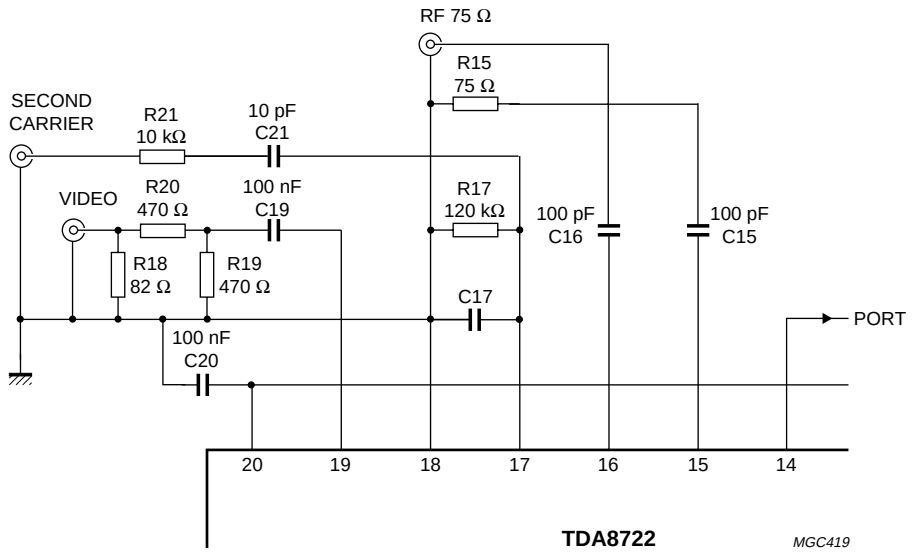
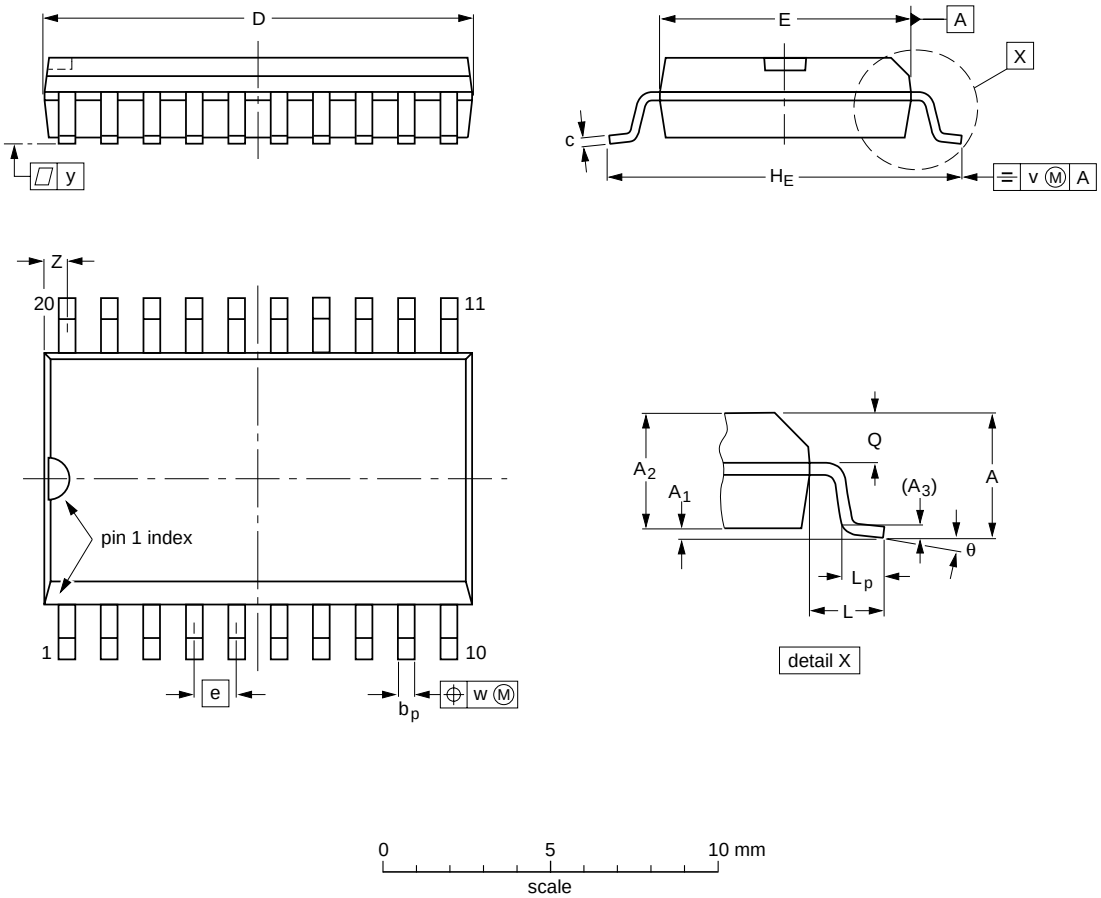


Fig.13 Possible application for a second sound subcarrier.

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

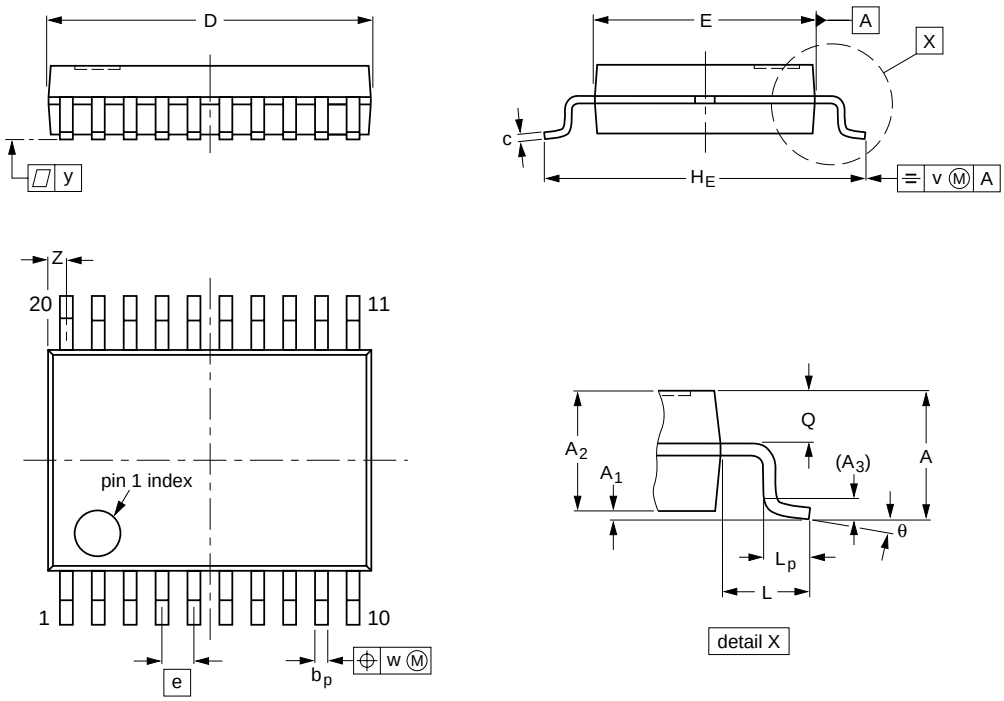
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

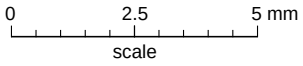
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO and SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

SSOP

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

METHOD (SO AND SSOP)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

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Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

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Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
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Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
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Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
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Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

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Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
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04547-130 SÃO PAULO, SP, Brazil,
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Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
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Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
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United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
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