



SN74LVC2G04 Dual Inverter Gate

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.1 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- IP Phones: Wired and Wireless
- Optical Modules
- Optical Networking: EPON and Video Over Fiber
- Point-to-Point Microwave Backhaul
- Power: Telecom DC/DC Module: Analog and Digital
- Private Branch Exchanges (PBX)
- TETRA Base Exchanges
- Telecom Base Band Units
- Telecom Shelters: Power Distribution Units (PDU), Power Monitoring Units (PMU), Wireless Battery Monitoring, Remote Electrical Tilt Units (RET), Remote Radio Units (RRU), Tower Mounted

Amplifiers (TMA)

- Vector Signal Analyzers and Generators
- Video Converencing: IP-Based HD
- WiMAX and Wireless Infrastructure Equipment
- Wireless Communications Testers and Wireless Repeaters
- xDSL Modems and DSLAM

3 Description

This dual inverter is designed for 1.65-V to 5.5-V V_{CC} operation. The SN74LVC2G04 device performs the Boolean function $Y = \overline{A}$.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2G04DBV	SOT-23 (6)	2.90 mm $\times$ 1.60 mm
SN74LVC2G04DCK	SC70 (6)	2.00 mm $\times$ 1.25 mm
SN74LVC2G04DRL	SOT (6)	1.60 mm $\times$ 1.20 mm
SN74LVC2G04YZP	DSBGA (6)	1.41 mm $\times$ 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Logic Diagram (Positive Logic)

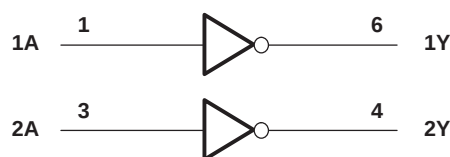


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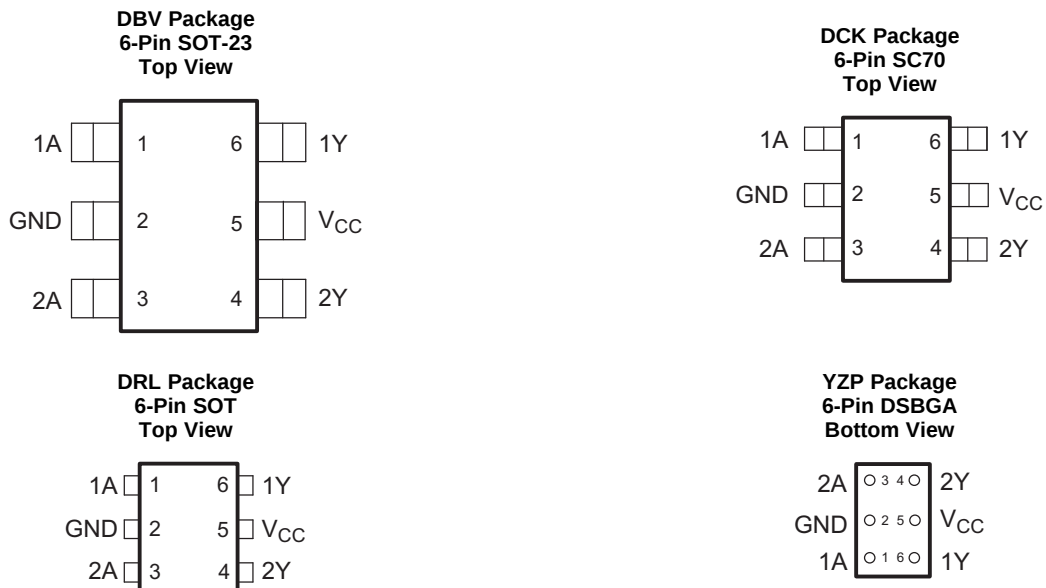
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (November 2013) to Revision N	Page
Removed the <i>Ordering Information table</i>, added the <i>Device Information table</i>, ESD Ratings table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.	1

Changes from Revision L (January 2007) to Revision M	Page
- Updated document to new TI data sheet format. - Added ESD warning - Updated operating temperature range.	1 4 4

5 Pin Configuration and Functions



Pin Functions⁽¹⁾

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	I	Inverter 1 input
1Y	6	O	Inverter 1 output
2A	3	I	Inverter 2 input
2Y	4	O	Inverter 2 output
GND	2	—	Ground
V _{CC}	5	—	Power

(1) See [Mechanical, Packaging, and Orderable Information](#) for dimensions.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	6.5	V
V _I	Input voltage ⁽²⁾		−0.5	6.5	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	6.5	V
V _O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±50		mA
	Continuous current through V _{CC} or GND		±100		mA
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	+2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	+1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See ⁽¹⁾.

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		−4	mA
		V _{CC} = 2.3 V		−8	
		V _{CC} = 3 V		−16	
		V _{CC} = 4.5 V		−24	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

Recommended Operating Conditions (continued)

See ⁽¹⁾.

		MIN	MAX	UNIT
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	mA
		$V_{CC} = 2.3\text{ V}$	8	
		$V_{CC} = 3\text{ V}$	16	
			24	
		$V_{CC} = 4.5\text{ V}$	32	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$	20	ns/V
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	10	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	5	
T_A	Operating free-air temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC2G04				UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	165	259	142	123	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}	$I_{OH} = -100\text{ }\mu\text{A}$	1.65 V to 5.5 V	$V_{CC} - 0.1$			V
	$I_{OH} = -4\text{ mA}$	1.65 V	1.2			
	$I_{OH} = -8\text{ mA}$	2.3 V	1.9			
	$I_{OH} = -16\text{ mA}$	3 V	2.4			
	$I_{OH} = -24\text{ mA}$		2.3			
	$I_{OH} = -32\text{ mA}$	4.5 V	3.8			
V_{OL}	$I_{OL} = 100\text{ }\mu\text{A}$	1.65 V to 5.5 V			0.1	V
	$I_{OL} = 4\text{ mA}$	1.65 V			0.45	
	$I_{OL} = 8\text{ mA}$	2.3 V			0.3	
	$I_{OL} = 16\text{ mA}$	3 V			0.4	
	$I_{OL} = 24\text{ mA}$				0.55	
	$I_{OL} = 32\text{ mA}$	4.5 V			0.55	
I_I	A inputs	$V_I = 5.5\text{ V or GND}$	0 to 5.5 V		± 5	μA
I_{off}		$V_I \text{ or } V_O = 5.5\text{ V}$	0		± 10	μA
I_{CC}		$V_I = 5.5\text{ V or GND}, I_O = 0$	1.65 V to 5.5 V		10	μA
ΔI_{CC}	One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	μA
C_i		$V_I = V_{CC} \text{ or GND}, -40^\circ\text{C to } 85^\circ\text{C}$	3.3 V	3.5		pF

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN74LVC2G04

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6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	-40°C to 85°C	3.1	8	1.5	4.4	1.2	4.1	1	3.2	ns
			-40°C to 125°C	3.1	8	1.5	4.9	1.2	4.6	1	3.7	ns

6.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	14	14	14	16	pF

6.8 Typical Characteristics

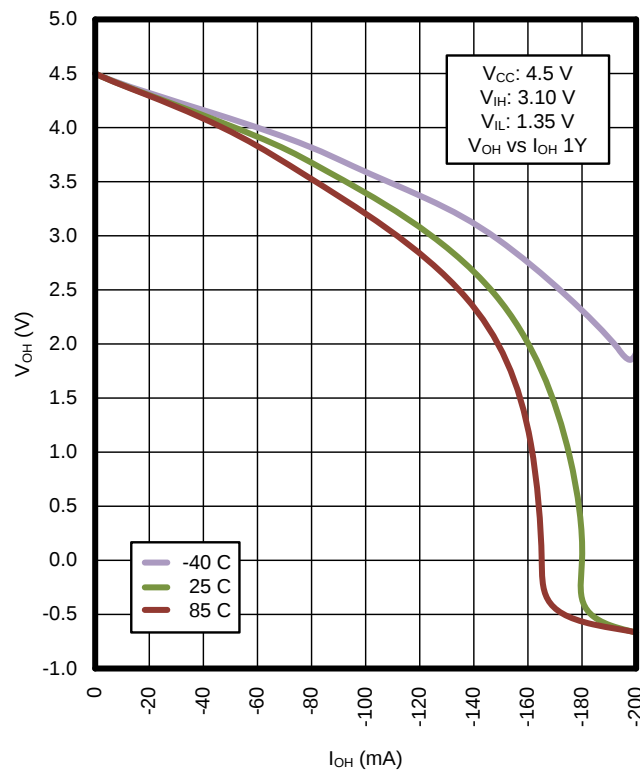
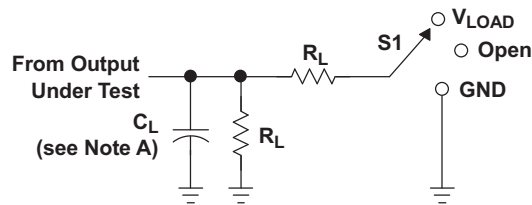


Figure 1. I_{OH} vs V_{OH}

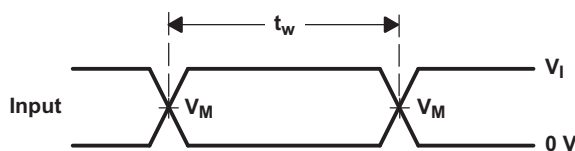
7 Parameter Measurement Information



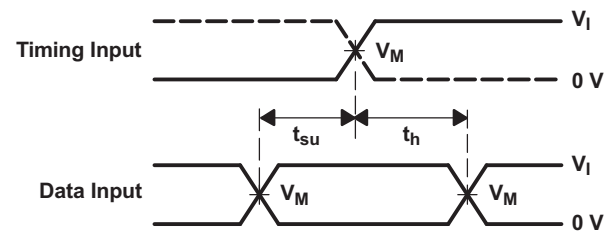
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

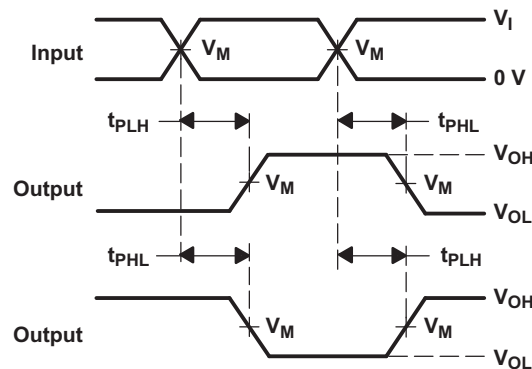
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



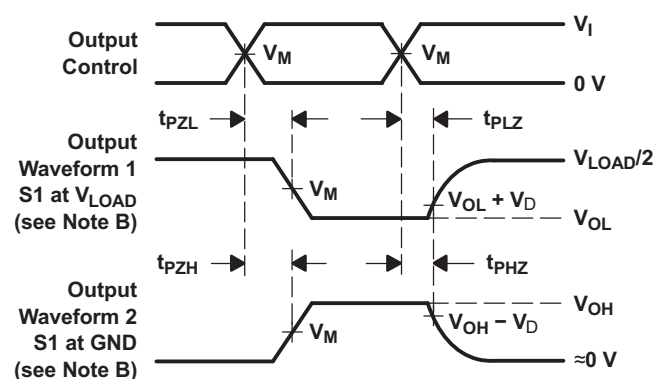
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

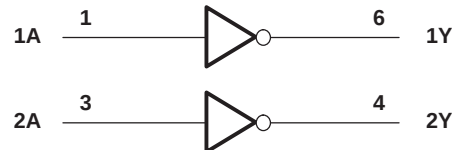
Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC2G04 contains two identical inverters that operate from 1.65-V to 5.5-V V_{CC} . Each inverter has a balanced output capable of outputting 32 mA at $V_{CC} = 4.5$ V. The overvoltage tolerant inputs allow for down-translation of up to 6.5 V, and the partial power-off feature ensures that the inputs and outputs can be any value from -0.5 V to 6.5 V when V_{CC} is 0 V

8.2 Functional Block Diagram



8.3 Feature Description

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package. This device supports 5-V V_{CC} operation and up to 5.5-V inputs. It has a low propagation delay of only 4.1 ns at 3.3 V.

Power consumption is low with only 10- μ A Max I_{CC} . Balanced drive output at 3.3 V can put out ± 24 -mA.

Typical output ground bounce is less than 0.8 V at 3.3-V V_{CC} and typical output undershoot is greater than 2 V at 3.3-V V_{CC} .

This device supports partial-power-down mode operation.

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74LVC2G04.

Table 1. Function Table (Each Inverter)

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC2G04 contains two logic inverters. It can be used in a wide variety of applications, with this being one example. Because this part has overvoltage tolerant inputs, it can be used for down translating logic levels. This example explains the method used for down-translating with this logic gate.

9.2 Typical Application

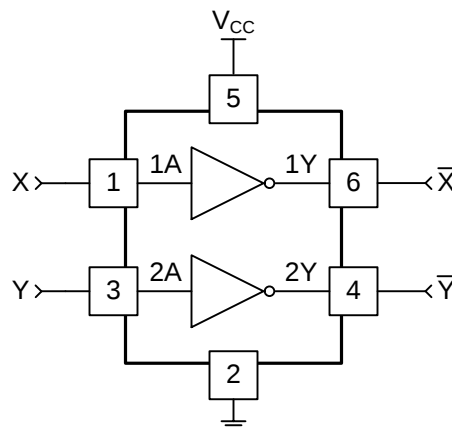


Figure 3. Application Schematic

9.2.1 Design Requirements

The inputs, X and Y in [Figure 3](#), to this device can be any value from -0.5 V to 6.5 V , according to [Absolute Maximum Ratings](#). Because the input limits are not associated with V_{CC} , down-translation is simple. The output voltage is selected with V_{CC} , and so long as the input logic voltage is larger than V_{IH} , found in [Recommended Operating Conditions](#), the output will trigger properly.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions

- For rise time and fall time specifications, see $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
- For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the [Recommended Operating Conditions](#) table at any valid V_{CC} .

2. Recommend Output Conditions

- Load currents should not exceed $(I_O \text{ max})$ per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
- Outputs should not be pulled above V_{CC} .

Typical Application (continued)

9.2.3 Application Curve

There is a slight delay from input to output in addition to the voltage change. [Figure 4](#) shows the expected output of the SN74LVC2G04 when an input is switched from 0 to 5 V and V_{CC} is set at 1.8 V. With V_{CC} set to 1.8 V, the output switches at 1.17 V ($0.65 \times V_{CC}$), and therefore the input can be anything from 1.18 V up to 6.5 V and the SN74LVC2G04 will work perfectly.

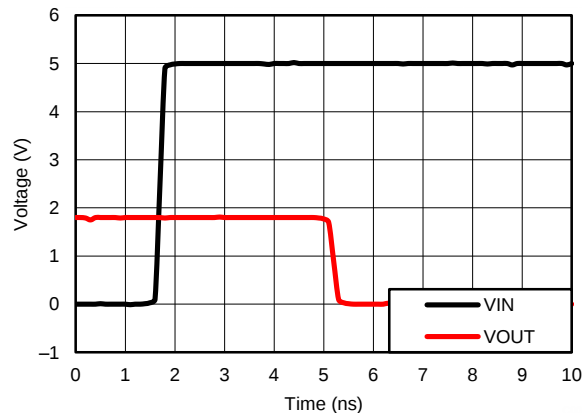


Figure 4. Simulated Voltage Down-Translation from 5-V Input to 1.8-V Output With $t_{pd} = 3.4$ ns.

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1- μ F capacitor is recommended and if there are multiple V_{CC} pins then a 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 5](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

11.2 Layout Example

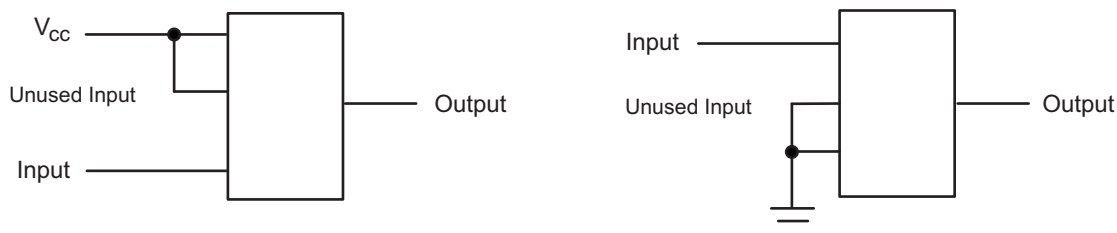


Figure 5. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G04DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(C045 ~ C04F ~ C04K ~ C04R)	Samples
SN74LVC2G04DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04F	Samples
SN74LVC2G04DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04F	Samples
SN74LVC2G04DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(C045 ~ C04F ~ C04K ~ C04R)	Samples
SN74LVC2G04DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04F	Samples
SN74LVC2G04DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5 ~ CCF ~ CCK ~ CCR)	Samples
SN74LVC2G04DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5 ~ CCF ~ CCK ~ CCR)	Samples
SN74LVC2G04DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5 ~ CCF ~ CCK ~ CCR)	Samples
SN74LVC2G04DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5 ~ CCF ~ CCK ~ CCR)	Samples
SN74LVC2G04DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5 ~ CCF ~ CCK ~ CCR)	Samples
SN74LVC2G04DRLR	ACTIVE	SOT-OTHER	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC7 ~ CCR)	Samples
SN74LVC2G04DRLRG4	ACTIVE	SOT-OTHER	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC7 ~ CCR)	Samples
SN74LVC2G04YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(CC7 ~ CCN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC2G04 :

- Enhanced Product: [SN74LVC2G04-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G04DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC2G04DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC2G04DBVTG4	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC2G04DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC2G04DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC2G04DCKT	SC70	DCK	6	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC2G04DCKT	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC2G04DRLR	SOT-OTHER	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC2G04DRLR	SOT-OTHER	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC2G04YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

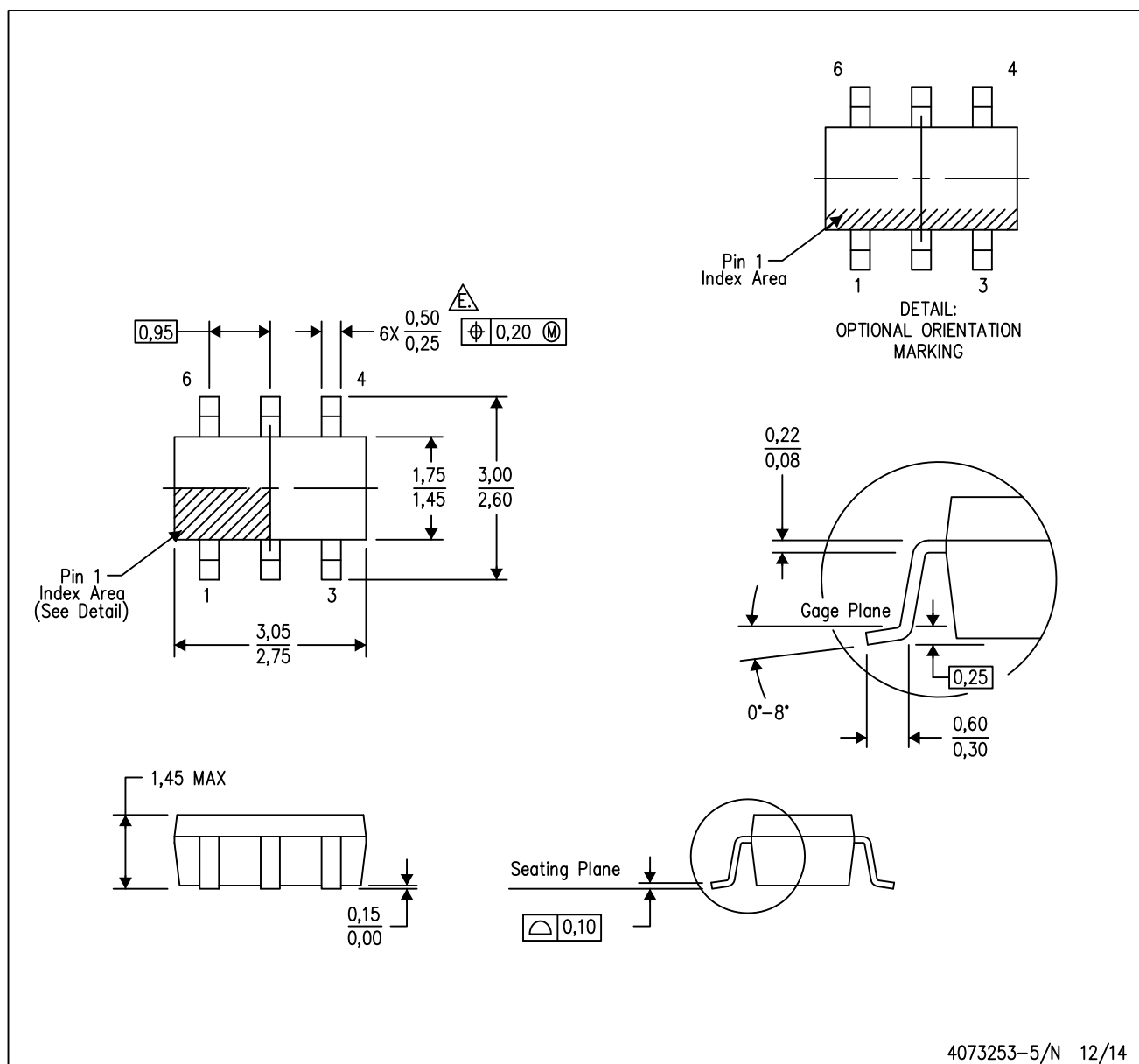


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G04DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC2G04DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC2G04DBVTG4	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC2G04DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC2G04DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC2G04DCKT	SC70	DCK	6	250	205.0	200.0	33.0
SN74LVC2G04DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC2G04DRLR	SOT-OTHER	DRL	6	4000	184.0	184.0	19.0
SN74LVC2G04DRLR	SOT-OTHER	DRL	6	4000	202.0	201.0	28.0
SN74LVC2G04YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

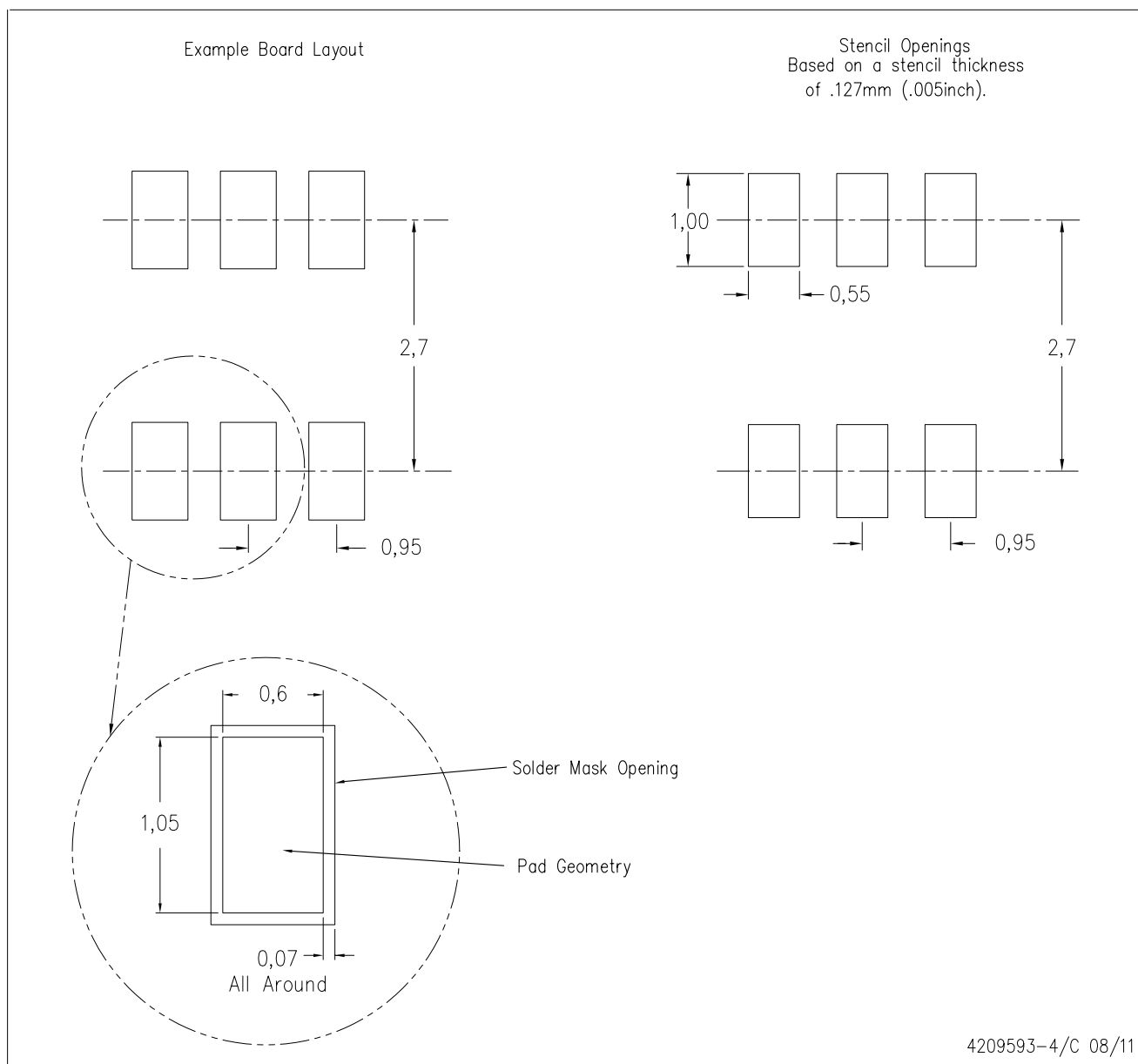


4073253-5/N 12/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
 - E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

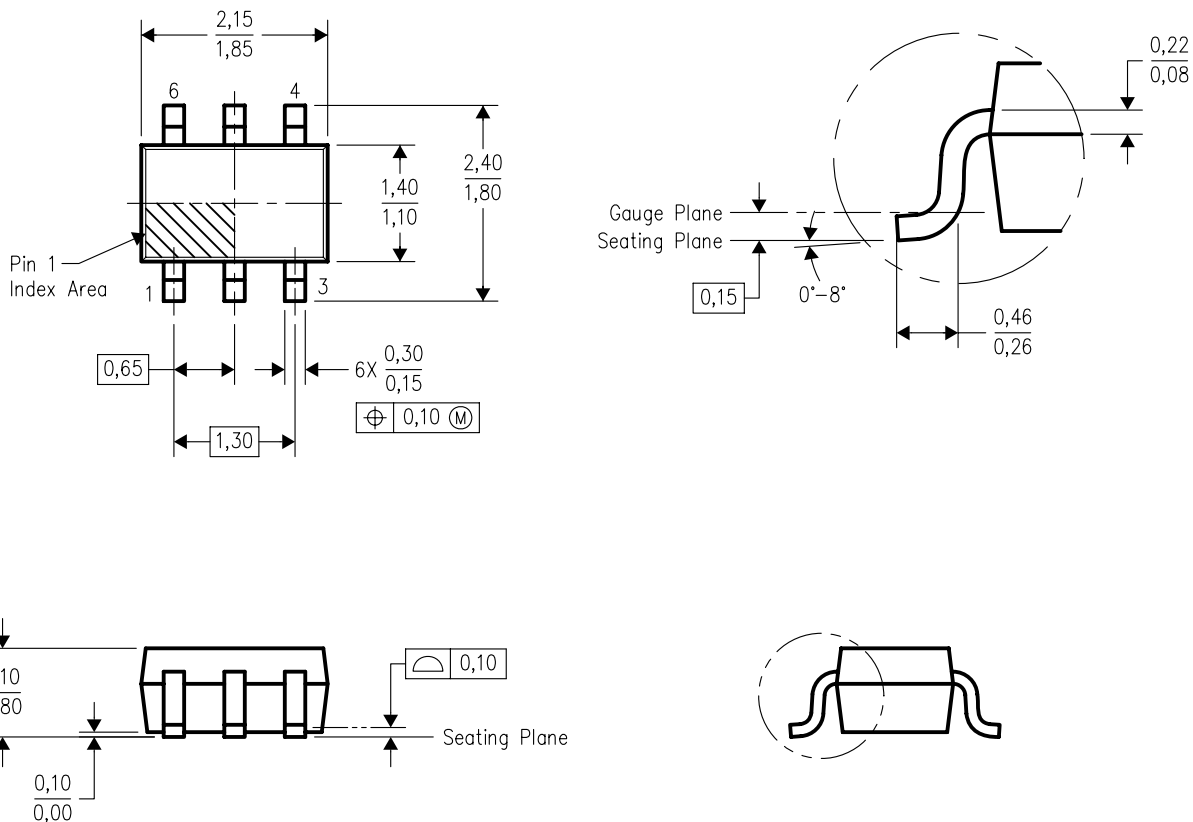
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

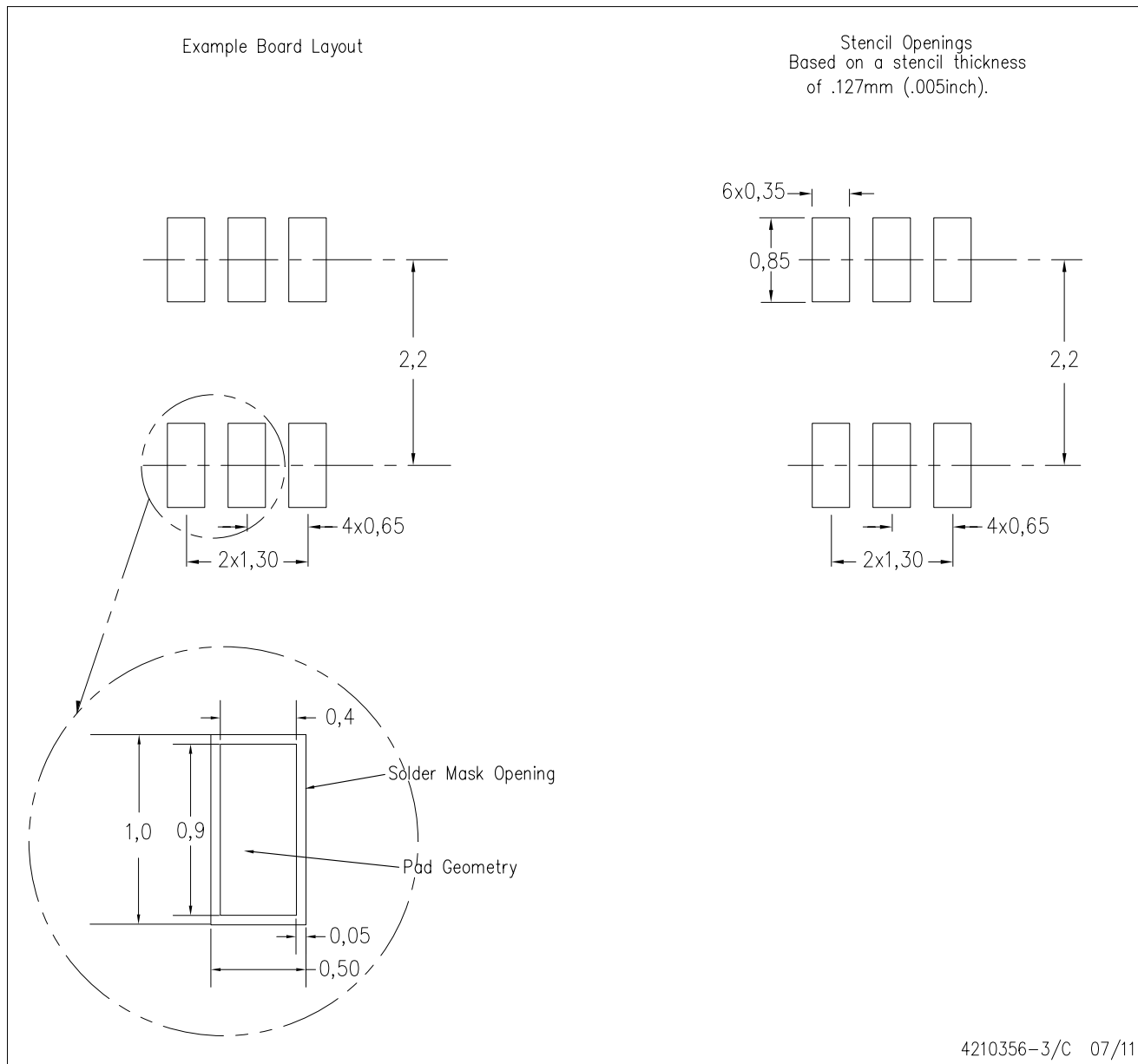


4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



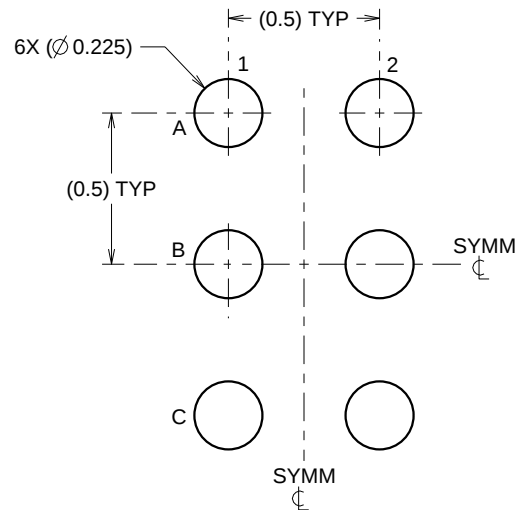
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

EXAMPLE BOARD LAYOUT

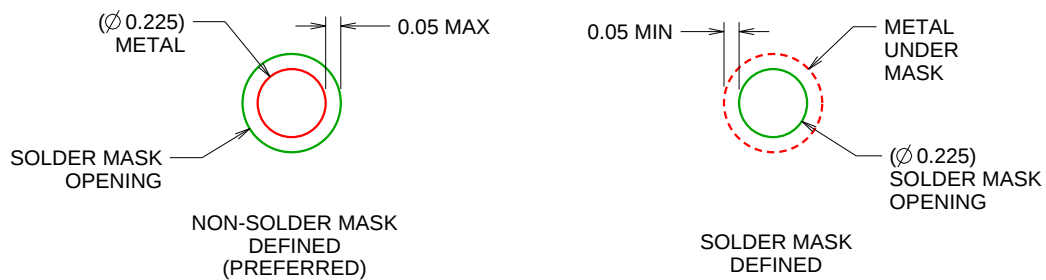
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

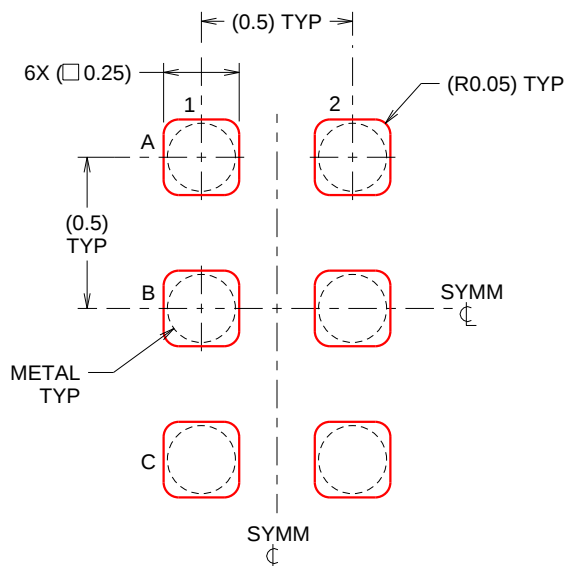
NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



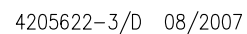
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PLASTIC SMALL OUTLINE



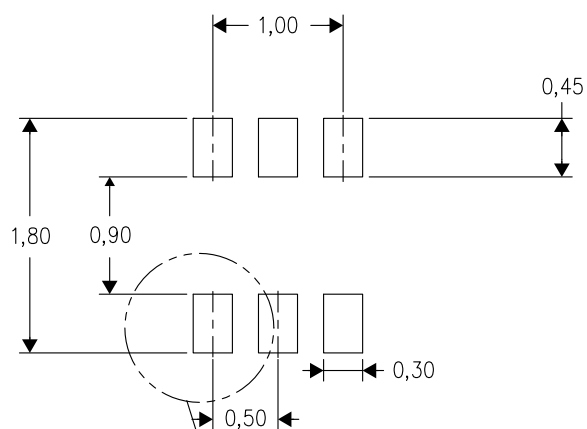
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
-  C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.

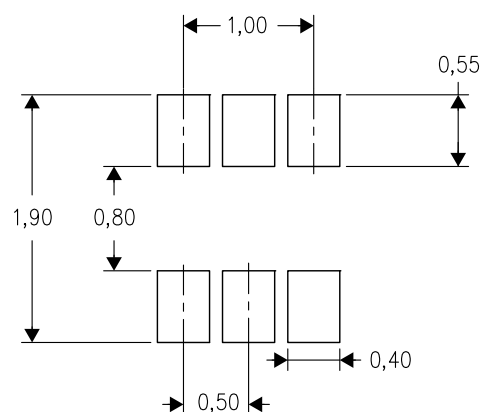
DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE

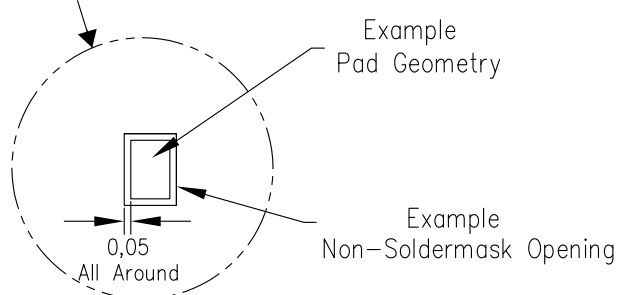
Example Board Layout



Example Stencil Design
(Note E)



Example
Non-Soldermask Defined Pad



Example
Pad Geometry

Example
Non-Soldermask Opening

4208207-3/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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