

High-Frequency Flash Programmable PLL Die with Spread Spectrum

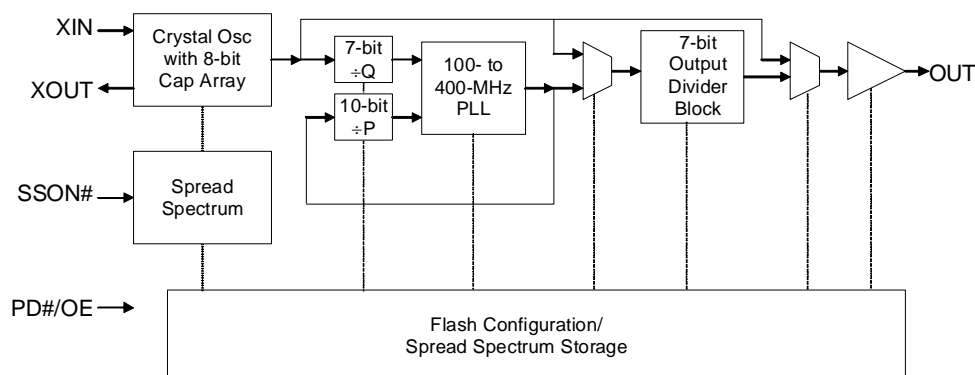
Features

- Flash programmable die for in-package programming of crystal oscillators
- High resolution phase-locked loop (PLL) with 10-bit multiplier and 7-bit divider
- Flash programmable capacitor tuning array
- Simple two-pin programming interface (excluding VDD and V_{SS} pins)
- On-chip oscillator used with external 25.1 MHz fundamental tuned crystal
- Flash programmable spread spectrum with spread percentages between $\pm 0.25\%$ and $\pm 2.00\%$
- Spread spectrum on/off function
- Operating frequency: 5 MHz to 170 MHz at 3.3 V $\pm 10\%$
- Seven-bit linear post divider with divide options from divide-by-2 to divide-by-127
- Programmable PD# or OE pin
- Programmable asynchronous or synchronous OE and PD# modes
- Low jitter output: < 200 ps (pk-pk) at 3.3 V $\pm 10\%$
- Controlled rise and fall times and output slew rate
- Software configuration support

Benefits

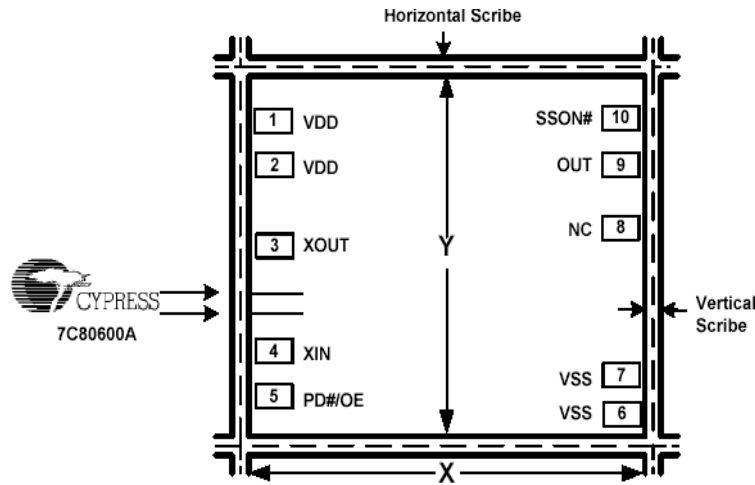
- Enables quick turnaround of custom oscillators and lowers inventory costs through stocking blank parts. In addition, the part may be Flash programmed up to 100 times. This reduces programming errors and provides an easy upgrade path for existing designs.
- Enables synthesis of highly accurate and stable output clock frequencies with zero or low PPM.
- Enables fine tuning of output clock frequency by adjusting the load capacitance of the crystal.
- Allows the device to go into standard 4 or 6-pin packages.
- Lowers cost of oscillator, because PLL may be programmed to a high frequency using a low frequency, low cost crystal.
- Provides various spread percentage.
- Provides the ability to enable or disable spread spectrum with an external pin.
- Provides flexibility in output configurations and testing.
- Enables low power operation or output enable function.
- Provides flexibility for system applications through selectable instantaneous or synchronous change in outputs.
- Suitable for most PC, consumer, and networking applications.
- Has lower EMI than oscillators.
- Easy to use software support for design entry.

Logic Block Diagram



Die Pad

Figure 1. Die Pad Diagram



Note

Active die size: X = 75.0 mils / 1907 μ m
 Y = 56.2 mils / 1428 μ m
 Scribe: X (vertical) = 3.4 mils / 86.2 μ m
 Y (horizontal) = 2.8 mils / 71 μ m
 Bond pad opening: 85 μ m x 85 μ m
 Pad pitch: 125 μ m x 125 μ m
 (pad center to pad center)
 Wafer thickness: 11 mils typical

Table 1. Die Pad Definitions [Pad coordinates are referenced from the center of the die (X = 0, Y = 0)]

Name	Die Pad	Description	X Coordinate	Y Coordinate
V _{DD}	1,2	Power supply	-843.612	597.849, 427.266
V _{SS}	6,7	Ground	883.743, 887.355	-563.304, -369.957
XIN	4	Crystal gate pin	-843.612	-1.806
XOUT	3	Crystal drain pin	-843.612	236.565
PD#/OE	5	Flash programmable to function as power down or output enable in normal operating mode. Weak pull up is enabled by default.	-843.612	-424.662
V _{PP}		Super voltage when going into programming mode.		
SDA		Data pin when going into and when in programming mode.		
SSON#	10	Active low spread spectrum control. Asserting LOW turns the internal modulation waveform on. Strong pull down is enabled by default. Pull down is disabled in power down mode.	834.183	589.848
SCL		Clock pin in programming mode. Must be double bonded to the OUT pad for pinouts not using the SSON# function. There is an internal pull down resistor on this pad.		
OUT	9	Clock output. There is an internal pull down resistor on this pad. Weak pull down is enabled by default. Default output is from the reference.	834.183	462.840
NC	8	No connect pin (do not connect this pad).	834.183	335.832

Functional Description

CY5057 is a Flash programmable, high accuracy, PLL-based die designed for the crystal oscillator market. It also contains spread spectrum circuitry that is enabled or disabled with an external pin. The die is integrated with a low cost 25.1 MHz fundamental tuned crystal in a 4 or 6-pin through hole or surface mount package. The oscillator devices may be stocked as blank parts and custom frequencies programmed in-package at the last stage before shipping. This enables faster manufacturing of custom and standard crystal oscillators without the need for dedicated and expensive crystals.

CY5057 contains an on-chip oscillator and unique oscillator tuning circuit for fine tuning the output frequency. The crystal C_{load} is selectively adjusted by programming a set of Flash memory bits. This feature is used to compensate for crystal variations or to obtain a more accurate synthesized frequency.

CY5057 uses a simple two-pin programming interface, excluding the V_{SS} and V_{DD} pins. Clock outputs are generated from 5 MHz to 170 MHz at $3.3\text{ V} \pm 10\%$ operating voltage. You can reprogram the entire Flash configuration multiple times to alter or reuse the programmed inventory.

CY5057 PLL die is designed for very high resolution. It has a 10-bit feedback counter multiplier and a 7-bit reference counter divider. This enables the synthesis of highly accurate and stable output clock frequencies with zero or low PPM error. The output of the PLL or the oscillator is further modified by a 7-bit linear post divider with a total of 126 divider options (2 to 127).

CY5057 also contains flexible power management controls. These parts include both power down mode ($PD\# = 0$) and output enable mode ($OE = 1$). The power down and output enable modes have an additional setting to determine timing (asynchronous or synchronous) with respect to the output signal.

Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enables CY5057 to have low jitter and accurate outputs. This makes it suitable for most PC, networking, and consumer applications.

CY5057 also has an additional spread spectrum feature that is disabled or enabled with an external pin. For more information, refer the section [Spread Spectrum](#).

Flash Configuration and Spread Spectrum Storage Block

Table 2 summarizes the features configurable by the Flash memory bits. Refer to “CY5057 Programming Specification” for programming details. The specification can be obtained from your Cypress factory representative.

Table 2. Flash Programmable Features

Adjust Frequency	Feedback counter value (P)
	Reference counter value (Q)
	Output divider selection
	Oscillator tuning (load capacitance values)
Oscillator direct output	
Power management mode (OE or PD#)	
Power management timing (synchronous or asynchronous)	
Spread spectrum	
Pull up and Pull down resistors	

PLL Output Frequency

CY5057 contains a high resolution PLL with a 10-bit multiplier and a 7-bit divider. The output frequency of the PLL is determined by the following equation:

$$F_{PLL} = \frac{2 \cdot (P_{BL} + 4) + P_o}{(Q_L + 2)} \cdot F_{REF} \quad \text{Equation (1)}$$

In this equation:

- Q_L is the loaded or programmed reference counter value (Q counter)
- P_{BL} is the loaded or programmed feedback counter value (P counter)
- P_o is the P offset bit (is only 0 or 1)

In spread spectrum mode, the time averaged P value is used to calculate the average frequency.

Power Management Features

CY5057 contains Flash programmable PD# (active LOW) and OE (active HIGH) functions. If power down mode is selected ($PD\# = 0$), the oscillator and PLL are placed in a low supply current standby mode and the output is tri-stated and weakly pulled low. The oscillator and PLL circuits must relock when the part leaves power down mode. If output enable mode is selected ($OE = 0$), the output is tri-stated and weakly pulled low. In this mode, the oscillator and PLL circuits continue to operate allowing a rapid return to normal operation when the output is enabled.

In addition, the PD# and OE modes may be programmed to occur synchronously or asynchronously with respect to the output signal. When the asynchronous setting is used, the power down or output disable occurs immediately (allowing for logic delays) irrespective of the position in the clock cycle. However, when the synchronous setting is used, the part waits for a falling edge at the output before power down or output enable signal is initiated. This prevents output glitches. In asynchronous or synchronous setting, the output is always enabled synchronously by waiting for the next falling edge of the output.

Spread Spectrum

CY5057 contains spread spectrum with Flash programmable spread percentage and modulation frequency. Center spread nonlinear “hershey kiss” modulation is obtained. Spread percentage is programmed to values between $\pm 0.25\%$ and $\pm 2.00\%$, in 0.25% intervals. Only one spread profile (for one specific percentage spread and for one output frequency) may be programmed into the device at a time.

CY5057 has a spread spectrum on and off function. The spread spectrum is enabled or disabled through an external pin. Timing this feature is explained in the section [Switching Waveforms](#) on page 7.

Figure 2. Crystal Oscillator Tuning Circuit

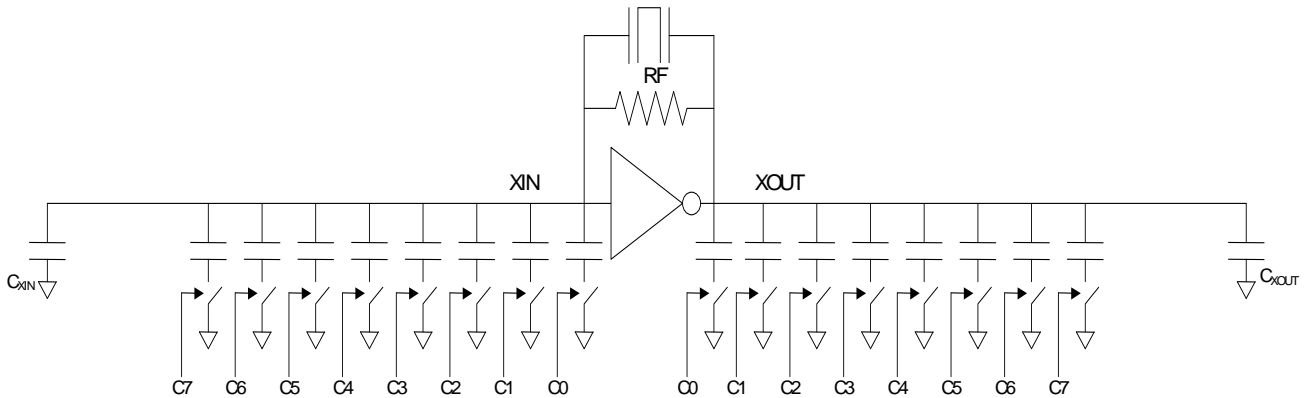


Table 3. Crystal Oscillator Tuning Cap Values

Bit ^[1]	Capacitance per Bit (pF)
C ₇ (MSB)	24.32
C ₆	12.16
C ₅	6.08
C ₄	3.04
C ₃	1.52
C ₂	0.76
C ₁	0.38
C ₀ (LSB)	0.19

Inkless Die Pick Map (DPM) Format

Cypress ships inkless wafers to customers with an accompanying die pick map, which is used to determine the good die for assembly and programming. Customers can also access individual DPM files at their convenience through ftp.cypress.com with a valid user account login and password. Contact your local Cypress Field Application Engineer (FAE) or sales representative for a customer FTP account. The DPM files are named using the fab lot number and wafer number scribed on the wafer. The DPM files are transferred to the FTP account of the customer when the factory ships out the wafers against their purchase order (PO).

Note

1. C_{XIN}, C_{XOUT}, and parasitic capacitance due to fixture and package must be included when calculating the total capacitance.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply voltage	-0.5 to 7.0 V
Input voltage	-0.5 V to $V_{DD} + 0.5$
Storage temperature (noncondensing)	-55°C to 125°C
Junction temperature	-40°C to 125°C

Data retention at $T_j = 125^\circ\text{C}$	> 10 years
Maximum non volatile programming cycles	100
Static discharge voltage	≥ 2000 V (per MIL-STD-883, method 3015)
Output (pad 9) sink or sources current	20 mA maximum

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage (3.3 V)	3.0	3.6	V
$T_{AJ}^{[2]}$	Operating temperature, junction	-40	100	°C
C_{LC}	Maximum capacitive load on the output (CMOS levels spec) $V_{DD} = 3.0$ V to 3.6 V, output frequency = 5 MHz to 170 MHz	-	15	pF
X_{REF}	Reference frequency with spread spectrum disabled. Fundamental tuned crystals only	25.1	25.1	MHz
C_{in}	Input capacitance (except crystal pins)	-	7	pF
C_{XIN}	Crystal input capacitance (all internal caps off)	10	14	pF
C_{Xout}	Crystal output capacitance (all internal caps off)	10	14	pF
T_{PSRT}	Power up time for all V_{DD} s to reach minimum specified voltage (power ramps must be monotonic)	0.005	500	ms

DC Electrical Characteristics ($T_j = -40$ to 100°C)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input low voltage PD#/OE and SSON# pins	$V_{DD} = 3.0$ V–3.6 V	-	$0.3 \cdot V_{DD}$	V
V_{IH}	Input high voltage PD#/OE and SSON# pins	$V_{DD} = 3.0$ V–3.6 V	$0.7 \cdot V_{DD}$	-	V
V_{OL}	Output low voltage, OUT pin	$V_{DD} = 3.0$ V–3.6 V, $I_{OL} = 8$ mA	-	0.4	V
V_{OH}	Output high voltage, CMOS levels	$V_{DD} = 3.0$ V–3.6 V, $I_{OH} = -8$ mA	$V_{DD} - 0.4$	-	V
I_{ILPDOE}	Input low current, PD#/OE pin	$V_{IN} = V_{SS}$ (Internal pull up = 3 M Ω typical)	-	10	μA
I_{IHPDOE}	Input high current, PD#/OE pin	$V_{IN} = V_{DD}$ (Internal pull up = 100 k Ω typical)	-	10	μA
I_{ILSR}	Input low current, SSON# pin	$V_{IN} = V_{SS}$ (Internal pull down = 100 k Ω typical)	-	10	μA
I_{IHSR}	Input high current, SSON# pin	$V_{IN} = V_{DD}$ (Internal pull down = 100 k Ω typical)	-	50	μA
I_{DD}	Supply current	No load, $V_{DD} = 3.0$ V–3.6 V, $f_{out} = 170$ MHz	-	50	mA
I_{OZ}	Output leakage current, OUT pin	$V_{DD} = 3.0$ V–3.6 V, output disabled with OE	-	50	μA
I_{PD}	Standby current	$V_{DD} = 3.0$ V–3.6 V, device powered down with PD#	-	50	μA
R_{UP}	Pull up resistor on PD#/OE pin	$V_{DD} = 3.0$ V–3.6 V, measured at $V_{IN} = V_{SS}$ $V_{DD} = 3.0$ V–3.6 V, measured at $V_{IN} = 0.7 V_{DD}$	1 80	6 150	M Ω k Ω
R_{DN}	Pull down resistor on SSON# and OUT pins	$V_{DD} = 3.0$ V–3.6 V, measured at $V_{IN} = 0.5 V_{DD}$	80	150	k Ω
R_f	Crystal feedback resistor	$V_{DD} = 3.0$ V–3.6 V, measured at $X_{IN} = 0$	100	-	k Ω

AC Electrical Characteristics ($T_j = -40$ to 100°C)

Parameter ^[2]	Description	Test Conditions	Min	Max	Unit
F_{out}	Output frequency	$V_{DD} = 3.0\text{ V} - 3.6\text{ V}$, $C_L = 15\text{ pF}$	5	170	MHz
t_r	OUT rise time	$V_{DD} = 3.0\text{ V} - 3.6\text{ V}$, 20% to 80% V_{DD} , $C_L = 15\text{ pF}$	–	2.7	ns
t_f	OUT fall time	$V_{DD} = 3.0\text{ V} - 3.6\text{ V}$, 80% to 20% V_{DD} , $C_L = 15\text{ pF}$	–	2.7	ns
DC	OUT duty cycle	Divider output, measured at $V_{DD}/2$	45	55	%
		Crystal direct output, measured at $V_{DD}/2$	40	60	%
t_{j1}	Peak-to-peak period jitter	$F_{out} \geq 133\text{ MHz}$, $V_{DD}/2$, SS off	–	200	ps
		$25\text{ MHz} \leq F_{out} < 133\text{ MHz}$, $V_{DD}/2$, SS off		400	ps
		$F_{out} < 25\text{ MHz}$, $V_{DD}/2$, SS off		1% of $1/F_{out}$	s
t_{j2}	Cycle-to-cycle jitter	$F_{out} > 133\text{ MHz}$, $V_{DD}/2$, SS on	–	200	ps
		$25\text{ MHz} \leq F_{out} < 133\text{ MHz}$, $V_{DD}/2$, SS on		400	ps
		$F_{out} < 25\text{ MHz}$, $V_{DD}/2$, SS on		1% of $1/F_{out}$	s
F_{MOD}	Modulation frequency		30	33	kHz
DL	Crystal drive level	Measured at 25.1 MHz, with crystal ESR = 20Ω , cap setting = hex16, DL = program code [1,0]	–	540	μW
–R	Negative resistance	Measured at 25.1 MHz, cap setting = hex 3F	–	–200	Ω

Timing Parameters

Parameter ^[2]	Description	Min	Max	Unit
T_{SSON1}	Time from steady state spread to steady state nonspread	--	600	μs
T_{SSON2}	Time from steady state non spread to steady state spread	--	100	μs
T_{SSON3}	Minimum SSON# pulse width (positive or negative)	250	–	μs
T_{MOD}	Spread spectrum modulation period	30	33.33	μs
$T_{STP,SYNC}$	Time from falling edge on PD# to stopped outputs, synchronous mode, $T = 1/F_{out}$	--	$1.5T + 350$	ns
$T_{STP,ASYNC}$	Time from falling edge on PD# to stopped outputs, asynchronous mode	--	350	ns
$T_{PU,SYNC}$	Time from rising edge on PD# to outputs at valid frequency, synchronous mode	--	3	ms
$T_{PU,ASYNC}$	Time from rising edge on PD# to outputs at valid frequency, asynchronous mode	--	3	ms
$T_{PXZ,SYNC}$	Time from falling edge on OE to high impedance outputs, synchronous mode, $T = 1/F_{out}$	--	$1.5T + 350$	ns
$T_{PXZ,ASYNC}$	Time from falling edge on OE to high impedance outputs, asynchronous mode	--	350	ns
$T_{PZX,SYNC}$	Time from rising edge on OE to running outputs, synchronous mode, $T = 1/F_{out}$	--	$1.5T + 350$	ns
$T_{PZX,ASYNC}$	Time from rising edge on OE to running outputs, asynchronous mode	--	350	ns
T_{LOCK}	PLL lock time (from 0.9 V_{DD} to valid output clock frequency)	--	10	ms

Note

- In Cypress standard TSSOP packages with external crystal.

Switching Waveforms

Figure 3. Duty Cycle Timing (dc)

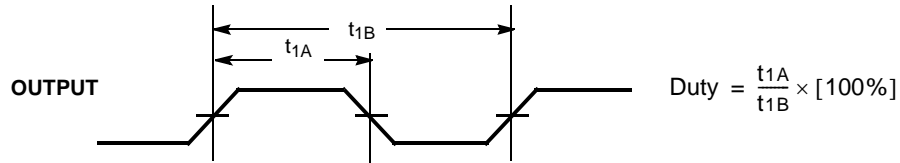


Figure 4. Output Rise/Fall Time

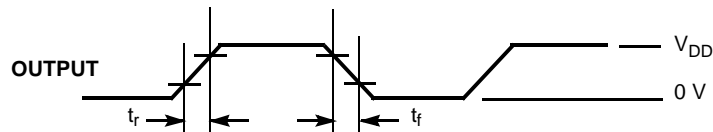


Figure 5. Power Down Timing (Synchronous and Asynchronous Modes)

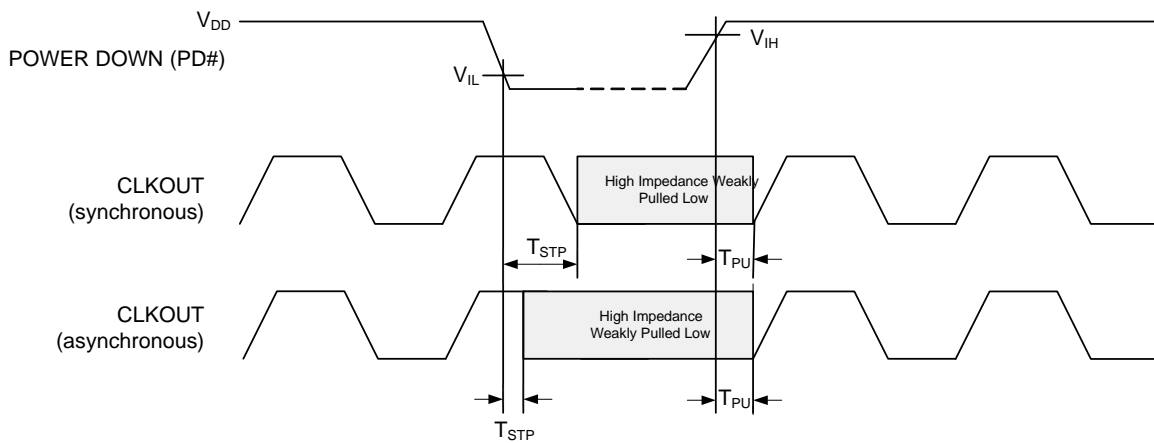


Figure 6. Output Enable Timing (Synchronous and Asynchronous Modes)

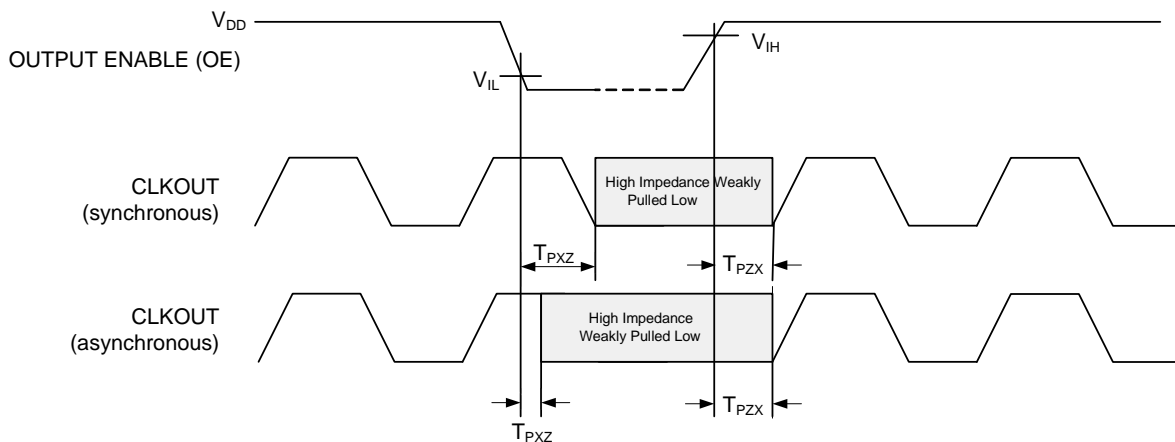


Figure 7. Power Up Timing

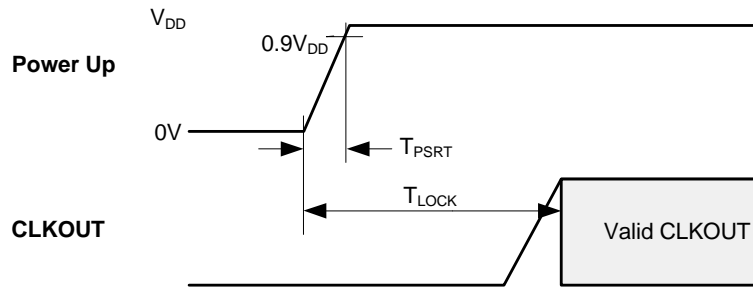
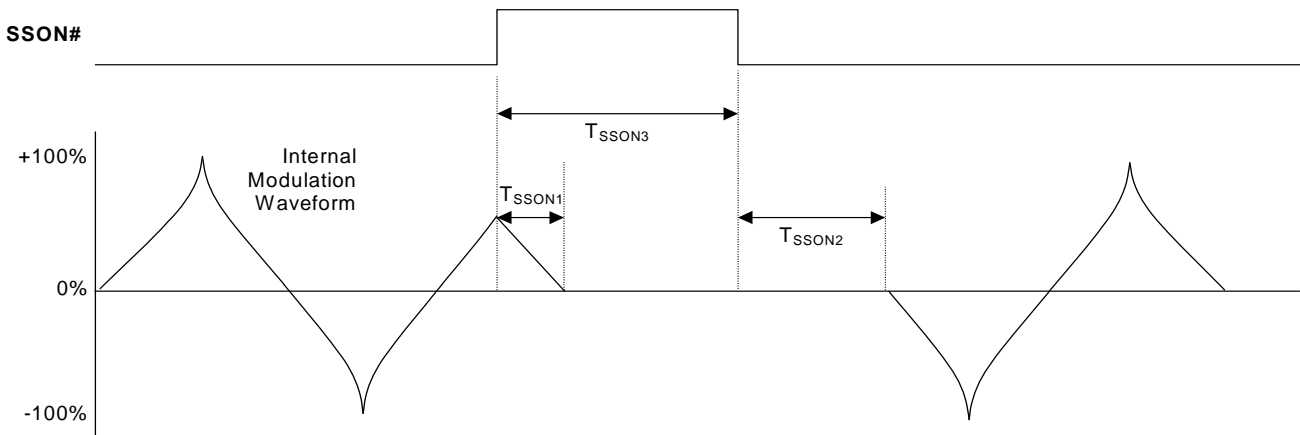


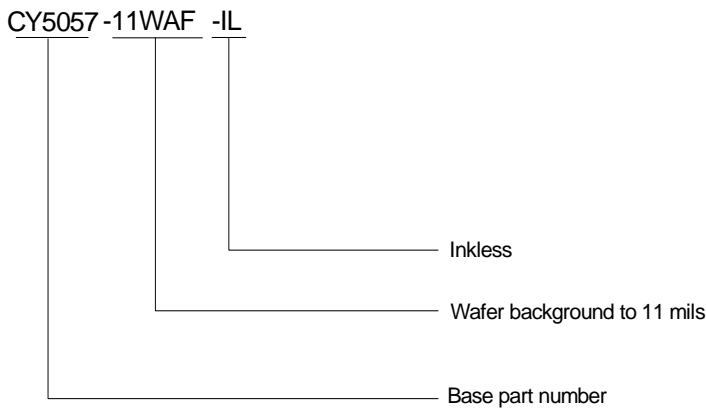
Figure 8. Spread Spectrum On and OFF Timing



Ordering Information

Ordering Code	Status	Type	Operating Range
CY5057-11WAF-IL	Active	Inkless wafer (background to 11 mils)	-40 °C to 100 °C

Ordering Code Definitions



Acronyms

Acronym	Description
CLKOUT	Clock output
CMOS	Complementary metal oxide semiconductor
DPM	Die pick map
EMI	Electromagnetic interference
EPROM	Erasable programmable read only memory
FAE	Field Application Engineer
FTP	File transfer protocol
OE	Output enable
PAL	Phase alternate line
PD	Power down
PLL	Phase locked loop
PPM	Parts per million
TSSOP	Thin shrunk small outline package
TTL	Transistor transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
mA	milli Amperes
mm	milli meters
ms	milli seconds
ns	nano seconds
ps	pico seconds
ppm	parts per million
Ω	ohms
kΩ	kilo ohms
MHz	Mega Hertz
MΩ	Mega Ohms
μA	micro Amperes
μF	micro Farads
μm	micro meters
pF	pico Farads
pp	peak-to-peak
V	Volts
%	percent

Document History Page

Document Title: CY5057 High-Frequency Flash Programmable PLL Die with Spread Spectrum Document Number: 38-07363				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	112486	CKN	See ECN	New data sheet
*A	121373	CKN	See ECN	Added scribe lines to die pad description Added wafer thickness to die pad description Added X and Y coordinates to die pad description Removed list of discrete frequencies and discrete spread percentages Removed references to discrete frequencies and profile tables Replaced with description of software for full programmability Operating frequency changed to 5 MHz–170 MHz Removed C0 and C1 from crystal oscillator tuning circuit; renumbered other capacitors Changed maximum junction temperature to 125°C Changed PDOE internal pull up value to 1–6 Mohm when $V_{IN} = V_{SS}$ Changed ILLPDOE to 10 μ A Changed Rf spec to 100 kohm, at condition $X_{IN} = 0$ Change DL spec to 540 μ W, at condition cap setting = hex16, DL=10 Added power up timing diagram separate from power down timing diagram Removed die information table
*B	127414	RGL	See ECN	Added –11 and other details to ordering Information Added t_{PU} details to operating conditions Changed max T_{SSON1} value to 600 in timing parameters table Changed parameter T_{PU} under timing parameters to T_{LOCK} with the description “PLL lock time” Altered minimum and maximum values in power up timing figure
*C	2143928	FGA/PYRS	See ECN	Modified power down timing diagram Changed power up timing from min. of 50 μ s to 5 μ s Added output sink/source current specification in the absolute max ratings Change cap array from 10 to 8-bit Add MSB and LSB in the crystal oscillator tuning cap values table Fixed power up timing diagram Added -R cap setting value FF Added Inkless die information before Absolute Maximum Ratings Added new part number (CY5057-11WAF-IL) with note
*D	2541797	AESA	07/24/08	Updated template. Added Note “Not recommended for new designs.” Added part number CY5057K-11WAF-IL in ordering information table.
*E	2600816	KVM/AESA	11/04/08	Updated to match data sheet labeled “Rev *C November 16, 2004” (added logo and die number to die drawing; added pull up & pull down resistors to features table; revised –R spec and conditions; added missing labels to waveform drawings) Removed CY5057K-11WAF-IL from ordering information table. Updated die dimensions (page 2) with 29 mil thickness; corrected scribe variables
*F	2621902	KVM/AESA	12/15/2008	Corrected typos on p. 1 (spread amount) & p. 5 (V_{IL} & V_{IH} test conditions). Connected text frames.
*G	2897373	CXQ	03/22/10	Removed part number CY5057-29WAF-IL from Ordering information table. Updated copyright section.
*H	3068367	CXQ	10/21/2010	Removed CY5057-11WAF part from Ordering Information . Added Ordering Code Definitions .
*I	3201346	CXQ	03/21/2011	Sunset review. No material changes to document. Fixed various typos. Included Acronyms and units tables. Updated template and styles.

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