

FEATURES

- Stable in Gain $A_V \geq 2$ ($A_V = -1$)
- 200MHz Gain Bandwidth Product
- 30V/ μ s Slew Rate
- Settling Time: 800ns (150 μ V, 10V Step)
- Specified at ± 5 V and ± 15 V Supplies
- Maximum Input Offset Voltage: 125 μ V
- Low Distortion: -96.5 dB for 100kHz, 10V_{P-P}
- Maximum Input Offset Voltage Drift: 3 μ V/ $^{\circ}$ C
- Maximum Inverting Input Bias Current: 10nA
- Minimum DC Gain: 300V/mV
- Minimum Output Swing into 2k: ± 12.8 V
- Input Noise Voltage: 5nV/ $\sqrt{\text{Hz}}$
- Input Noise Current: 0.6pA/ $\sqrt{\text{Hz}}$
- Total Input Noise Optimized for $1\text{k}\Omega < R_S < 20\text{k}\Omega$
- Available in 8-Lead Plastic SO and 12-Lead (4mm $\times$ 4mm) DFN Packages

APPLICATIONS

- Precision Instrumentation
- High Accuracy Data Acquisition Systems
- 16-Bit DAC Current-to-Voltage Converter
- ADC Buffer
- Low Distortion Active Filters
- Photodiode Amplifiers

DESCRIPTION

The LT $^{\circ}$ 1469-2 is a dual, precision high speed operational amplifier with 16-bit accuracy, decompensated to be stable in a gain of 2 or greater. The combination of precision and AC performance makes the LT1469-2 the optimum choice for high accuracy applications such as DAC current-to-voltage conversion and ADC buffers. The initial accuracy and drift characteristics of the input offset voltage and inverting input bias current are tailored for inverting applications.

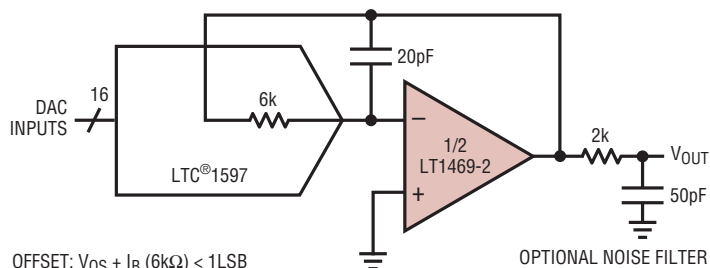
The 200MHz gain bandwidth ensures high open-loop gain at frequency for reducing distortion. In noninverting applications such as an ADC buffer, the low distortion and DC accuracy allow full 16-bit AC and DC performance. The high slew rate of the LT1469-2 improves large-signal performance in applications such as active filters and instrumentation amplifiers compared to other precision op amps.

The LT1469-2 is specified on power supply voltages of ± 5 V and ± 15 V and from -40°C to 85°C . It is available in an 8-lead SOIC package and a space saving 4mm $\times$ 4mm leadless package. For a unity-gain stable op amp with same DC performance, see the LT1469 datasheet.

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TYPICAL APPLICATION

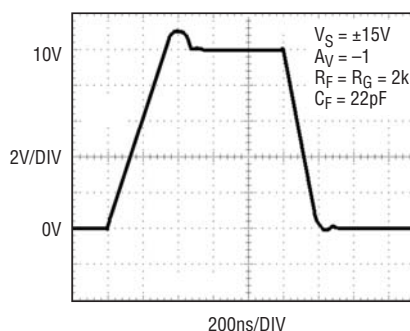
16-Bit DAC I-to-V Converter



OFFSET: $V_{OS} + I_B (6\text{k}\Omega) < 1\text{LSB}$
 SETTLING TIME TO 150 μ V = 1.6 μ s
 SETTLING LIMITED BY 6k AND 20pF TO COMPENSATE DAC OUTPUT CAPACITANCE

14692 TA01a

Large-Signal Transient, $A_V = -1$



14692 TA02

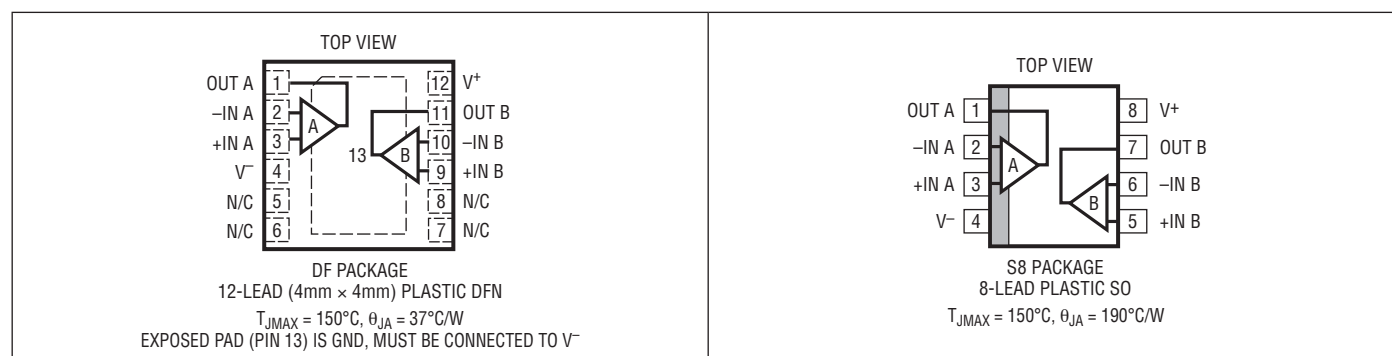
LT1469-2

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-).....36V
 Input Current (Note 2)..... $\pm 10\text{mA}$
 Output Short-Circuit Duration (Note 3) Indefinite
 Operating Temperature Range (Note 4).... -40°C to 85°C

Specified Temperature Range (Note 5) -40°C to 85°C
 Maximum Junction Temperature..... 150°C
 Storage Temperature Range..... -65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1469CS8-2#PBF	LT1469CS8-2#TRPBF	14692	8-Lead Plastic Small Outline	0°C to 70°C
LT1469IS8-2#PBF	LT1469IS8-2#TRPBF	14692	8-Lead Plastic Small Outline	-40°C to 85°C
LT1469ACDF-2#PBF	LT1469ACDF-2#TRPBF	14692	12-Lead (4mm × 4mm) Plastic DFN	0°C to 70°C
LT1469AIDF-2#PBF	LT1469AIDF-2#TRPBF	14692	12-Lead (4mm × 4mm) Plastic DFN	-40°C to 85°C
LT1469CDF-2#PBF	LT1469CDF-2#TRPBF	14692	12-Lead (4mm × 4mm) Plastic DFN	0°C to 70°C
LT1469IDF-2#PBF	LT1469IDF-2#TRPBF	14692	12-Lead (4mm × 4mm) Plastic DFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8 Package	$\pm 15\text{V}$		50	125	μV
			$\pm 5\text{V}$		50	200	μV
		LT1469A, DF Package	$\pm 15\text{V}$		50	125	μV
			$\pm 5\text{V}$		50	200	μV
		LT1469, DF Package	$\pm 15\text{V}$		100	225	μV
			$\pm 5\text{V}$		150	300	μV
I_{OS}	Input Offset Current		$\pm 5\text{V}$ to $\pm 15\text{V}$		13	± 50	nA

14692f

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
I_{B-}	Inverting Input Bias Current		$\pm 5\text{V to } \pm 15\text{V}$	3	± 10		nA
I_{B+}	Noninverting Input Bias Current		$\pm 5\text{V to } \pm 15\text{V}$	-10	± 40		nA
	Input Noise Voltage	0.1Hz to 10Hz	$\pm 5\text{V to } \pm 15\text{V}$	0.3			μV_{P-P}
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$	$\pm 5\text{V to } \pm 15\text{V}$	5			$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$	$\pm 5\text{V to } \pm 15\text{V}$	0.6			$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Common Mode, $V_{CM} = \pm 12.5\text{V}$ Differential	$\pm 15\text{V}$ $\pm 15\text{V}$	100 50	240 150		$\text{M}\Omega$ $\text{k}\Omega$
C_{IN}	Input Capacitance		$\pm 15\text{V}$	4			pF
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR	$\pm 15\text{V}$ $\pm 5\text{V}$	12.5 2.5	13.5 3.6		V V
	Input Voltage Range (Negative)	Guaranteed by CMRR	$\pm 15\text{V}$ $\pm 5\text{V}$		-14.3 -4.4	-12.5 -2.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12.5\text{V}$ $V_{CM} = \pm 2.5\text{V}$	$\pm 15\text{V}$ $\pm 5\text{V}$	96 96	110 112		dB dB
	Minimum Supply Voltage	Guaranteed by PSRR			± 2.5	± 4.5	V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V to } \pm 15\text{V}$		100	112		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12.5\text{V}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	300	2000		V/mV
		$V_{OUT} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	300	2000		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 10\text{k}$	$\pm 5\text{V}$	200	8000		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	200	8000		V/mV
V_{OUT}	Maximum Output Swing	$R_L = 10\text{k}$, 1mV Overdrive	$\pm 15\text{V}$	± 13.0	± 13.6		V
		$R_L = 2\text{k}$, 1mV Overdrive	$\pm 15\text{V}$	± 12.8	± 13.5		V
		$R_L = 10\text{k}$, 1mV Overdrive	$\pm 5\text{V}$	± 3.0	± 3.7		V
		$R_L = 2\text{k}$, 1mV Overdrive	$\pm 5\text{V}$	± 2.8	± 3.6		V
I_{OUT}	Maximum Output Current	$V_{OUT} = \pm 12.5\text{V}$, 1mV Overdrive	$\pm 15\text{V}$	± 15	± 22		mA
		$V_{OUT} = \pm 2.5\text{V}$, 1mV Overdrive	$\pm 5\text{V}$	± 15	± 22		mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0\text{V}$, 0.2V Overdrive (Note 3)	$\pm 15\text{V}$	± 25	± 40		mA
SR	Slew Rate	$R_L = 2\text{k}$ (Note 6)	$\pm 15\text{V}$	20	30		V/ μs
			$\pm 5\text{V}$	15	22		V/ μs
FPBW	Full-Power Bandwidth	10V Peak, (Note 7)	$\pm 15\text{V}$		475		kHz
		3V Peak, (Note 7)	$\pm 5\text{V}$		1160		kHz
GBW	Gain Bandwidth Product	$f = 100\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	140	200		MHz
			$\pm 5\text{V}$	130	190		MHz
t_s	Settling Time	10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		650		ns
		10V Step, 150 μV , $A_V = -1$	$\pm 15\text{V}$		800		ns
R_{OUT}	Output Resistance	$A_V = -1$, $f = 100\text{kHz}$	$\pm 15\text{V}$		0.02		Ω
	Channel Separation	$V_{OUT} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	100	130		dB
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	100	130		dB
I_S	Supply Current	Per Amplifier	$\pm 15\text{V}$	4.1	5.2		mA
			$\pm 5\text{V}$	3.8	5		mA
ΔV_{OS}	Input Offset Voltage Match		$\pm 15\text{V}$	30	225		μV
			$\pm 5\text{V}$	50	350		μV
ΔI_{B-}	Inverting Input Bias Current Match		$\pm 5\text{V to } \pm 15\text{V}$	2	18		nA
ΔI_{B+}	Noninverting Input Bias Current Match		$\pm 5\text{V to } \pm 15\text{V}$	5	78		nA
ΔCMRR	Common Mode Rejection Match	$V_{CM} = \pm 12.5\text{V}$ (Note 9)	$\pm 15\text{V}$	93	113		dB
		$V_{CM} = \pm 2.5\text{V}$ (Note 9)	$\pm 5\text{V}$	93	115		dB
ΔPSRR	Power Supply Rejection Match	$V_S = \pm 4.5\text{V to } \pm 15\text{V}$ (Note 9)		97	115		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. $V_{\text{CM}} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8 Package	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●			350 350	μV μV
		LT1469A, DF Package	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●			225 275	μV μV
		LT1469, DF Package	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●			450 450	μV μV
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift	(Note 8)	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●		1 1	5 3	$\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 80	nA
$\Delta I_{\text{OS}}/\Delta T$	Input Offset Current Drift	(Note 8)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●		60		$\text{pA}/^{\circ}\text{C}$
$I_{\text{B-}}$	Inverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 20	nA
$\Delta I_{\text{B-}}/\Delta T$	Inverting Input Bias Current Drift	(Note 8)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●		40		$\text{pA}/^{\circ}\text{C}$
$I_{\text{B+}}$	Noninverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 60	nA
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●	12.5 2.5			V V
	Input Voltage Range (Negative)	Guaranteed by CMRR	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●			-12.5 -2.5	V V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = \pm 12.5\text{V}$	$\pm 15\text{V}$	●	94			dB
		$V_{\text{CM}} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	94			dB
	Minimum Supply Voltage	Guaranteed by PSRR		●			± 4.5	V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$		●	95			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	●	100			V/mV
		$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	100			V/mV
		$V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 10\text{k}$	$\pm 5\text{V}$	●	100			V/mV
		$V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	●	100			V/mV
V_{OUT}	Maximum Output Swing	$R_L = 10\text{k}$, 1mV Overdrive	$\pm 15\text{V}$	●	± 12.9			V
		$R_L = 2\text{k}$, 1mV Overdrive	$\pm 15\text{V}$	●	± 12.7			V
		$R_L = 10\text{k}$, 1mV Overdrive	$\pm 5\text{V}$	●	± 2.9			V
		$R_L = 2\text{k}$, 1mV Overdrive	$\pm 5\text{V}$	●	± 2.7			V
I_{OUT}	Maximum Output Current	$V_{\text{OUT}} = \pm 12.5\text{V}$, 1mV Overdrive	$\pm 15\text{V}$	●	± 12.5			mA
		$V_{\text{OUT}} = \pm 2.5\text{V}$, 1mV Overdrive	$\pm 5\text{V}$	●	± 12.5			mA
I_{SC}	Output Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, 0.2V Overdrive (Note 3)	$\pm 15\text{V}$	●	± 17			mA
SR	Slew Rate	$R_L = 2\text{k}$ (Note 6)	$\pm 15\text{V}$	●	18			V/ μs
			$\pm 5\text{V}$	●	13			V/ μs
GBW	Gain Bandwidth Product	$f = 100\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	130	200		MHz
			$\pm 5\text{V}$	●	120	190		MHz
	Channel Separation	$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 2\text{k}$ $V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	98			dB
			$\pm 5\text{V}$	●	98			dB
I_S	Supply Current	Per Amplifier	$\pm 15\text{V}$	●			6.5	mA
			$\pm 5\text{V}$	●			6.3	mA
ΔV_{OS}	Input Offset Voltage Match		$\pm 15\text{V}$ $\pm 5\text{V}$	● ●			600 600	μV μV
$\Delta I_{\text{B-}}$	Inverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			38	nA
$\Delta I_{\text{B+}}$	Noninverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			118	nA
ΔCMRR	Common Mode Rejection Match	$V_{\text{CM}} = \pm 12.5\text{V}$ (Note 9)	$\pm 15\text{V}$	●	91			dB
		$V_{\text{CM}} = \pm 2.5\text{V}$ (Note 9)	$\pm 5\text{V}$	●	91			dB
ΔPSRR	Power Supply Rejection Match	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$ (Note 9)		●	92			dB

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{\text{CM}} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8 Package	$\pm 15\text{V}$	●			500	μV
			$\pm 5\text{V}$	●			500	μV
		LT1469A, DF Package	$\pm 15\text{V}$	●			300	μV
			$\pm 5\text{V}$	●			350	μV
		LT1469, DF Package	$\pm 15\text{V}$	●			600	μV
			$\pm 5\text{V}$	●			600	μV
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift	(Note 8)	$\pm 15\text{V}$	●	1	6		$\mu\text{V}/^{\circ}\text{C}$
			$\pm 5\text{V}$	●	1	5		$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 120	nA
$\Delta I_{\text{OS}}/\Delta T$	Input Offset Current Drift	(Note 8)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●	120			$\text{pA}/^{\circ}\text{C}$
$I_{\text{B-}}$	Inverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 40	nA
$\Delta I_{\text{B-}}/\Delta T$	Inverting Input Bias Current Drift	(Note 8)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●	80			$\text{pA}/^{\circ}\text{C}$
$I_{\text{B+}}$	Noninverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 80	nA
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR	$\pm 15\text{V}$	●	12.5			V
			$\pm 5\text{V}$	●	2.5			V
	Input Voltage Range (Negative)	Guaranteed by CMRR	$\pm 15\text{V}$	●			-12.5	V
			$\pm 5\text{V}$	●			-2.5	V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = \pm 12.5\text{V}$	$\pm 15\text{V}$	●	92			dB
		$V_{\text{CM}} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	92		± 4.5	dB
	Minimum Supply Voltage	Guaranteed by PSRR		●				V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$		●	93			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	●	75			V/mV
		$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	75			V/mV
		$V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 10\text{k}$	$\pm 5\text{V}$	●	75			V/mV
		$V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	●	75			V/mV
V_{OUT}	Maximum Output Swing	$R_L = 10\text{k}$, 1mV Overdrive	$\pm 15\text{V}$	●	± 12.8			V
		$R_L = 2\text{k}$, 1mV Overdrive	$\pm 15\text{V}$	●	± 12.6			V
		$R_L = 10\text{k}$, 1mV Overdrive	$\pm 5\text{V}$	●	± 2.8			V
		$R_L = 2\text{k}$, 1mV Overdrive	$\pm 5\text{V}$	●	± 2.6			V
I_{OUT}	Maximum Output Current	$V_{\text{OUT}} = \pm 12.5\text{V}$, 1mV Overdrive	$\pm 15\text{V}$	●	± 7			mA
		$V_{\text{OUT}} = \pm 2.5\text{V}$, 1mV Overdrive	$\pm 5\text{V}$	●	± 7			mA
I_{SC}	Output Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, 0.2V Overdrive (Note 3)	$\pm 15\text{V}$	●	± 12			mA
SR	Slew Rate	$R_L = 2\text{k}$ (Note 6)	$\pm 15\text{V}$	●	15			V/ μs
			$\pm 5\text{V}$	●	11			V/ μs
GBW	Gain Bandwidth Product	$f = 100\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	110	200		MHz
			$\pm 5\text{V}$	●	100	190		MHz
	Channel Separation	$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 2\text{k}$ $V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	96			dB
			$\pm 5\text{V}$	●	96			dB
I_S	Supply Current	Per Amplifier	$\pm 15\text{V}$	●			7	mA
			$\pm 5\text{V}$	●			6.8	mA
ΔV_{OS}	Input Offset Voltage Match		$\pm 15\text{V}$	●			800	μV
			$\pm 5\text{V}$	●			800	μV
$\Delta I_{\text{B-}}$	Inverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			78	nA
$\Delta I_{\text{B+}}$	Noninverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			158	nA
ΔCMRR	Common Mode Rejection Match	$V_{\text{CM}} = \pm 12.5\text{V}$ (Note 9)	$\pm 15\text{V}$	●	89			dB
		$V_{\text{CM}} = \pm 2.5\text{V}$ (Note 9)	$\pm 5\text{V}$	●	89			dB
ΔPSRR	Power Supply Rejection Match	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$ (Note 9)		●	90			dB

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ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes and two 100Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: The LT1469C-2 and LT1469I-2 are guaranteed functional over the operating temperature range of -40°C to 85°C.

Note 5: The LT1469C-2 is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet specified performance from -40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1469I-2 is guaranteed to meet specified performance from -40°C to 85°C.

Note 6: Slew rate is measured between ±8V on the output with ±12V swing for ±15V supplies and ±2V on the output with ±3V swing for ±5V supplies. Tested in $A_V = -10$.

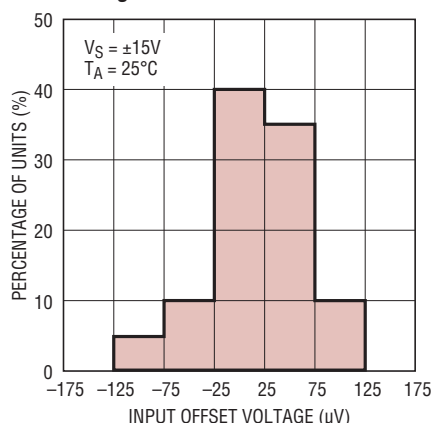
Note 7: Full-power bandwidth is calculated from the slew rate. $FPBW = SR/2\pi V_P$.

Note 8: This parameter is not 100% tested.

Note 9: $\Delta CMRR$ and $\Delta PSRR$ are defined as follows: 1) CMRR and PSRR are measured in $\mu V/V$ on each amplifier; 2) the difference between the two sides is calculated in $\mu V/V$; 3) the result is converted to dB.

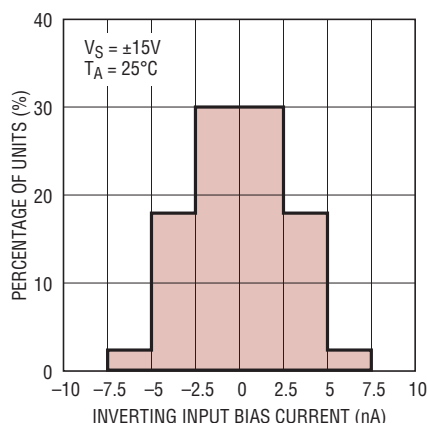
TYPICAL PERFORMANCE CHARACTERISTICS

Distribution of Input Offset Voltage



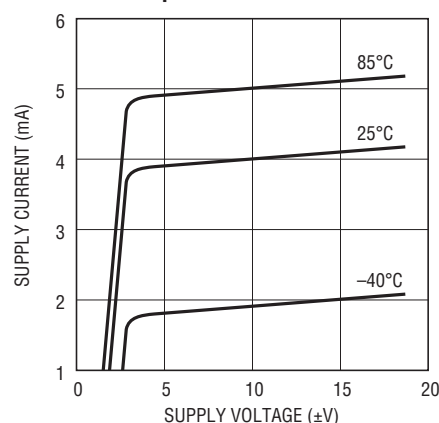
14692 G01

Distribution of Inverting Input Bias Current



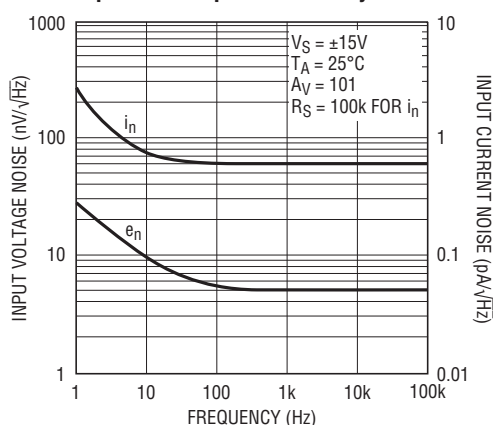
14692 G02

Supply Current vs Supply Voltage and Temperature



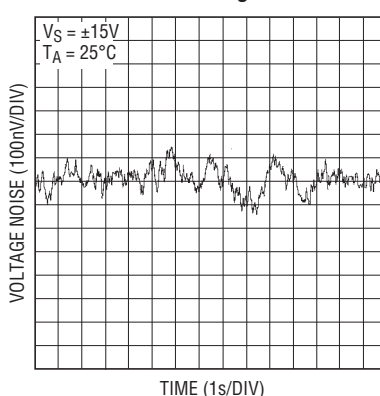
14692 G03

Input Noise Spectral Density



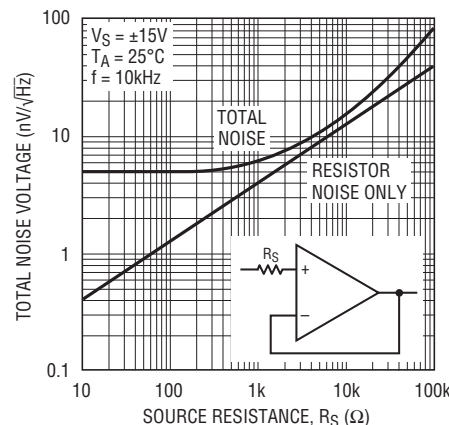
14692 G04

0.1Hz to 10Hz Voltage Noise



14692 G05

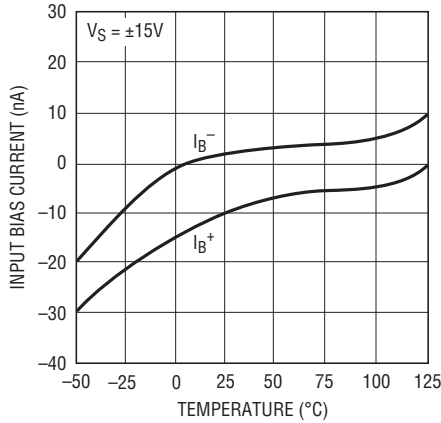
Total Noise vs Unmatched Source Resistance



14692 G06

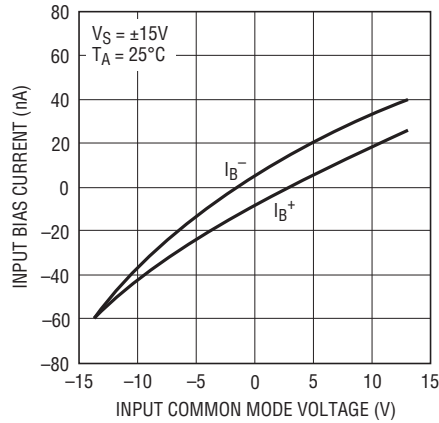
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Temperature



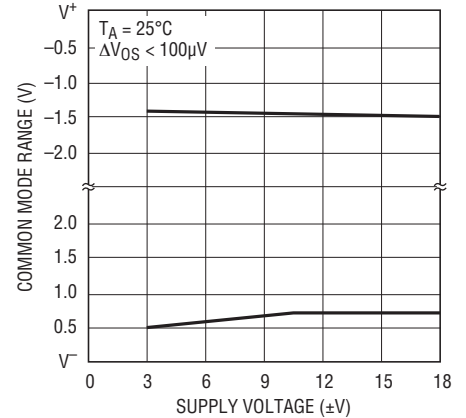
14692 G07

Input Bias Current vs Input Common Mode Voltage



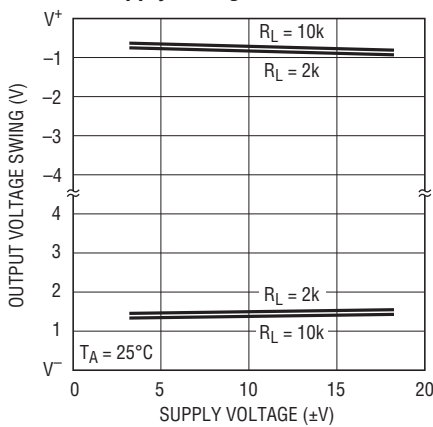
14692 G08

Input Common Mode Range vs Supply Voltage



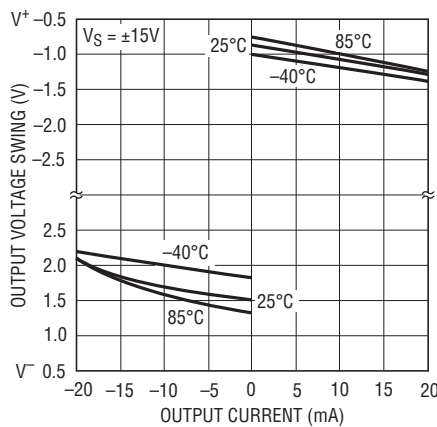
14692 G09

Output Voltage Swing vs Supply Voltage



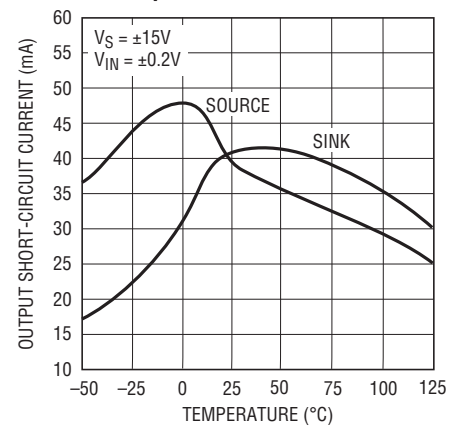
14692 G10

Output Voltage Swing vs Load Current



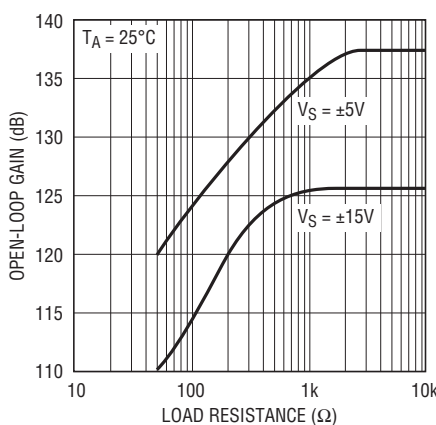
14692 G11

Output Short-Circuit Current vs Temperature



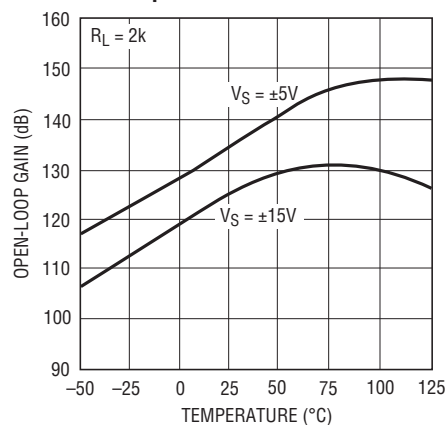
14692 G12

Open-Loop Gain vs Resistive Load



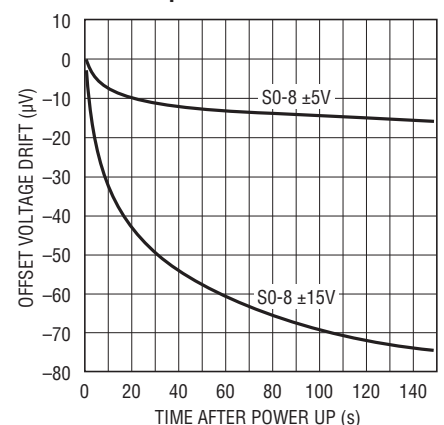
14692 G13

Open-Loop Gain vs Temperature



14692 G14

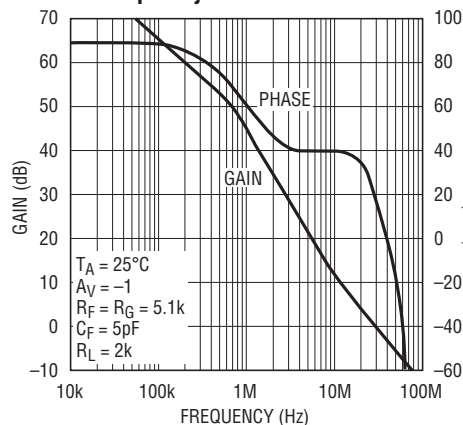
Warm-Up Drift vs Time



14692 G15

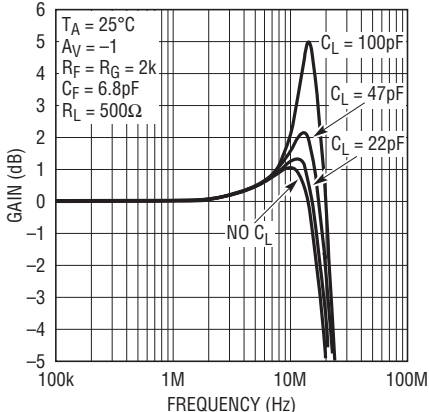
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Gain and Phase vs Frequency



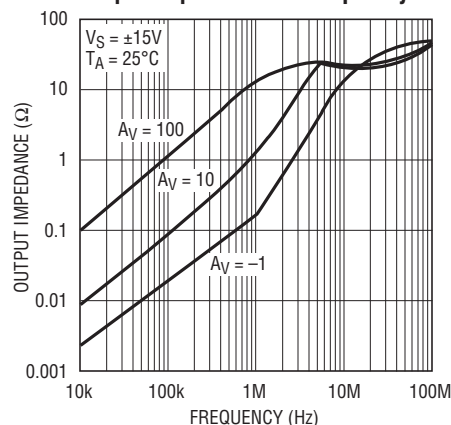
14692 G16

Gain vs Frequency, AV = -1



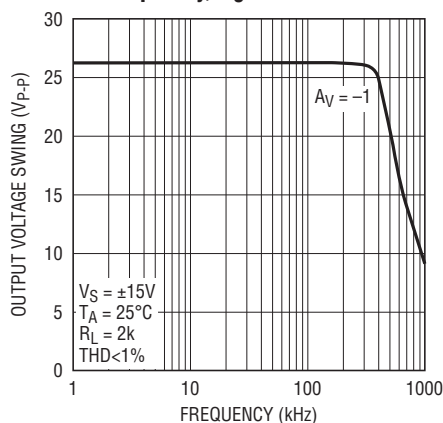
14692 G17

Output Impedance vs Frequency



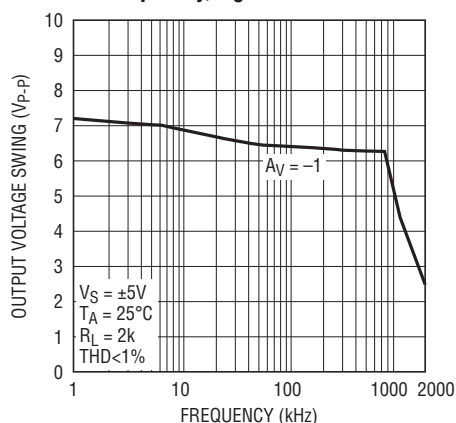
14692 G18

Undistorted Output Swing vs Frequency, VS = ±15V



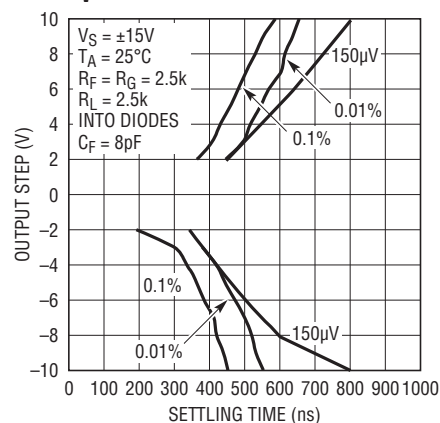
14692 G19

Undistorted Output Swing vs Frequency, VS = ±5V



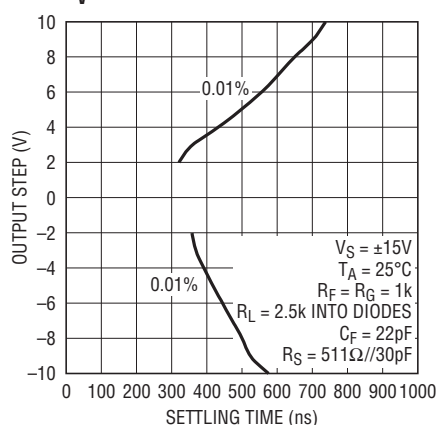
14692 G20

Settling Time vs Output Step, AV = -1



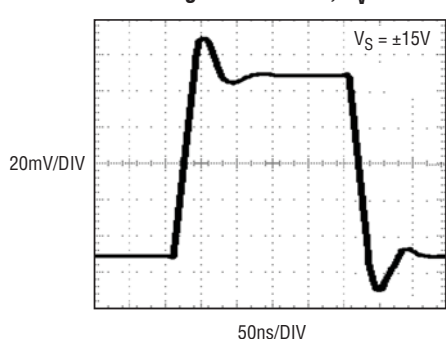
14692 G21

Settling Time vs Output Step, AV = 2



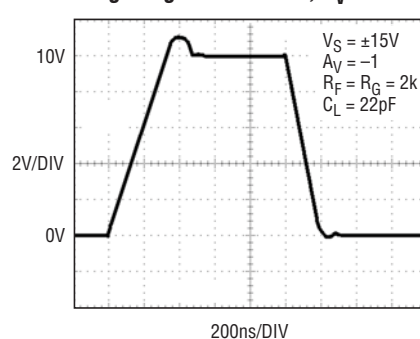
14692 G22

Small-Signal Transient, AV = -1



14692 G23

Large-Signal Transient, AV = -1



14692 G24

APPLICATIONS INFORMATION

Gain of 2 Stable

The LT1469-2 is a decompensated version of the LT1469. The DC precision performance is identical, but the internal compensation capacitors have been reduced to a point where the op amp needs a gain of 2 or greater in order to be stable.

In general, for applications where the gain around the op amp is ≥ 2 , the decompensated version should be used, because it will give the best AC performance. In applications where the gain is < 2 , the unity-gain stable version should be used.

The appropriate way to define the ‘gain’ is as the inverse of the feedback ratio from output to differential input, including all relevant parasitics. Moreover, as with all feedback loops, the stability of the loop depends on the value of that feedback ratio at frequencies where the total loop-gain would cross unity. Therefore, it is possible to have circuits in which the gain at DC is lower than the gain at high frequency, and these circuits can be stable even with a non unity-gain stable op amp. An example is many current-output DAC buffer applications.

Layout and Passive Components

The LT1469 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example, fast settling time) use a ground plane, short lead lengths and RF quality bypass capacitors ($0.01\mu\text{F}$ to $0.1\mu\text{F}$) in parallel with low ESR bypass capacitors ($1\mu\text{F}$ to $10\mu\text{F}$ tantalum). For best DC performance, use “star” grounding techniques, equalize input trace lengths and minimize leakage (e.g., $1.5\text{G}\Omega$ of leakage between an

input and a 15V supply will generate 10nA —equal to the maximum I_{B} specification).

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: for inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below).

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the inputs can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short and the two input leads should be as close together as possible and maintained at the same temperature.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. A feedback capacitor of value $C_F = R_G \cdot C_{\text{IN}}/R_F$ may be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, C_F should be less than or equal to one half of C_{IN} . An example would be a DAC I-to-V converter as shown on the front page of the data sheet where the DAC can have many tens of picofarads of output capacitance.

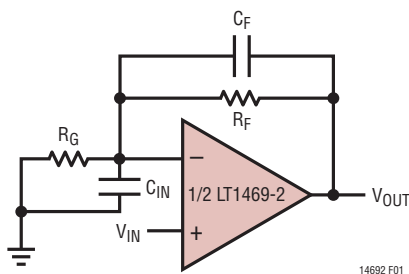


Figure 1. Nulling Input Capacitance

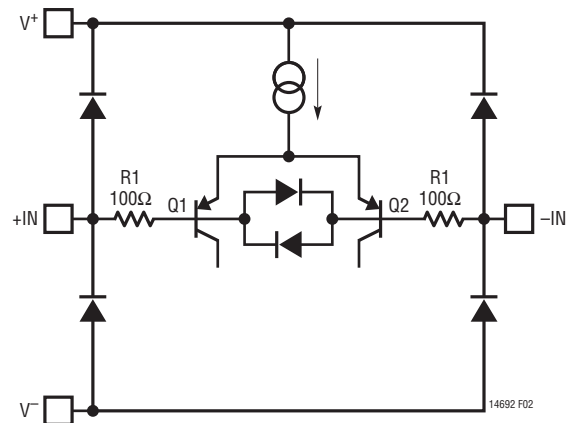


Figure 2. Input Stage Protection

APPLICATIONS INFORMATION

Input Considerations

Each input of the LT1469 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If large differential input voltages are anticipated, limit the input current to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven beyond the supply, limit the current with an external resistor to less than 10mA .

The LT1469 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

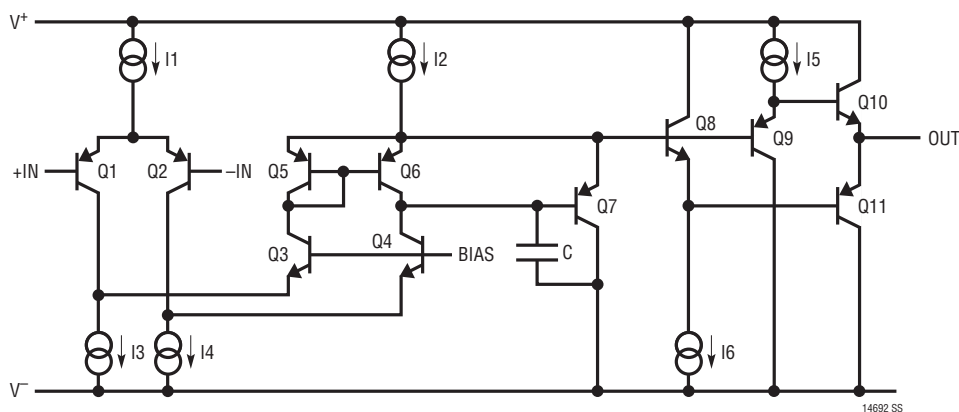
The input bias currents vary with common mode voltage. The cancellation circuitry was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1469 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

Total Input Noise

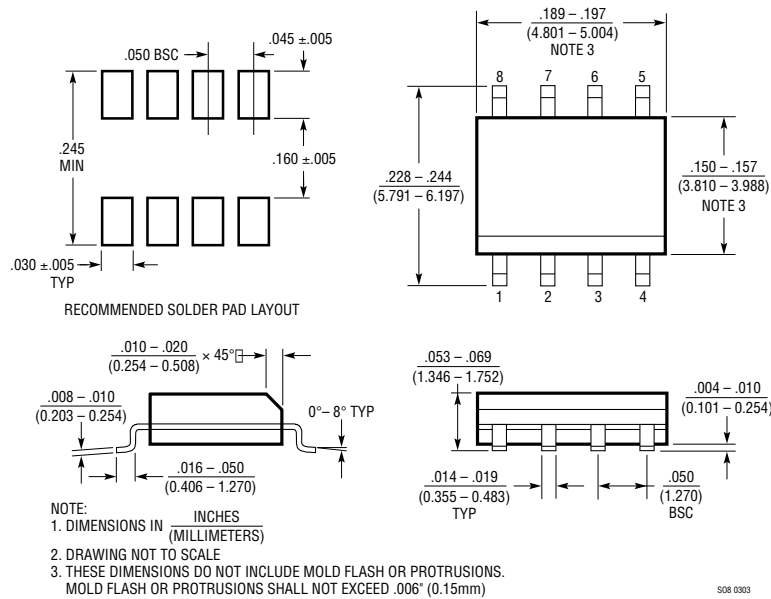
The total input noise of the LT1469 is optimized for a source resistance between 1k and 20k . Within this range, the total input noise is dominated by the noise of the source resistance itself. When the source resistance is below 1k , voltage noise of the amplifier dominates. When the source resistance is above 20k , the input noise current is the dominant contributor.

SIMPLIFIED SCHEMATIC

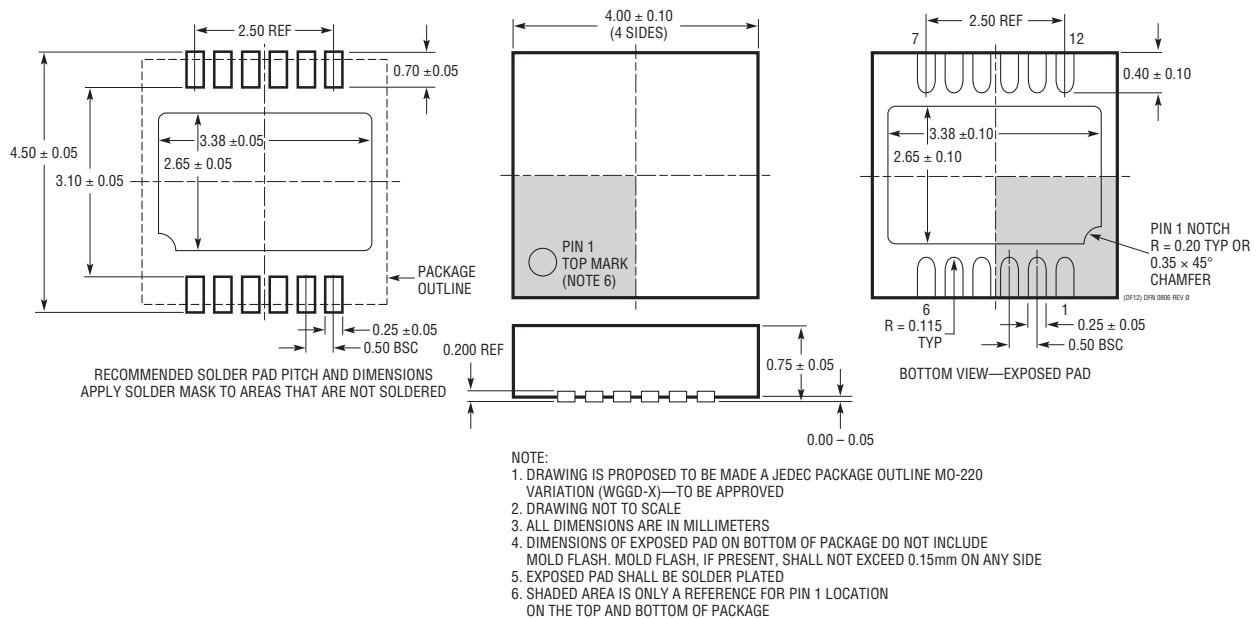


PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (Reference LTC DWG # 05-08-1610)



DF Package 12-Lead Plastic DFN (4mm × 4mm) (Reference LTC DWG # 05-08-1773 Rev 0)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1167	Precision Instrumentation Amplifier	Single Resistor Gain Set, 0.04% Max Gain Error, 10ppm Max Gain Nonlinearity
LT1468	Single 90MHz, 22V/ μ s, 16-Bit Accurate Op Amp	75 μ V Max V_{OS} , Single Version of LT1469
LTC1595/LTC1596	16-Bit Serial Multiplying I_{OUT} DAC	± 1 LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade
LTC1597	16-Bit Parallel Multiplying I_{OUT} DAC	± 1 LSB Max INL/DNL, Low Glitch, On-Chip Bipolar Resistors
LTC1604	16-Bit, 333ksps Sampling ADC	± 2.5 V Input, SINAD = 90dB, THD = -100dB
LTC1605	Single 5V, 16-Bit, 100ksps Sampling ADC	Low Power, ± 10 V Inputs, Parallel/Byte Interface