Six LVPECL Outputs, SiGe Clock Fanout Buffer

Data Sheet

ADCLK946

FEATURES

- 4.8 GHz operating frequency
- 75 fs rms broadband random jitter
- On-chip input terminations
- 3.3 V power supply

APPLICATIONS

- Low jitter clock distribution
- Clock and data signal restoration
- Level translation
- Wireless communications
- Wired communications
- Medical and industrial imaging
- ATE and high performance instrumentation

GENERAL DESCRIPTION

The ADCLK946 is an ultrafast clock fanout buffer fabricated on the Analog Devices, Inc., proprietary XFCB3 silicon germanium (SiGe) bipolar process. This device is designed for high speed applications requiring low jitter.

The device has a differential input equipped with center-tapped, differential, 100 Ω on-chip termination resistors. The input accepts dc-coupled LVPECL, CML, 3.3 V CMOS (single ended), and ac-coupled 1.8 V CMOS, LVDS, and LVPECL inputs. A V_{REF} pin is available for biasing ac-coupled inputs.

The ADCLK946 features six full-swing emitter-coupled logic (ECL) output drivers. For LVPECL (positive ECL) operation, bias V_{CC} to the positive supply and V_{EE} to ground. For ECL operation, bias V_{CC} to ground and V_{EE} to the negative supply.

The ECL output stages are designed to directly drive 800 mV each side into 50 Ω terminated to V_{CC} − 2 V for a total differential output swing of 1.6 V.

The ADCLK946 is available in a 24-lead LFCSP and is specified for operation over the standard industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

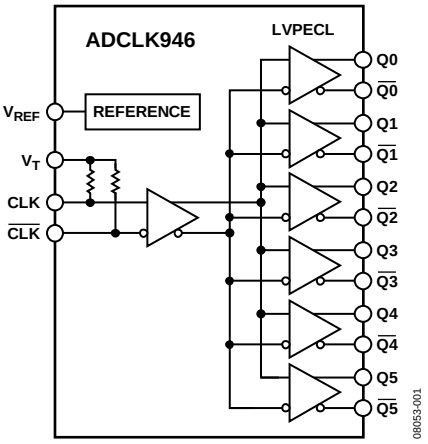

Figure 1.

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Technical Support www.analog.com

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8/2017—Rev. A to Rev. B

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5/2010—Rev. 0 to Rev. A

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4/2009—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Typical (typ) values are given for $V_{CC} - V_{EE}$ = 3.3 V and T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over the full $V_{CC} - V_{EE}$ = 3.3 V ± 10% and T_A = −40°C to +85°C variation, unless otherwise noted.

Table 1. Clock Inputs and Outputs

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC INPUT CHARACTERISTICS						
Input Voltage High Level	V_{IH}	V_{EE} + 1.6		V_{CC}	V	
Input Voltage Low Level	V_{IL}	V_{EE}		V_{CC} − 0.2	V	
Input Differential Range	V_{ID}	0.4		3.4	V p-p	±1.7 V between input pins
Input Capacitance	C_{IN}		0.4		pF	
Input Resistance						
Single-Ended Mode			50		Ω	
Differential Mode			100		Ω	
Common Mode			50		kΩ	Open V_T
Input Bias Current			20		μA	
Hysteresis			10		mV	
DC OUTPUT CHARACTERISTICS						
Output Voltage High Level	V_{OH}	V_{CC} − 1.26		V_{CC} − 0.76	V	50 Ω to (V_{CC} − 2.0 V)
Output Voltage Low Level	V_{OL}	V_{CC} − 1.99		V_{CC} − 1.54	V	50 Ω to (V_{CC} − 2.0 V)
Output Voltage, Single-Ended	V_O	610		960	mV	$V_{OH} - V_{OL}$, output static
Reference Voltage	V_{REF}					
Output Voltage			(V_{CC} + 1)/2		V	−500 μA to +500 μA
Output Resistance			235		Ω	

Table 2. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC PERFORMANCE						
Maximum Output Frequency		4.5	4.8		GHz	See Figure 4 for differential output voltage vs. frequency, >0.8 V differential output swing
Output Rise/Fall Time	t_R, t_F	40	75	90	ps	20% to 80% measured differentially
Propagation Delay	t_{PD}	150	185	220	ps	V_{ICM} = 2 V, V_{ID} = 1.6 V p-p
Temperature Coefficient			50		fs/°C	
Output-to-Output Skew			9	28	ps	
Part-to-Part Skew[1]				45	ps	V_{ID} = 1.6 V p-p
Additive Time Jitter						
Integrated Random Jitter			28		fs rms	BW = 12 kHz − 20 MHz, CLK = 1 GHz
Broadband Random Jitter[2]			75		fs rms	V_{ID} = 1.6 V p-p, 8 V/ns, V_{ICM} = 2 V
Crosstalk-Induced Jitter[3]			90		fs rms	
CLOCK OUTPUT PHASE NOISE						
Absolute Phase Noise						Input slew rate > 1 V/ns (see Figure 11 for more details)
f_{IN} = 1 GHz			−119		dBc/Hz	@ 100 Hz offset
			−134		dBc/Hz	@ 1 kHz offset
			−145		dBc/Hz	@ 10 kHz offset
			−150		dBc/Hz	@ 100 kHz offset
			−150		dBc/Hz	>1 MHz offset

[1] The output skew is the difference between any two similar delay paths while operating at the same voltage and temperature.
[2] Measured at the rising edge of the clock signal; calculated using the SNR of the ADC method.
[3] The amount of added jitter measured at the output while two related, asynchronous, differential frequencies are applied to the inputs.

Table 3. Power

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Supply Voltage Requirement	$V_{CC} - V_{EE}$	2.97		3.63	V	3.3 V + 10%
Power Supply Current						Static
Negative Supply Current	I_{VEE}		90	115	mA	$V_{CC} - V_{EE}$ = 3.3 V ± 10%
Positive Supply Current	I_{VCC}		245	275	mA	$V_{CC} - V_{EE}$ = 3.3 V ± 10%
Power Supply Rejection[1]	PSR_{VCC}		<3		ps/V	$V_{CC} - V_{EE}$ = 3.3 V ± 10%
Output Swing Supply Rejection[2]	PSR_{VCC}		28		dB	$V_{CC} - V_{EE}$ = 3.3 V ± 10%

[1] Change in t_{PD} per change in V_{CC}.
[2] Change in output swing per change in V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	
$V_{CC} - V_{EE}$	6.0 V
Input Voltage	
CLK, $\overline{CLK}$	V_{EE} − 0.5 V to V_{CC} + 0.5 V
CLK, $\overline{CLK}$ to V_T Pin (CML, LVPECL Termination)	±40 mA
CLK to $\overline{CLK}$	±1.8 V
Input Termination, V_T to CLK, $\overline{CLK}$	±2 V
Maximum Voltage on Output Pins	V_{CC} + 0.5 V
Maximum Output Current	35 mA
Voltage Reference (V_{REF})	V_{CC} to V_{EE}
Operating Temperature Range	
Ambient	−40°C to +85°C
Junction	150°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

DETERMINING JUNCTION TEMPERATURE

To determine the junction temperature on the application printed circuit board (PCB), use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the customer at the top center of the package.
Ψ_{JT} is as indicated in Table 5.
P_D is the power dissipation.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A is the ambient temperature (°C).

Values of θ_{JB} are provided in Table 5 for package comparison and PCB design considerations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THERMAL PERFORMANCE

Table 5.

Parameter	Symbol	Description	Value[1]	Unit
Junction-to-Ambient Thermal Resistance				
Still Air				
0.0 m/sec Airflow	θ_{JA}	Per JEDEC JESD51-2	54.3	°C/W
Moving Air				
1.0 m/sec Airflow	θ_{JMA}	Per JEDEC JESD51-6	47.5	°C/W
2.5 m/sec Airflow	θ_{JMA}	Per JEDEC JESD51-6	42.6	°C/W
Junction-to-Board Thermal Resistance				
Moving Air				
1.0 m/sec Airflow	θ_{JB}	Per JEDEC JESD51-8 (moving air)	33.0	°C/W
Junction-to-Case Thermal Resistance (Die-to-Heat Sink)				
Moving Air	θ_{JC}	Per MIL-Std. 883, Method 1012.1	2.0	°C/W
Junction-to-Top-of-Package Characterization Parameter				
Still Air				
0 m/sec Airflow	Ψ_{JT}	Per JEDEC JESD51-2	0.9	°C/W

[1]Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

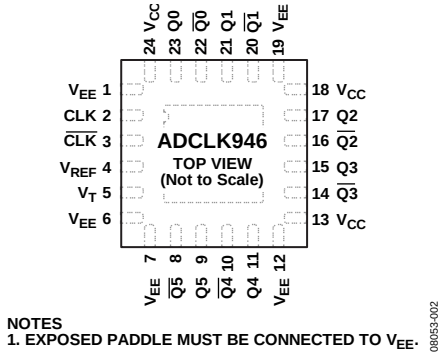

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6, 7, 12, 19	V_{EE}	Negative Supply Pin.
2	CLK	Differential Input (Positive).
3	$\overline{CLK}$	Differential Input (Negative).
4	V_{REF}	Reference Voltage. This pin provides the reference voltage for biasing ac-coupled CLK and $\overline{CLK}$ inputs.
5	V_T	Center Tap. This pin provides the center tap of a 100 Ω input resistor for CLK and $\overline{CLK}$ inputs.
8, 9	$\overline{Q5}$, Q5	Differential LVPECL Outputs.
10, 11	$\overline{Q4}$, Q4	Differential LVPECL Outputs.
13, 18, 24	V_{CC}	Positive Supply Pin.
14, 15	$\overline{Q3}$, Q3	Differential LVPECL Outputs.
16, 17	$\overline{Q2}$, Q2	Differential LVPECL Outputs.
20, 21	$\overline{Q1}$, Q1	Differential LVPECL Outputs.
22, 23	$\overline{Q0}$, Q0	Differential LVPECL Outputs.
	EPAD	EPAD must be soldered to V_{EE}.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3 V, V_{EE} = 0.0 V, V_{ICM} = V_{REF}, T_A = 25°C, clock outputs terminated at 50 Ω to V_{CC} − 2 V, unless otherwise noted.

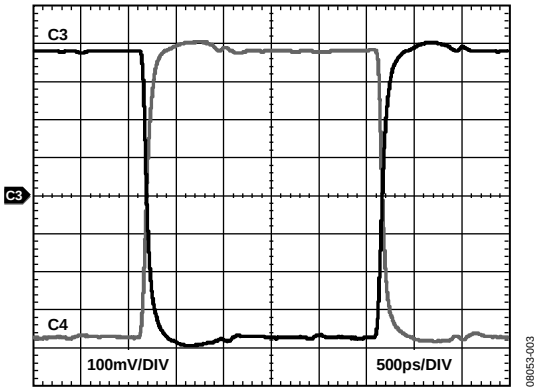

Figure 3. LVPECL Output Waveform @ 200 MHz

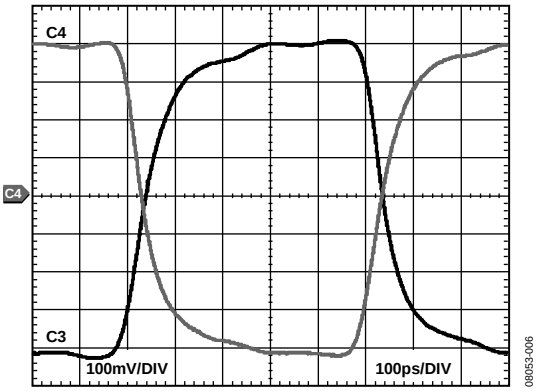

Figure 6. LVPECL Output Waveform @ 1000 MHz

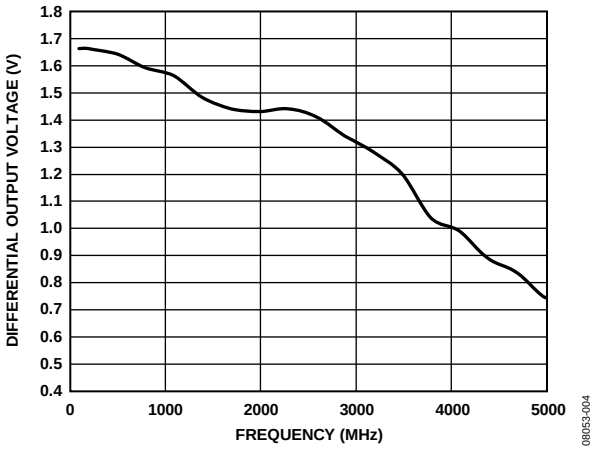

Figure 4. Differential Output Swing vs. Frequency

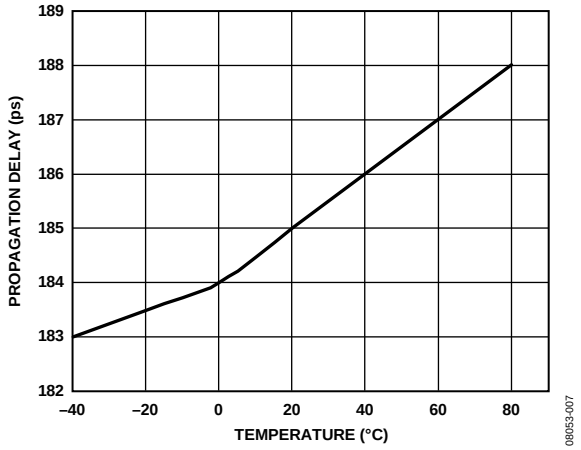

Figure 7. Propagation Delay vs. Temperature

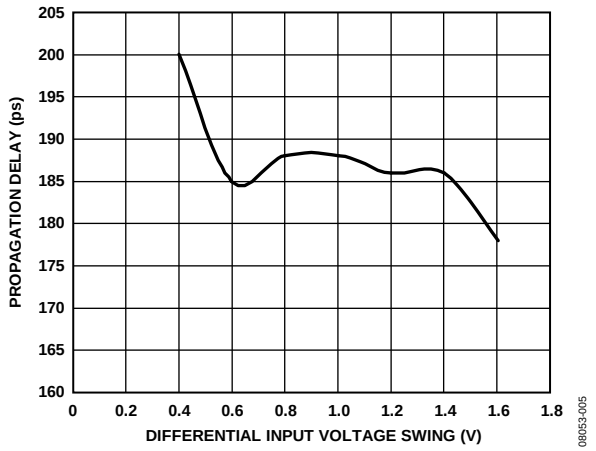

Figure 5. Propagation Delay vs. Differential Input Voltage

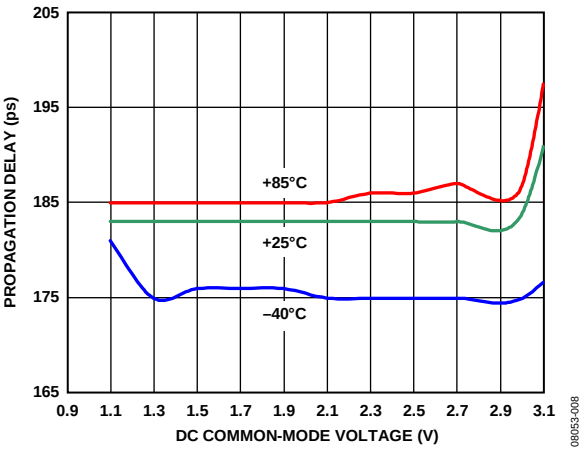

Figure 8. Propagation Delay vs. Common-Mode Voltage vs. Temperature, Input Slew Rate > 25 V/ns

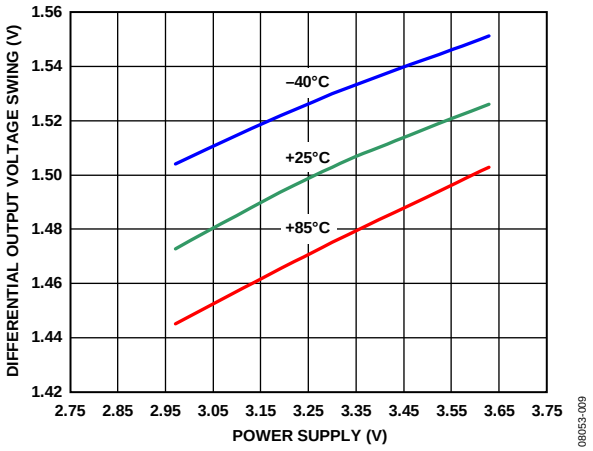

Figure 9. Differential Output Swing vs. Power Supply Voltage vs. Temperature, V_{ID} = 1.6 V p-p

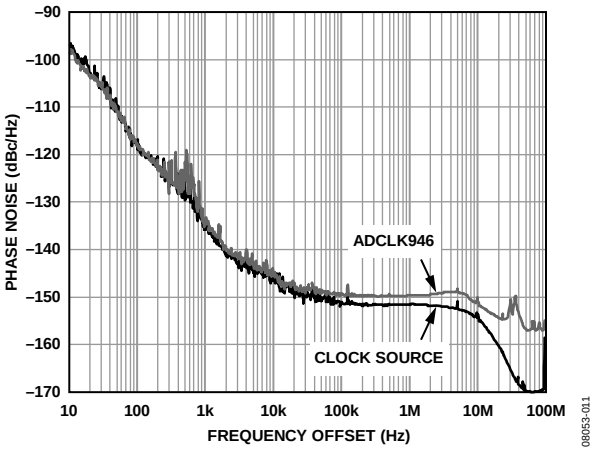

Figure 11. Absolute Phase Noise Measured @1 GHz with Agilent E5052

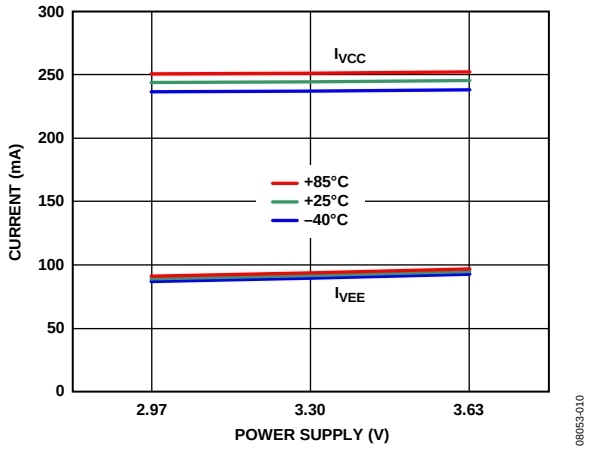

Figure 10. Power Supply Current vs. Power Supply Voltage vs. Temperature, All Outputs Loaded (50 Ω to V_{CC} – 2 V)

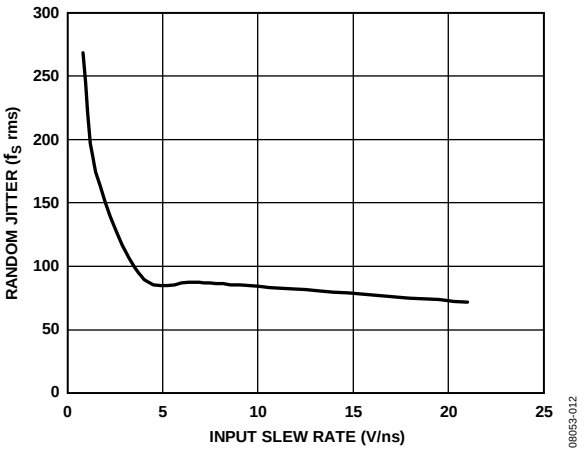

Figure 12. RMS Jitter vs. Input Slew Rate, V_{ID} Method

FUNCTIONAL DESCRIPTION

CLOCK INPUTS

The ADCLK946 accepts a differential clock input and distributes it to all six LVPECL outputs. The maximum specified frequency is the point at which the output voltage swing is 50% of the standard LVPECL swing (see Figure 4).

The device has a differential input equipped with center-tapped, differential, 100 Ω on-chip termination resistors. The input accepts dc-coupled LVPECL, CML, 3.3 V CMOS (single ended), and ac-coupled 1.8 V CMOS, LVDS, and LVPECL inputs. A V_{REF} pin is available for biasing ac-coupled inputs (see Figure 1).

Maintain the differential input voltage swing from approximately 400 mV p-p to no more than 3.4 V p-p. See Figure 14 through Figure 17 for various clock input termination schemes.

Output jitter performance is degraded by an input slew rate below 1 V/ns, as shown in Figure 12. The ADCLK946 is specifically designed to minimize added random jitter over a wide input slew rate range. Whenever possible, clamp excessively large input signals with fast Schottky diodes because attenuators reduce the slew rate. Input signal runs of more than a few centimeters should be over low loss dielectrics or cables with good high frequency characteristics.

CLOCK OUTPUTS

The specified performance necessitates using proper transmission line terminations. The LVPECL outputs of the ADCLK946 are designed to directly drive 800 mV into a 50 Ω cable or into microstrip/stripline transmission lines terminated with 50 Ω referenced to V_{CC} − 2 V, as shown in Figure 14. The LVPECL output stage is shown in Figure 13. The outputs are designed for best transmission line matching. If high speed signals must be routed more than a centimeter, either the microstrip or the stripline technique is required to ensure proper transition times and to prevent excessive output ringing and pulse-width-dependent, propagation delay dispersion.

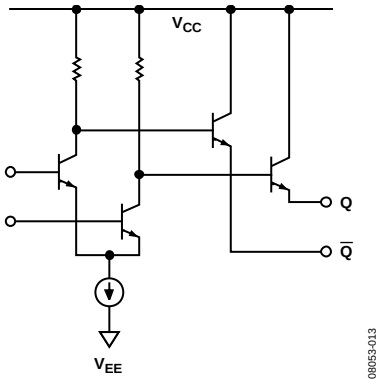

Figure 13. Simplified Schematic Diagram of the LVPECL Output Stage

Figure 14 through Figure 17 depict various LVPECL output termination schemes. When dc-coupled, V_{CC} of the receiving buffer should match the VS_DRV.

Thevenin-equivalent termination uses a resistor network to provide 50 Ω termination to a dc voltage that is below V_{OL} of the LVPECL driver. In this case, VS_DRV on the ADCLK946 should equal V_{CC} of the receiving buffer. Although the resistor combination shown in Figure 15 results in a dc bias point of VS_DRV − 2 V, the actual common-mode voltage is VS_DRV − 1.3 V because there is additional current flowing from the ADCLK946 LVPECL driver through the pull-down resistor.

LVPECL Y-termination is an elegant termination scheme that uses the fewest components and offers both odd- and even-mode impedance matching. Even-mode impedance matching is an important consideration for closely coupled transmission lines at high frequencies. Its main drawback is that it offers limited flexibility for varying the drive strength of the emitter-follower LVPECL driver. This can be an important consideration when driving long trace lengths but is usually not an issue.

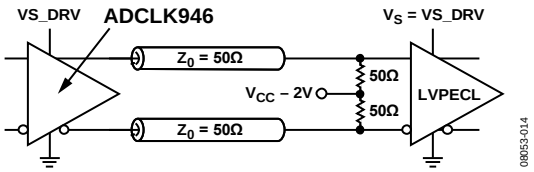

Figure 14. DC-Coupled, 3.3 V LVPECL

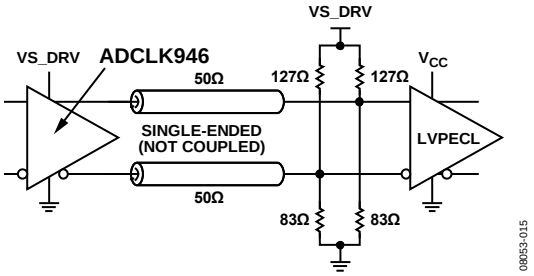

Figure 15. DC-Coupled, 3.3 V LVPECL Far-End Thevenin Termination

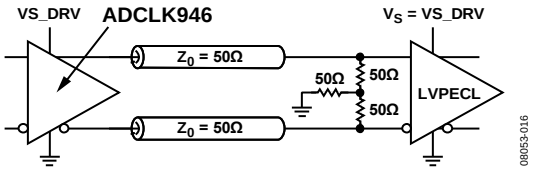

Figure 16. DC-Coupled, 3.3 V LVPECL Y-Termination

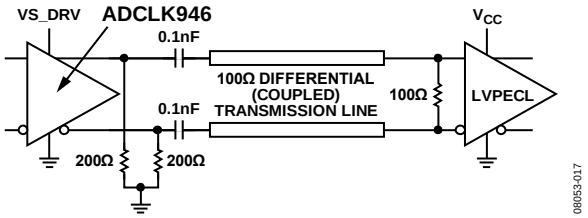

Figure 17. AC-Coupled, LVPECL with Parallel Transmission Line

PCB LAYOUT CONSIDERATIONS

The ADCLK946 buffer is designed for very high speed applications. Consequently, high speed design techniques must be used to achieve the specified performance. It is critically important to use low impedance supply planes for both the negative supply (V_{EE}) and the positive supply (V_{CC}) planes as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

The following references to the ground plane assume that the V_{EE} power plane is grounded for LVPECL operation. Note that, for ECL operation, the V_{CC} power plane becomes the ground plane.

It is also important to adequately bypass the input and output supplies. Place a 1 µF electrolytic bypass capacitor within several inches of each V_{CC} power supply pin to the ground plane. In addition, place multiple high quality 0.001 µF bypass capacitors as close as possible to each of the V_{CC} supply pins, and connect the capacitors to the ground plane with redundant vias. Carefully select high frequency bypass capacitors for minimum inductance and ESR. To improve the effectiveness of the bypass at high frequencies, minimize parasitic layout inductance. Also, avoid discontinuities along input and output transmission lines that can affect jitter performance.

In a 50 Ω environment, input and output matching have a significant impact on performance. The buffer provides internal 50 Ω termination resistors for both CLK and $\overline{\text{CLK}}$ inputs. Normally, the return side is connected to the reference pin that is provided. Carefully bypass the termination potential using ceramic capacitors to prevent undesired aberrations on the input signal due to parasitic inductance in the termination return path. If the inputs are dc-coupled to a source, take care to ensure that the pins are within the rated input differential and common-mode ranges.

If the return is floated, the device exhibits a 100 Ω cross-termination, but the source must then control the common-mode voltage and supply the input bias currents.

There are ESD/clamp diodes between the input pins to prevent the application from developing excessive offsets to the input transistors. ESD diodes are not optimized for best ac performance. When a clamp is required, it is recommended that appropriate external diodes be used.

Exposed Metal Paddle

The exposed metal paddle on the ADCLK946 package is both an electrical connection and a thermal enhancement. For the device to function properly, the paddle must be properly attached to the V_{EE} pin.

When properly mounted, the ADCLK946 also dissipates heat through its exposed paddle. The PCB acts as a heat sink for the ADCLK946. The PCB attachment must provide a good thermal path to a larger heat dissipation area. This requires a grid of vias from the top layer down to the V_{EE} power plane (see Figure 18). The ADCLK946 evaluation board (ADCLK946/PCBZ) provides an example of how to attach the part to the PCB.

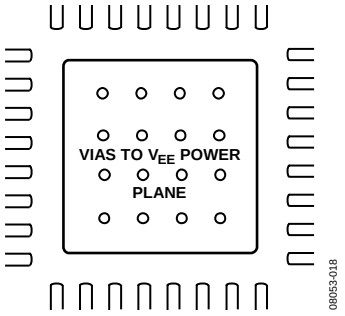

Figure 18. PCB Land for Attaching Exposed Paddle

INPUT TERMINATION OPTIONS

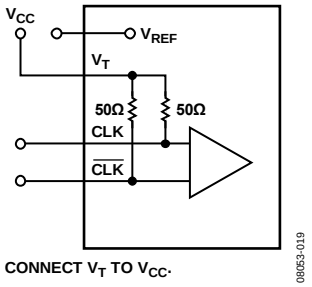

Figure 19. Interfacing to CML Inputs

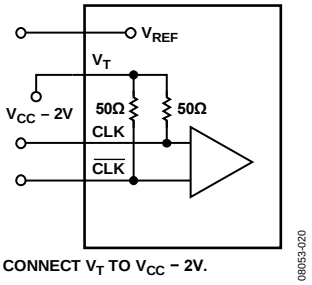

Figure 20. Interfacing to PECL Inputs

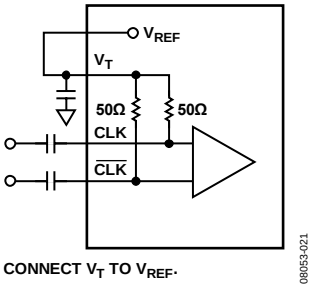

Figure 21. AC-Coupling Differential Signals Inputs, Such as LVDS

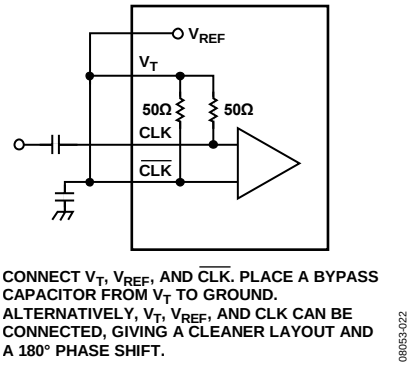

Figure 22. Interfacing to AC-Coupled Single-Ended Inputs

OUTLINE DIMENSIONS

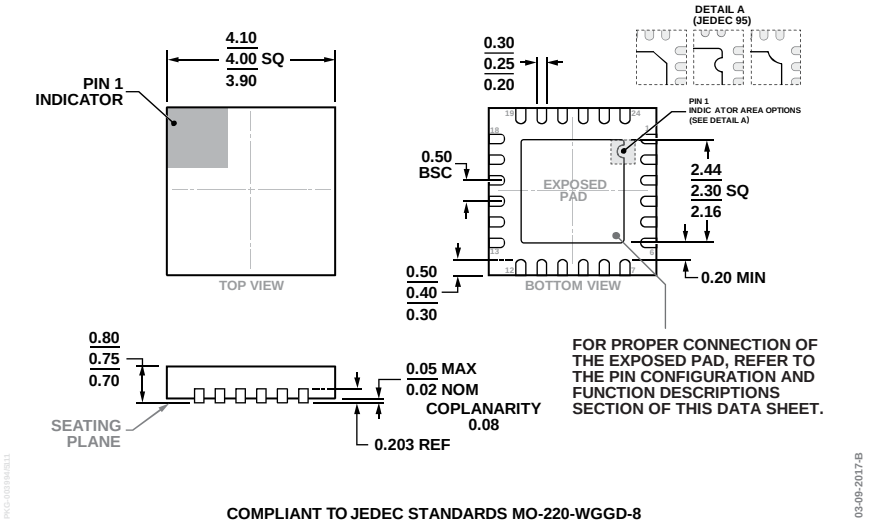

Figure 23. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
CP-24-14
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADCLK946BCPZ	−40°C to +85°C	24-Lead LFCSP	CP-24-14
ADCLK946BCPZ-REEL7	−40°C to +85°C	24-Lead LFCSP	CP-24-14
ADCLK946/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.