Discontinued Product

OKI Semiconductor

This version: Jan. 1998
Previous version: May 1997

MSM518200

4,194,304-Word × 2-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM518200 is a 4,194,304-word × 2-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM518200 achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM518200 is available in a 26/24-pin plastic SOJ or 26/24-pin plastic TSOP.

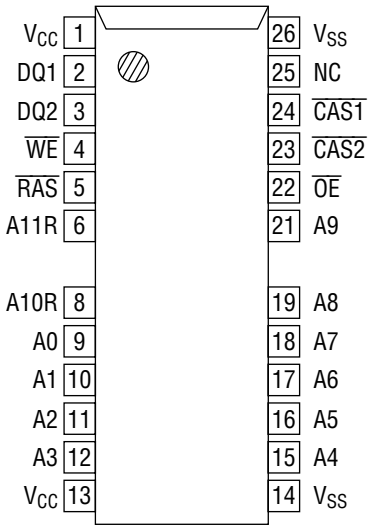
FEATURES

- 4,194,304-word × 2-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 4096 cycles/64 ms
- Fast page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$-only refresh capability
- Multi-bit test mode capability
- Package options:
  26/24-pin 300 mil plastic SOJ (SOJ26/24-P-300-1.27) (Product : MSM518200-xxSJ)
  26/24-pin 300 mil plastic TSOP (TSOPII26/24-P-300-1.27-K) (Product : MSM518200-xxTS-K)
  xx indicates speed rank.

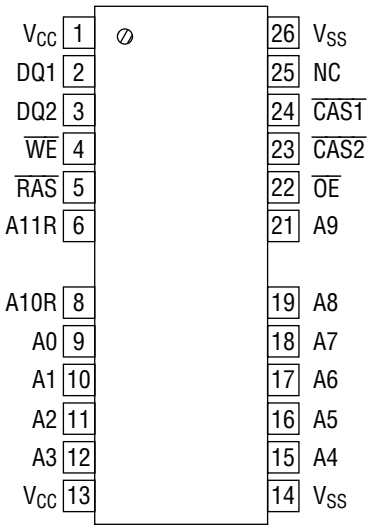
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM518200-60	60 ns	30 ns	15 ns	15 ns	110 ns	385 mW	5.5 mW
MSM518200-70	70 ns	35 ns	20 ns	20 ns	130 ns	358 mW	
MSM518200-80	80 ns	40 ns	20 ns	20 ns	150 ns	330 mW	

PIN CONFIGURATION (TOP VIEW)



26/24-Pin Plastic SOJ

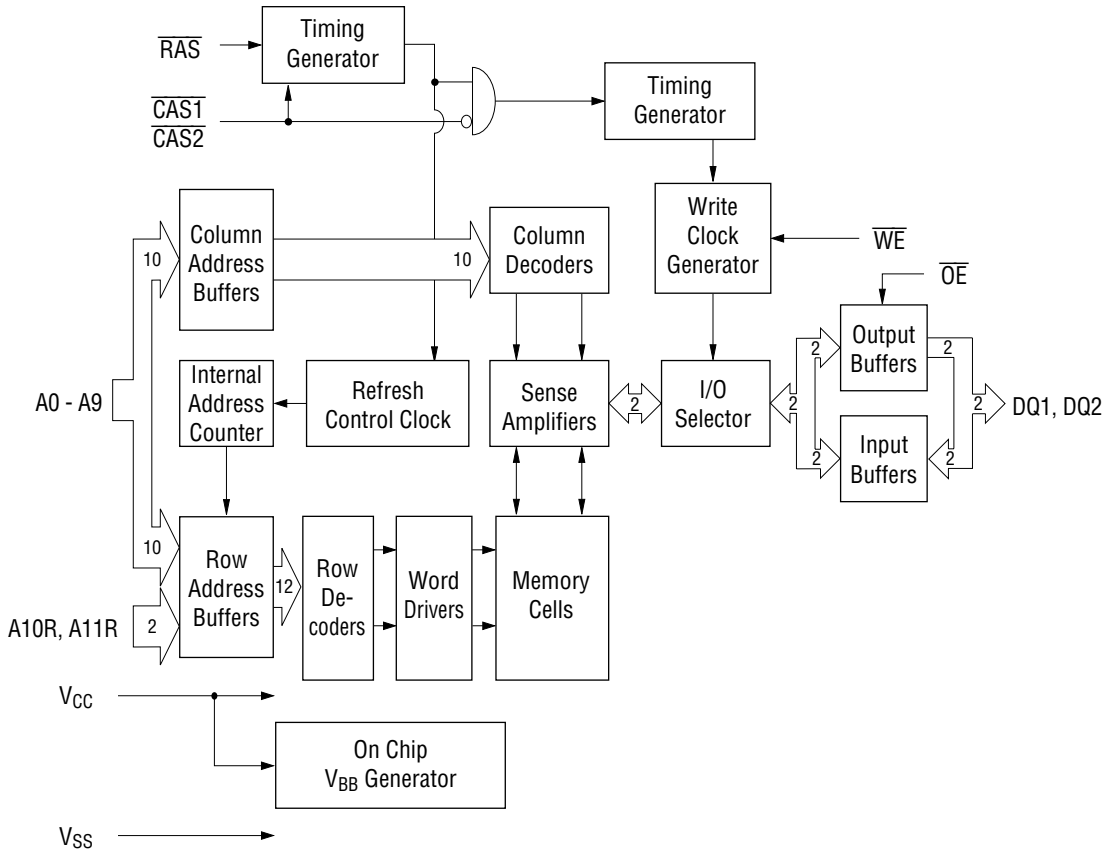


26/24-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0 - A9, A10R, A11R	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS1}$, $\overline{CAS2}$	Column Address Strobe
DQ1, DQ2	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (5 V)
V_{SS}	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
$\overline{RAS}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{WE}$	$\overline{OE}$	DQ1	DQ2	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	DQ1 Read
L	H	L	H	L	High-Z	D_{OUT}	DQ2 Read
L	L	L	H	L	D_{OUT}	D_{OUT}	DQ1, DQ2 Read
L	L	H	L	H	D_{IN}	Don't Care	DQ1 Write
L	H	L	L	H	Don't Care	D_{IN}	DQ2 Write
L	L	L	L	H	D_{IN}	D_{IN}	DQ1, DQ2 Write
L	L	L	H	H	High-Z	High-Z	—

*: "H" or "L"

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	–1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9, A10R, A11R)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1, DQ2)	$C_{I/O}$	—	10	pF

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM518200 -60		MSM518200 -70		MSM518200 -80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V	–10	10	–10	10	–10	10	µA	
Output Leakage Current	I_{LO}	DQ disable 0 V ≤ V_O ≤ 5.5 V	–10	10	–10	10	–10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS1}$, $\overline{CAS2}$ cycling, t_{RC} = Min.	—	70	—	65	—	60	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS1}$, $\overline{CAS2}$ = V_{IH}	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS1}$, $\overline{CAS2}$ ≥ V_{CC} –0.2 V	—	1	—	1	—	1		
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS1}$, $\overline{CAS2}$ = V_{IH}, t_{RC} = Min.	—	70	—	65	—	60	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS1}$, $\overline{CAS2}$ = V_{IL}, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS1}$, $\overline{CAS2}$ before $\overline{RAS}$	—	70	—	65	—	60	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS1}$, $\overline{CAS2}$ cycling, t_{PC} = Min.	—	60	—	55	—	50	mA	1, 3

Notes : 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. The address can be changed once or less while $\overline{CAS1}$, $\overline{CAS2}$ = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3, 11, 12

Parameter	Symbol	MSM518200 -60		MSM518200 -70		MSM518200 -80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	ns	
Read Modify Write Cycle Time	t_{RWC}	155	—	185	—	205	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	85	—	100	—	105	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	ns	4, 14
Access Time from $\overline{OE}$	t_{OEA}	—	15	—	20	—	20	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	4
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	20	0	20	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	0	20	0	20	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	64	—	64	—	64	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10	—	10	—	10	—	ns	16
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	13
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	ns	13
Column Address Hold Time from $\overline{RAS}$	t_{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	13
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8, 13
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	8

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3, 11, 12

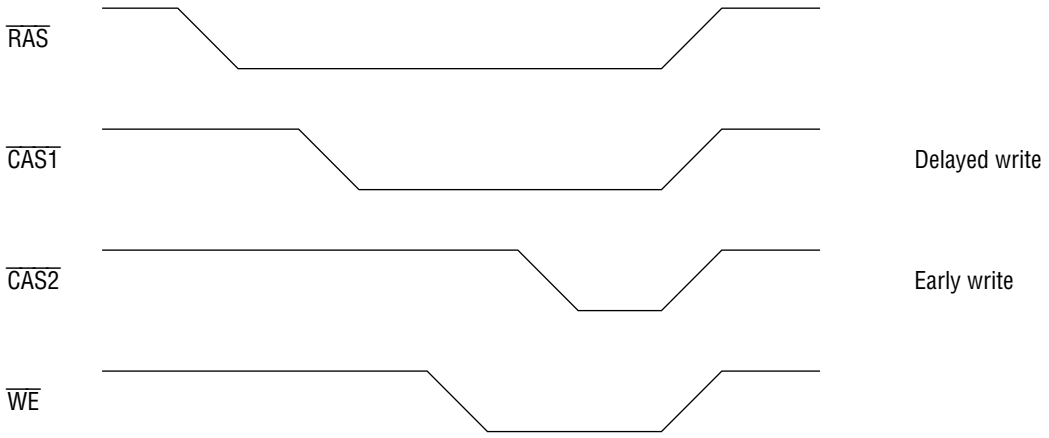
Parameter	Symbol	MSM518200 -60		MSM518200 -70		MSM518200 -80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	9, 13
Write Command Hold Time	t_{WCH}	10	—	15	—	15	—	ns	13
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	45	—	55	—	60	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	15	—	20	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	ns	15
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	10, 13
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	ns	10, 13
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	50	—	55	—	60	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	15	—	20	—	20	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40	—	50	—	50	—	ns	9
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	65	—	70	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	100	—	110	—	ns	9
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t_{CPWD}	60	—	70	—	75	—	ns	9, 14
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	10	—	10	—	10	—	ns	13
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	ns	13
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	—	20	—	20	—	ns	14
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WTH}	20	—	20	—	20	—	ns	

Notes:
1. A start-up delay of 200 µs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.
2. The AC characteristics assume t_T = 5 ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.
4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA}.
7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) , $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in an early write cycle, and to the $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle, or a read modify write cycle.
11. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test mode CA0 and CA1 are not used and each DQ pin now accesses 4-bit locations. Since all 2 DQ pins are used, a total of 8 data bits can be written in parallel into the memory array. In a read cycle, if 4 data bits are equal, the DQ pin will indicate a high level. If the 4 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
12. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.
13. These parameters are determined by the falling edge of either $\overline{CAS1}$ or $\overline{CAS2}$, whichever is earlier.
14. These parameters are determined by the rising edge of either $\overline{CAS1}$ or $\overline{CAS2}$, whichever is later.
15. t_{CWL} should be satisfied by both $\overline{CAS1}$ and $\overline{CAS2}$.
16. t_{CP} is determined by the time both $\overline{CAS1}$ and $\overline{CAS2}$ are high.

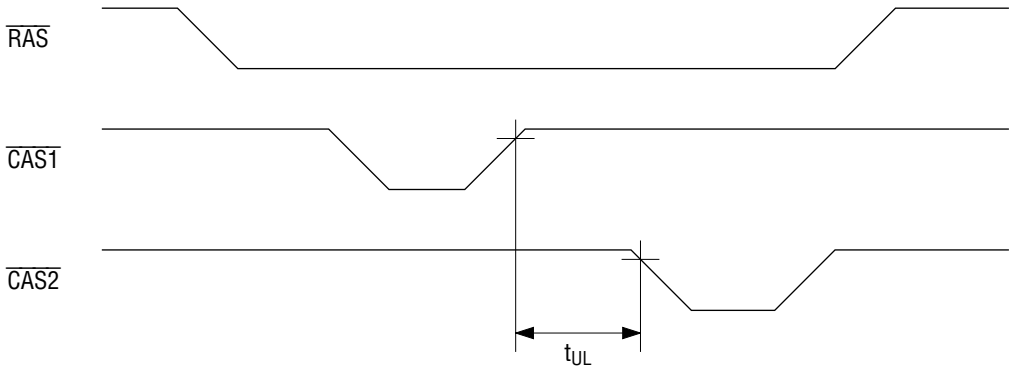
Notes concerning $\overline{CAS1}$ and $\overline{CAS2}$ control

Overlap the active-low timings of $\overline{CAS1}$ and $\overline{CAS2}$. Skew between $\overline{CAS1}$ and $\overline{CAS2}$ is allowed under the following conditions:

(1) The timing specification for $\overline{CAS1}$ and $\overline{CAS2}$ should be met individually.
(2) Different operation modes for $\overline{CAS1}$/$\overline{CAS2}$ are not allowed (as shown below).

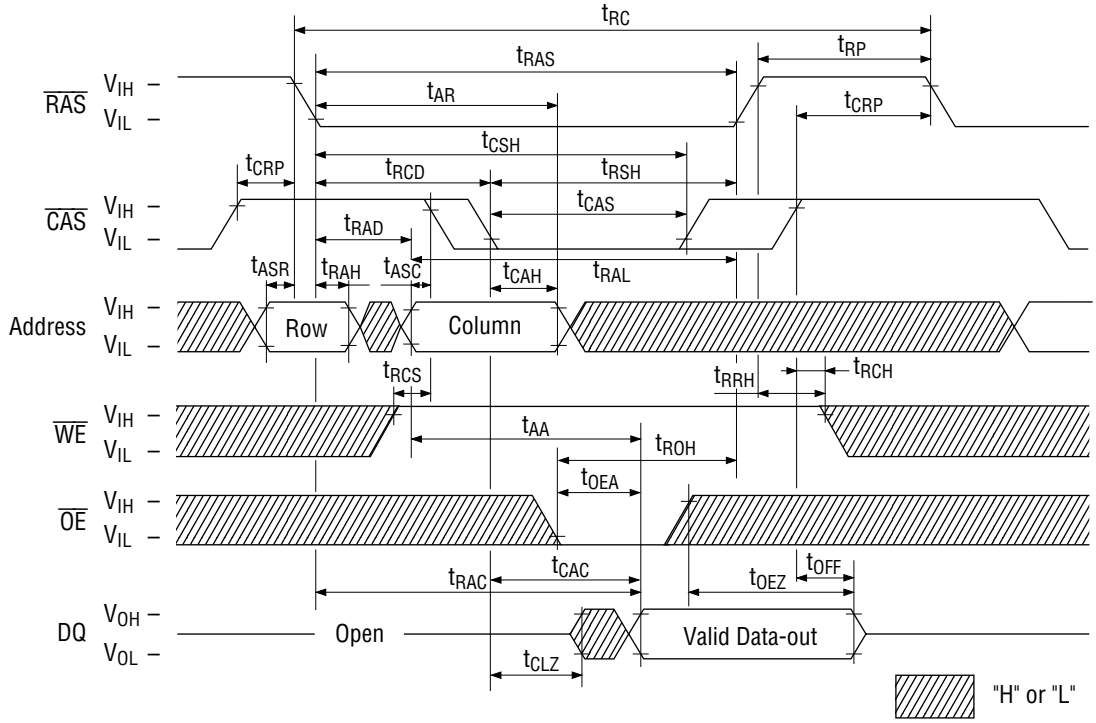


(3) Closely separated $\overline{CAS1}$/$\overline{CAS2}$ control is not allowed. However, when the condition ($t_{CP} \leq t_{UL}$) is satisfied, fast page mode can be performed.

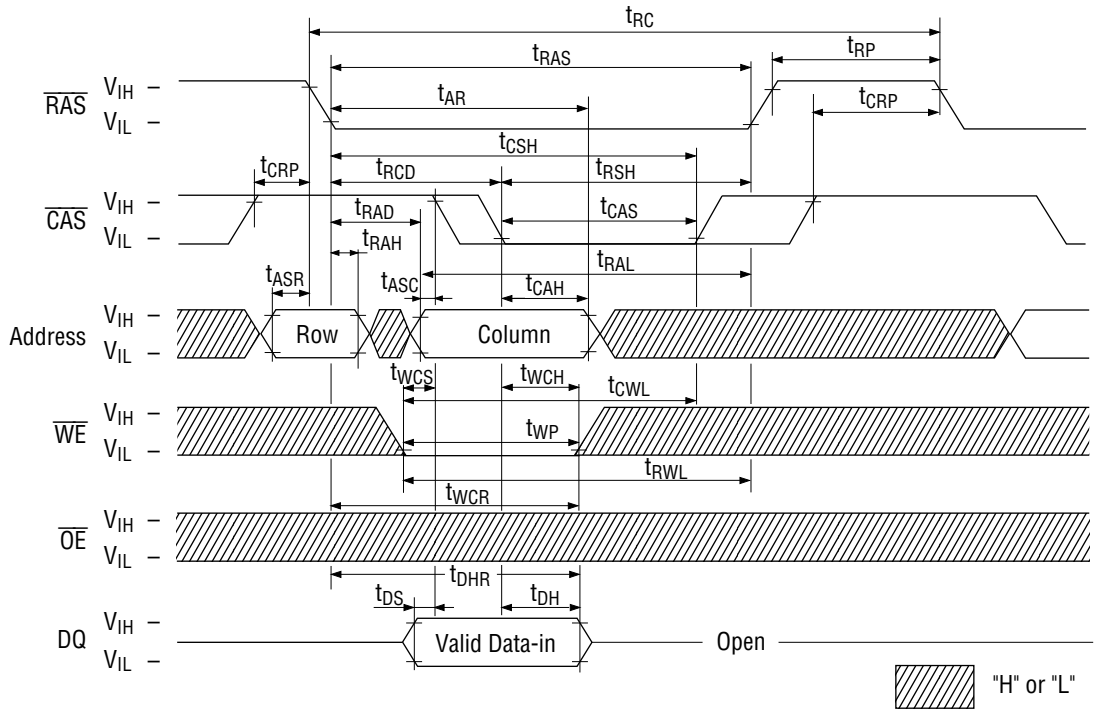


TIMING WAVEFORM

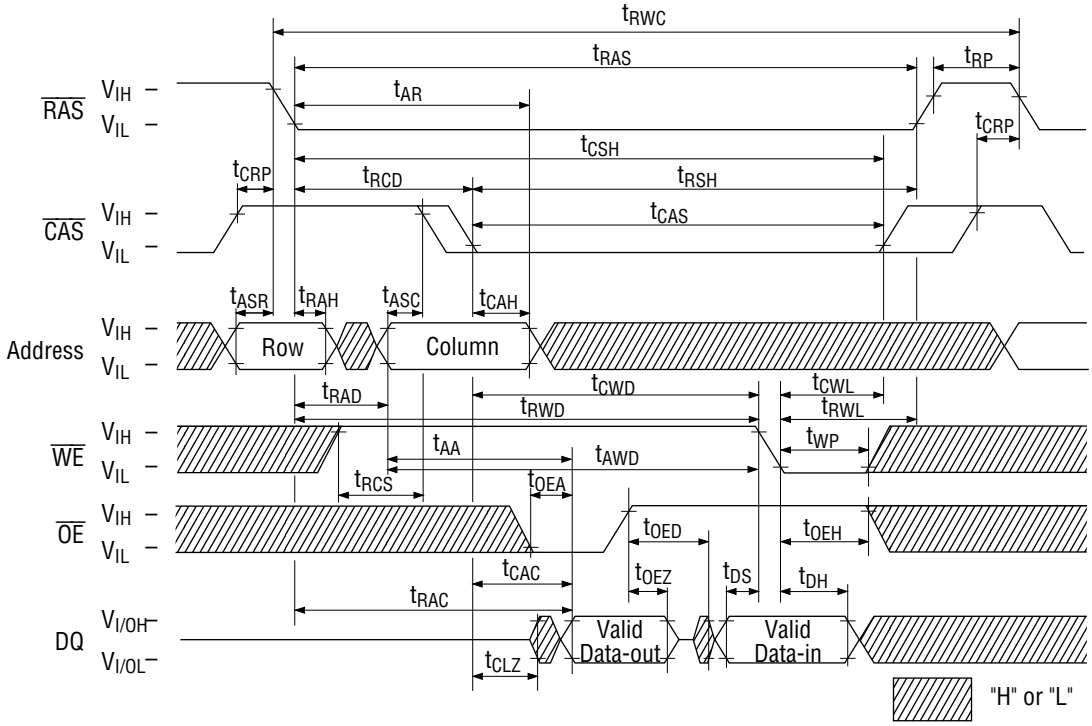
Read Cycle



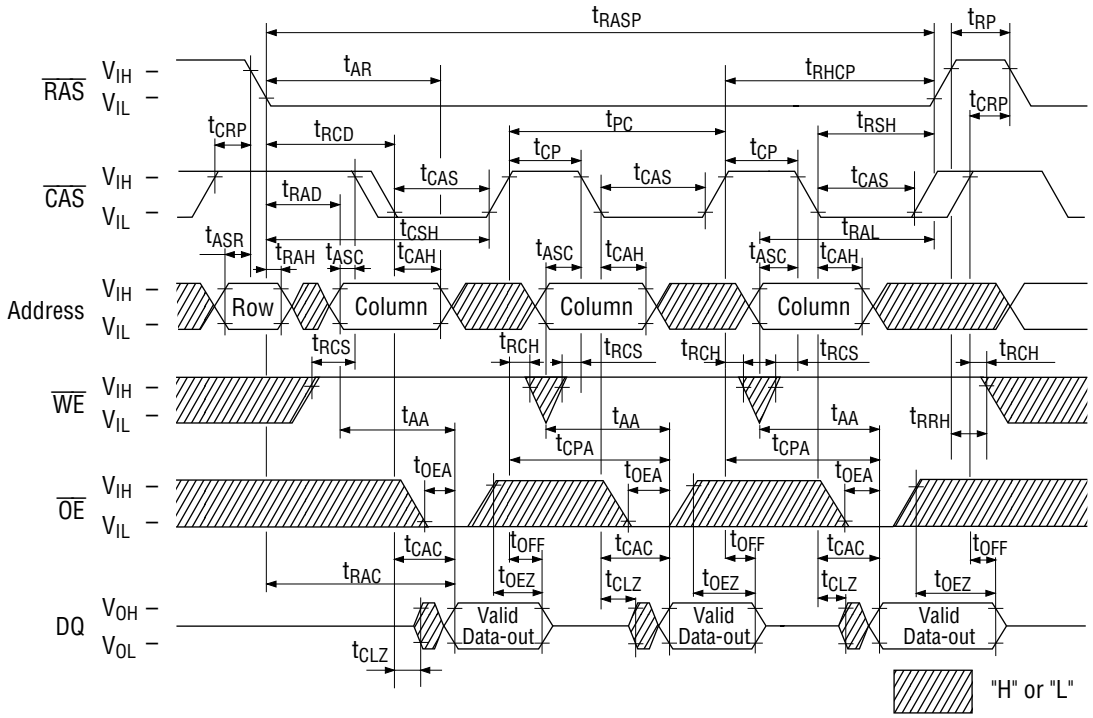
Write Cycle (Early Write)



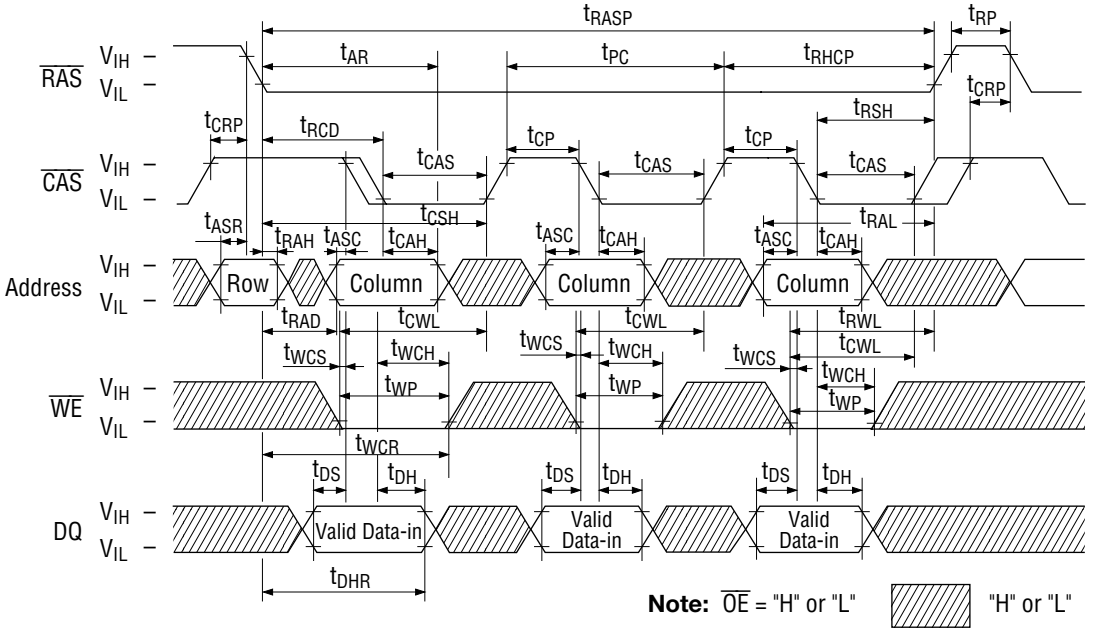
Read Modify Write Cycle



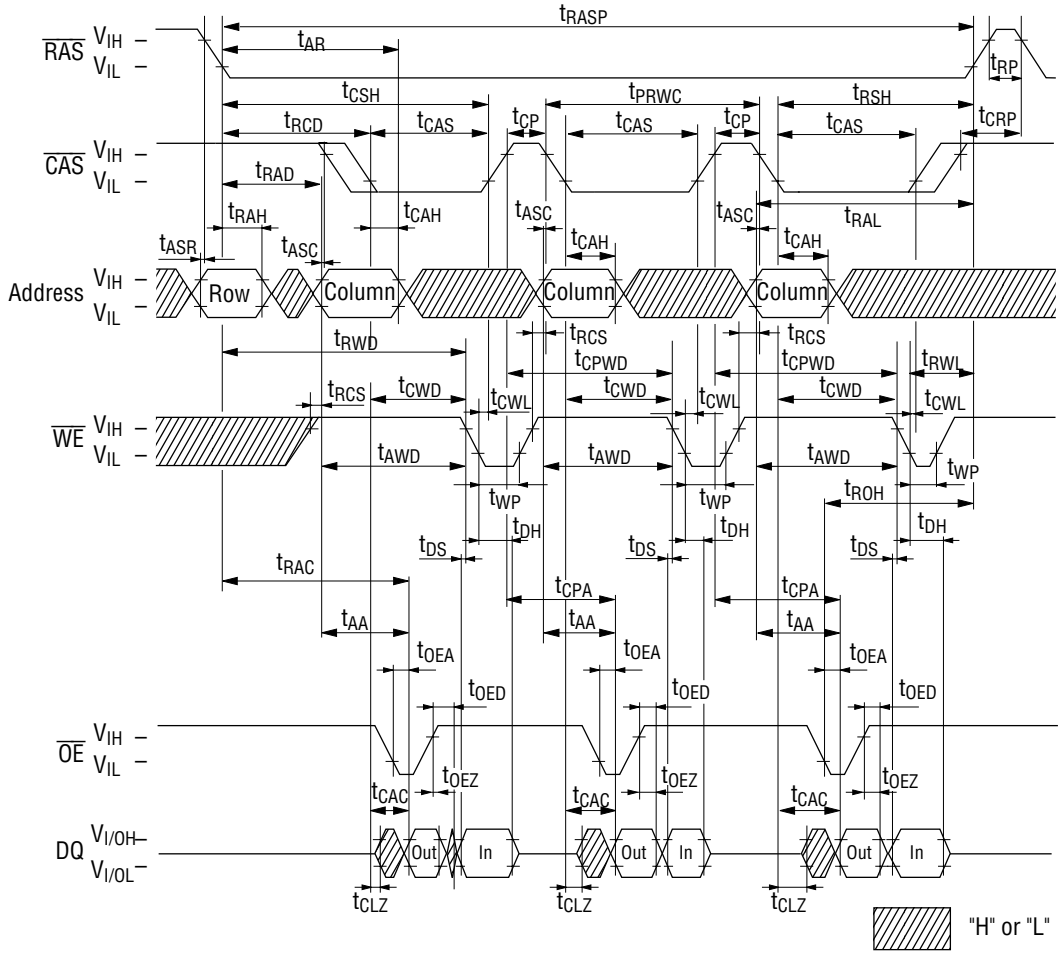
Fast Page Mode Read Cycle



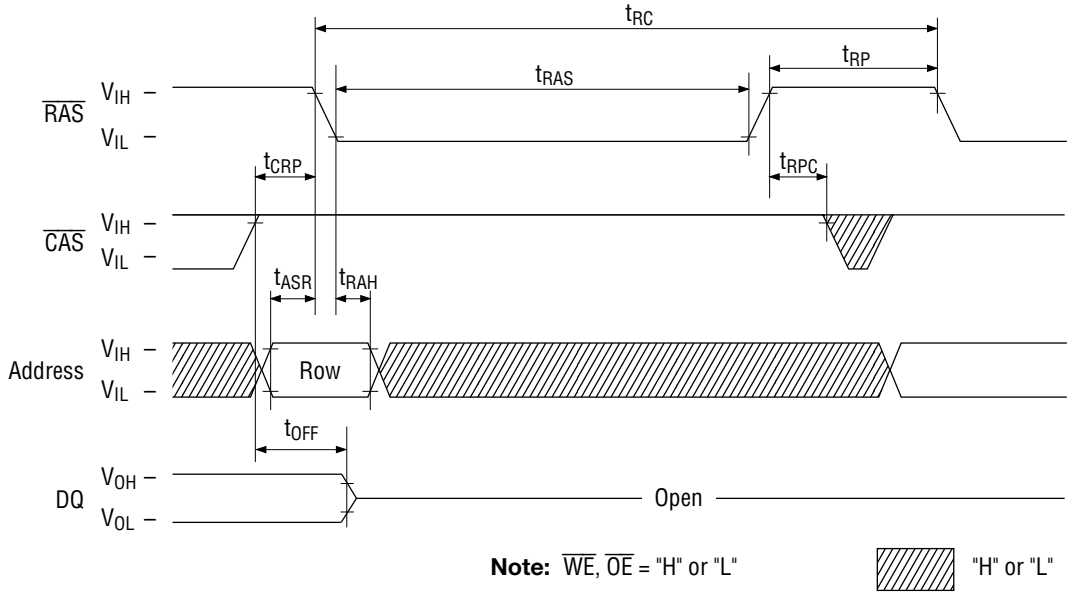
Fast Page Mode Write Cycle (Early Write)



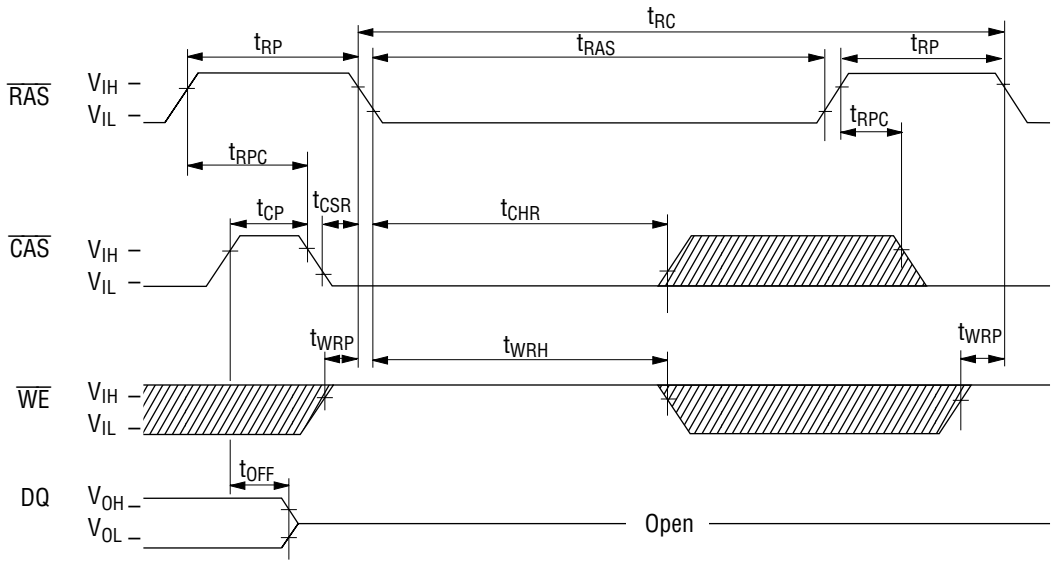
Fast Page Mode Read Modify Write Cycle



RAS-Only Refresh Cycle

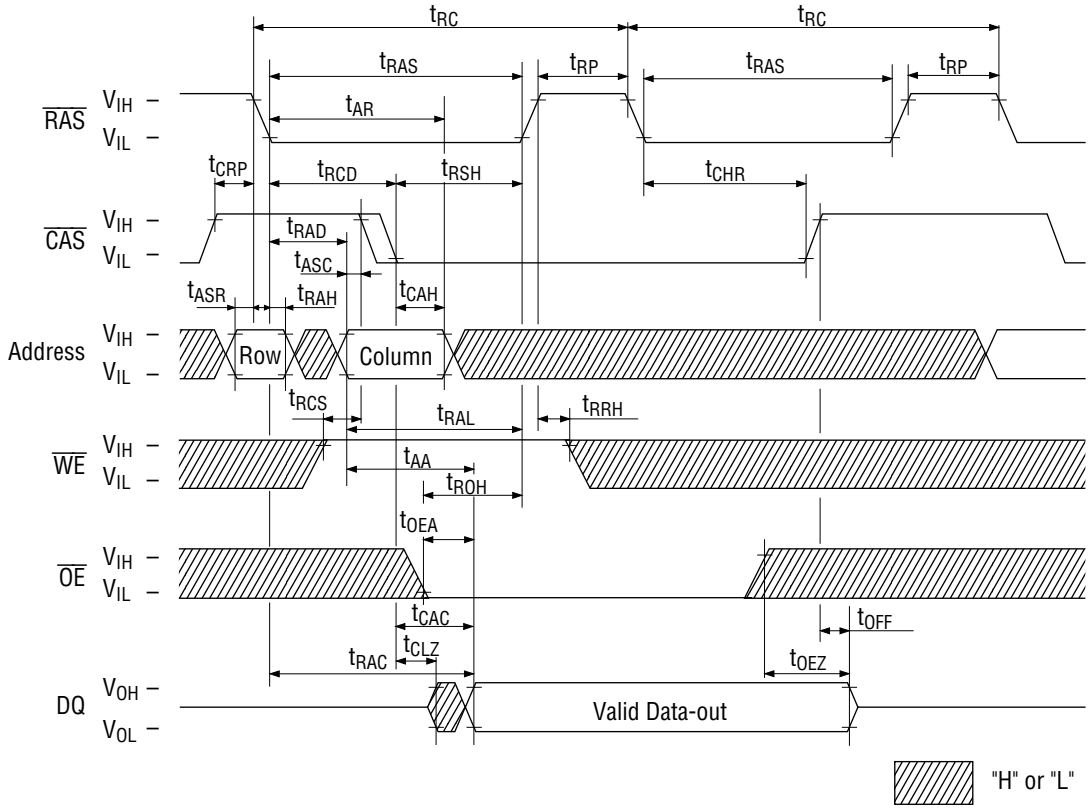


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

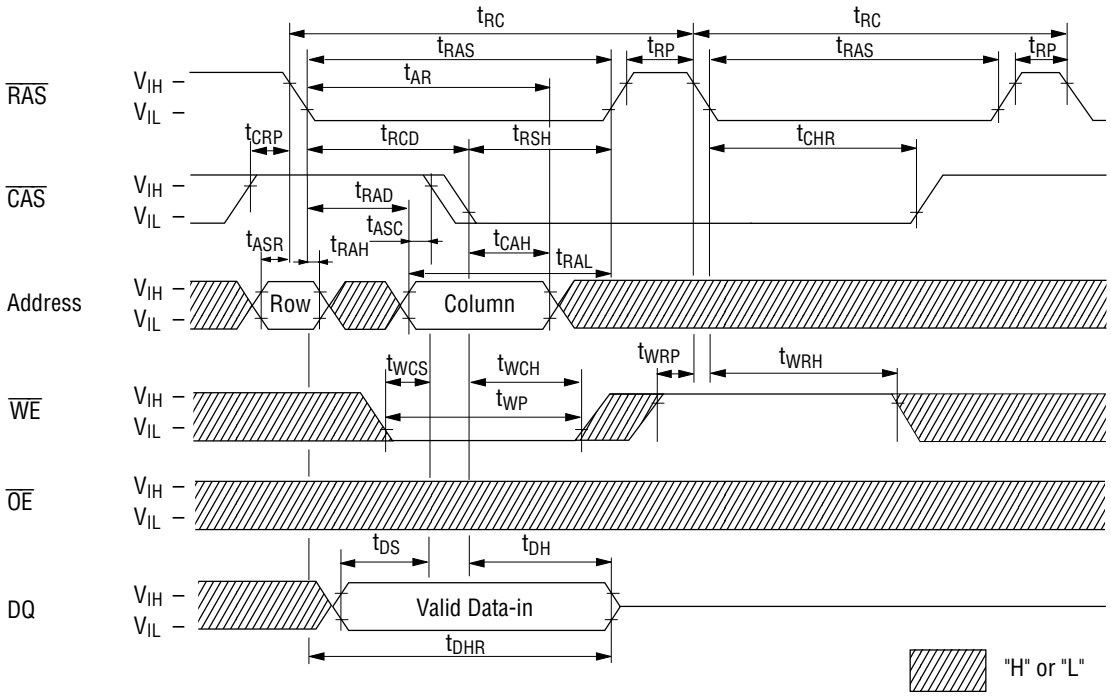


Note: $\overline{OE}$, Address = "H" or "L" "H" or "L"

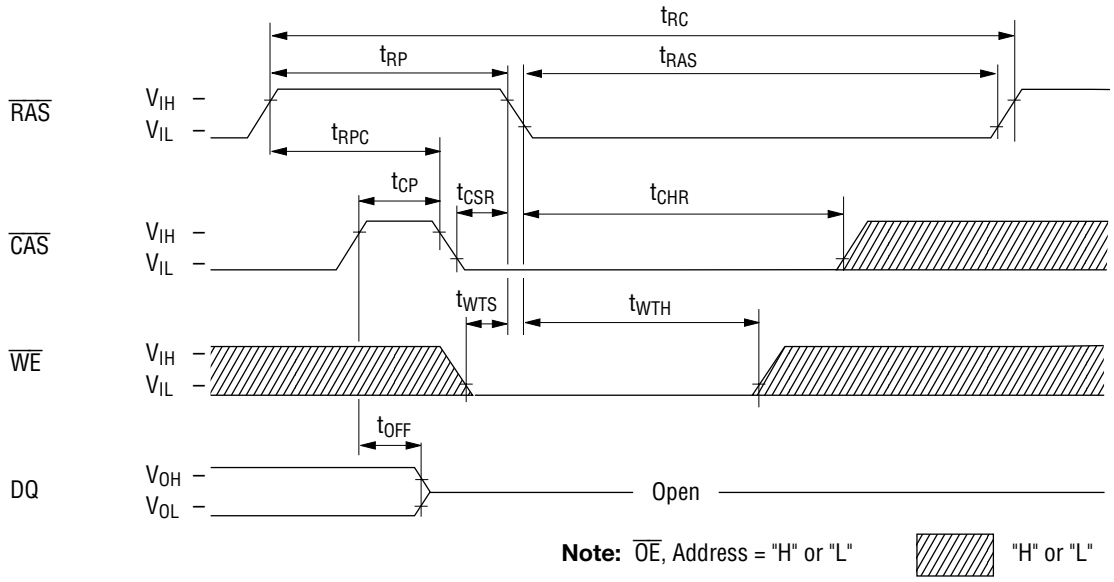
Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



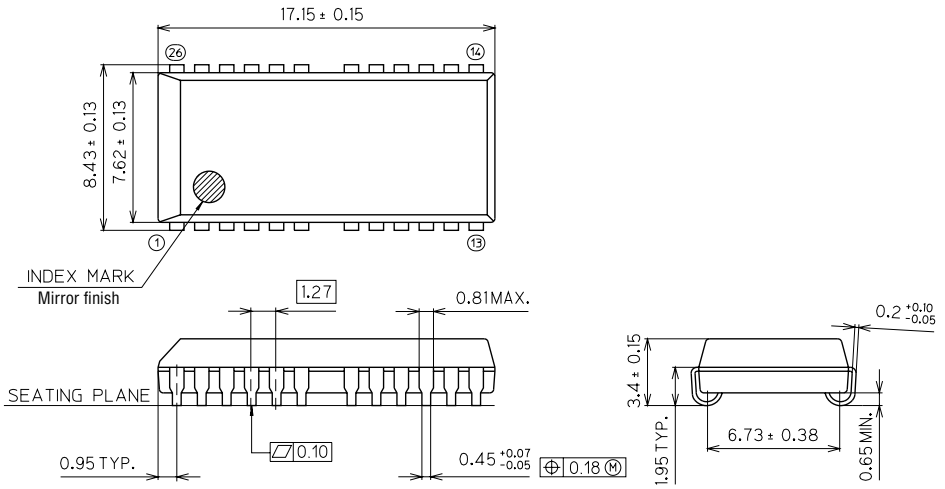
Test Mode Initiate Cycle



PACKAGE DIMENSIONS

(Unit : mm)

SOJ26/24-P-300-1.27



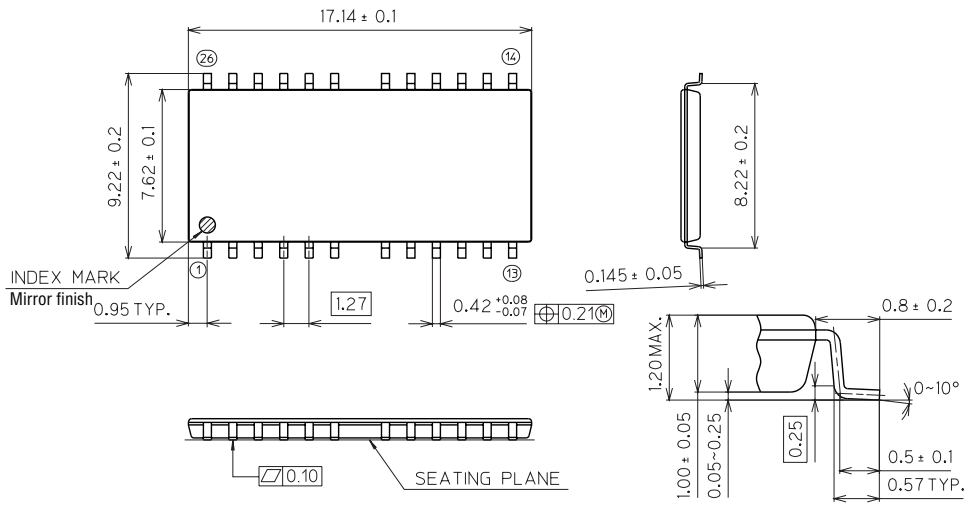
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.80 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TSOPII26/24-P-300-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.29 TYP.

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