

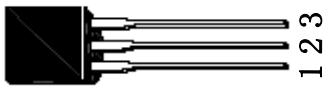
## 1、Description

Designed for use in solid state relays, MPU interface, TTL logic and any other light industrial or consumer application. Supplied in an inexpensive TO-92 package which is readily adaptable for use in automatic insertion equipment. Sensitive Gate Triggering In Four Trigger Modes for all possible Combinations of Trigger Sources, and Especially for Circuits that Source Gate Drives

## 2、Features

- Blocking voltage to 600V
- On-state RMS current to 1.0 A
- Sensitive Gate Triggering in Four Trigger Modes (Quadrants) for all possible Combinations of Trigger Sources, and especially for Circuits that Source Gate Drives
- All Diffused and Glassivated Junctions for Maximum Uniformity of Parameters and Reliability
- Low cost package.

## 3、Pinning information

PIN	Description	Simplified outline	Symbol
1	main terminal 1(T1)	 TO-92	
2	Gate(G)		
3	main terminal 2(T2)		

## 4、Quick reference data

SYMBOL	PARAMETER	MAX	UNIT
$V_{DRM}$ & $V_{RRM}$	Repetitive peak off-state voltages	600	V
$I_T(RMS)$	RMS on-state current	1.0	A
$I_{TSM}$	Non-repetitive peak on-state current	10	A

## 5、Thermal characteristics

SYMBOL	PARAMETER	Value	UNIT
$R_{th(j-c)}$	junction to case(AC)	75	°C/W

## 6. Limiting value

Limiting values in accordance with the Maximum System(IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DRM}$ & $V_{RRM}$	Repetitive peak off-state voltages	$T_j=25^\circ C$	-	-	600	V
$I_{TRMS}$	RMS on-state current	Full Cycle Sine Wave 50 to 60 Hz ( $T_C = 50^\circ C$ )	-	-	1.0	A
$I_{TSM}$	Non-repetitive peak on-state current	One Full Cycle, Sine Wave 50 Hz ( $T_C = 110^\circ C$ )	-	-	10	A
$I^2t$	$I^2t$ for fusing	$t = 8.3 \text{ ms}$	-	-	0.4	$\text{A}^2\text{s}$
$I_{GM}$	Peak gate current		-	-	1.0	A
$V_{GM}$	Peak gate voltage		-	-	5.0	V
$P_{GM}$	Peak gate power		-	-	1.0	W
$P_{G(AV)}$	Average gate power		-	-	0.1	W
$T_{stg}$	Storage temperature		-40	-	150	$^\circ C$
$T_j$	Operating junction temperature		-40	-	125	$^\circ C$

## 7. Characteristics

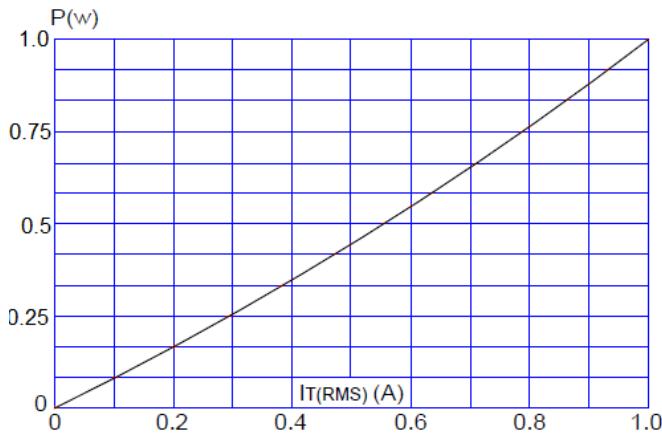
$T_j = 25^\circ C$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static characteristics</b>						
$I_{DRM}$	Peak Repetitive Forward Or Reverse Blocking Current	$V_D=\text{Rated } V_{DRM} \text{ and } V_{RRM}, R_{GK}=1\text{K}\Omega$ $T_C=25^\circ C$ $T_C=110^\circ C$	-	-	5 100	$\mu A$ $\mu A$
$I_{GT}$	Gate trigger current	( $V_D = 12 \text{ Vdc}$ , $R_L = 33 \text{ Ohms}$ ) T2+ G+ T2+ G- T2- G- T2- G+	- - - -	1.5 2.5 2.0 5.0	5 5 5 7	mA mA mA mA
$I_L$	Latching current	$V_D = 12 \text{ V}; I_{GT} = 0.1\text{A}$ T2+ G+ T2+ G- T2- G- T2- G+	- - - -	- - - -	10 20 10 10	mA mA mA mA
$I_H$	Holding current	$I_{TM} = 200 \text{ mA}$ ;	-	2.5	7.0	mA
$V_{TM}$	Peak On-State Voltage	$I_T = 1.1\text{A}$ ; $t_p=380\mu\text{s}$	-	-	1.5	V
$V_{GT}$	Gate trigger voltage	( $V_D = 12 \text{ Vdc}$ , $R_L = 33 \text{ Ohms}$ ) T2+ G+ T2+ G- T2- G- T2- G+	- - - -	- - - -	1.5 1.5 1.5 1.5	V V V V
$V_{GD}$	Off-state leakage Voltage	$V_D = V_{DRM}$ , $R_L = 3.3\text{KOhms}$ , $T_j = 110^\circ C$ ;All Four Quadrants	0.2	-	-	V
<b>Dynamic Characteristics</b>						
$dv/dt(c)$	Critical Rate-of-Rise of Commutation Voltage	$V_D = \text{Rated } V_{DRM}$ , $I_{TM} = .84 \text{ A}$ , Commutating $di/dt = .3 \text{ A/ms}$ , Gate Unenergized, $T_C = 50^\circ C$	1.5	-	-	$\text{V}/\mu\text{s}$
$dv/dt$	Critical Rate of Rise of Off-State Voltage	$V_D = \text{Rated } V_{DRM}$ , $T_C = 110^\circ C$ , Gate Open, Exponential Waveform	5	-	-	$\text{V}/\mu\text{s}$
$t_{gt}$	Gate controlled turn-on time	$V_D = \text{Rated } V_{DRM}$ , $I_{TM} = 1.0 \text{ A pk}$ , $I_G = 25 \text{ mA}$	-	2.0	-	$\mu\text{s}$

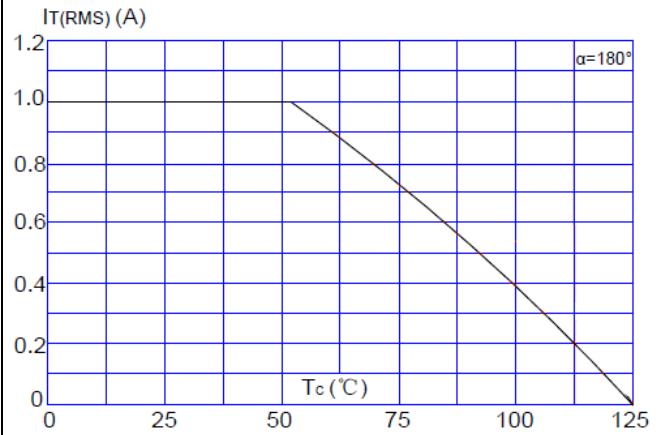
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## 8、Electrical Characteristics Curve

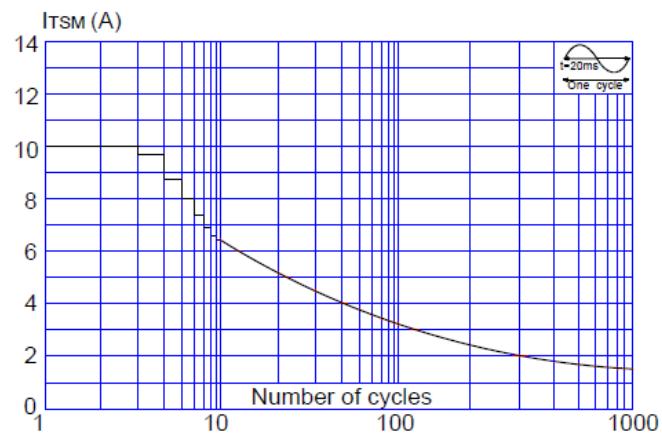
**FIG.1** Maximum power dissipation versus RMS on-state current



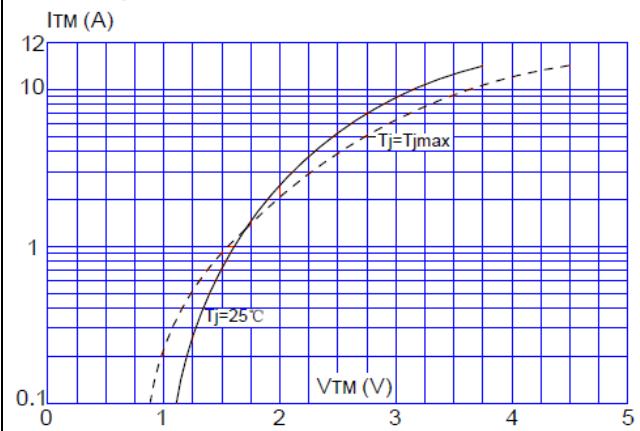
**FIG.2:** RMS on-state current versus case temperature



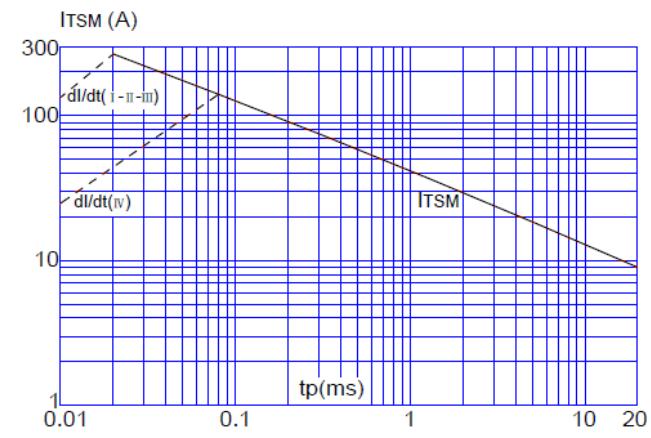
**FIG.3:** Surge peak on-state current versus number of cycles



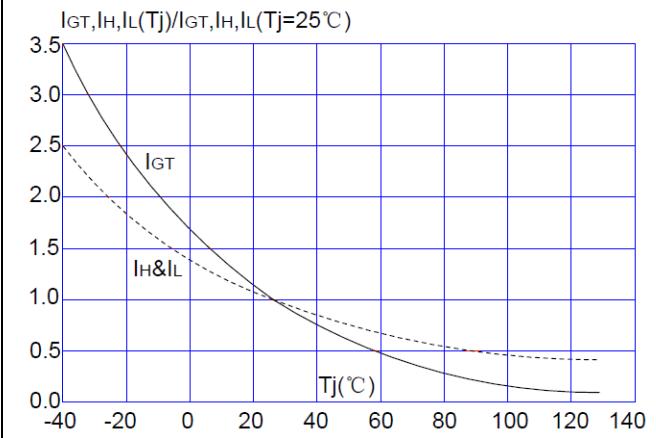
**FIG.4:** On-state characteristics (maximum values)



**FIG.5:** Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 20ms$  ( I - II - III:  $dI/dt < 50A/\mu s$ ; IV:  $dI/dt < 10A/\mu s$  )

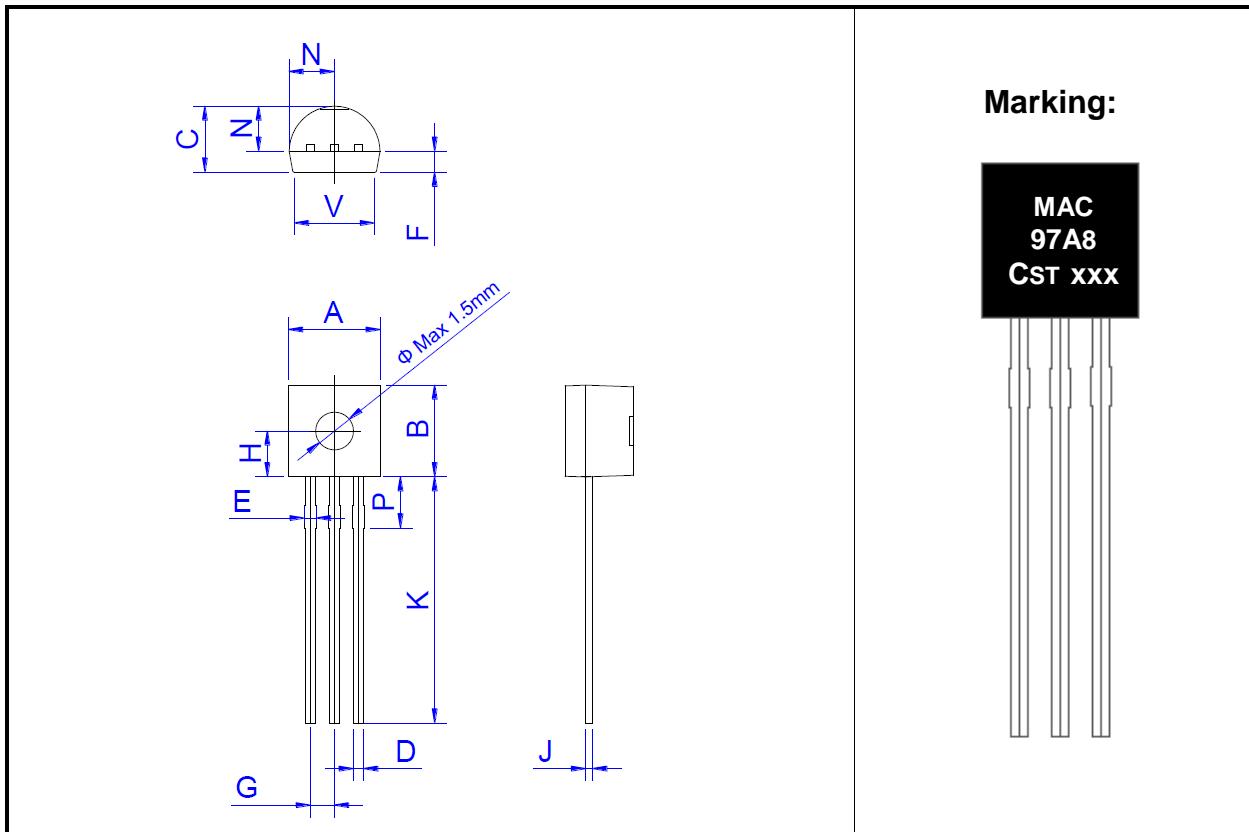


**FIG.6:** Relative variations of gate trigger current, holding current and latching current versus junction temperature



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## 9、Package outline(TO-92)



DIM	Inches			Millimeters		
	Min	Type	Max	Min	Type	Max
A	0.175	-	0.205	4.45	-	5.20
B	0.170	-	0.210	4.32	-	5.33
C	0.125	-	0.165	3.18	-	4.19
D	0.016	-	0.021	0.407	-	0.533
E	0.016	-	0.028	0.40	-	0.70
F	-	0.043	-	-	1.10	-
G	-	0.050	-	-	1.27	-
H	-	0.091	-	-	2.30	-
J	0.013	-	0.018	0.32	-	0.45
K	0.500	-	0.591	12.7	-	15.0
N	0.080	-	0.105	2.04	-	2.66
P	0.073	-	0.081	1.86	-	2.06
V	-	-	0.177	-	-	4.50

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