FLASH-ROM MODULE 2MByte (256K x 64-Bit) ,120PIN SMM,3.3V
Part No. HMF25664F4VP

GENERAL DESCRIPTION

The HMF25664F4VPis a high-speed flash read only memory (FROM) module containing 262,144 words organized in an x64bit configuration. The module consists of four 256K x 16 FROM mounted on a 120-pin, SMM connector FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.
Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.
Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits.
When FROM module is disable condition the module is becoming power standby mode, system designer can get low -power design. All module components may be powered from a single +3.0V DC power supply and all inputs and outputs are LVTTL-compatible

FEATURES

- Access time : 50, 55, 70, 90 and 120ns
- High-density 2MByte design
- High-reliability, low-power design
- Single + 3V ± 0.3V power supply
- Easy memory expansion
- Hardware reset pin(RESET#)
- FR4-PCB design
- 120-Pin Designed by 60-Pin Fine Pitch Connector P1,P2
- Minimum 1,000,000 write cycle guarantee per sector
- 20-year data retention at 125 ^{o}C
- Flexible sector architecture
- Embedded algorithms
- Erase suspend / Erase resume

OPTIONS MARKING

- Timing

50ns access	-50
55ns access	-55
70ns access	-70
90ns access	-90
120ns access	-120

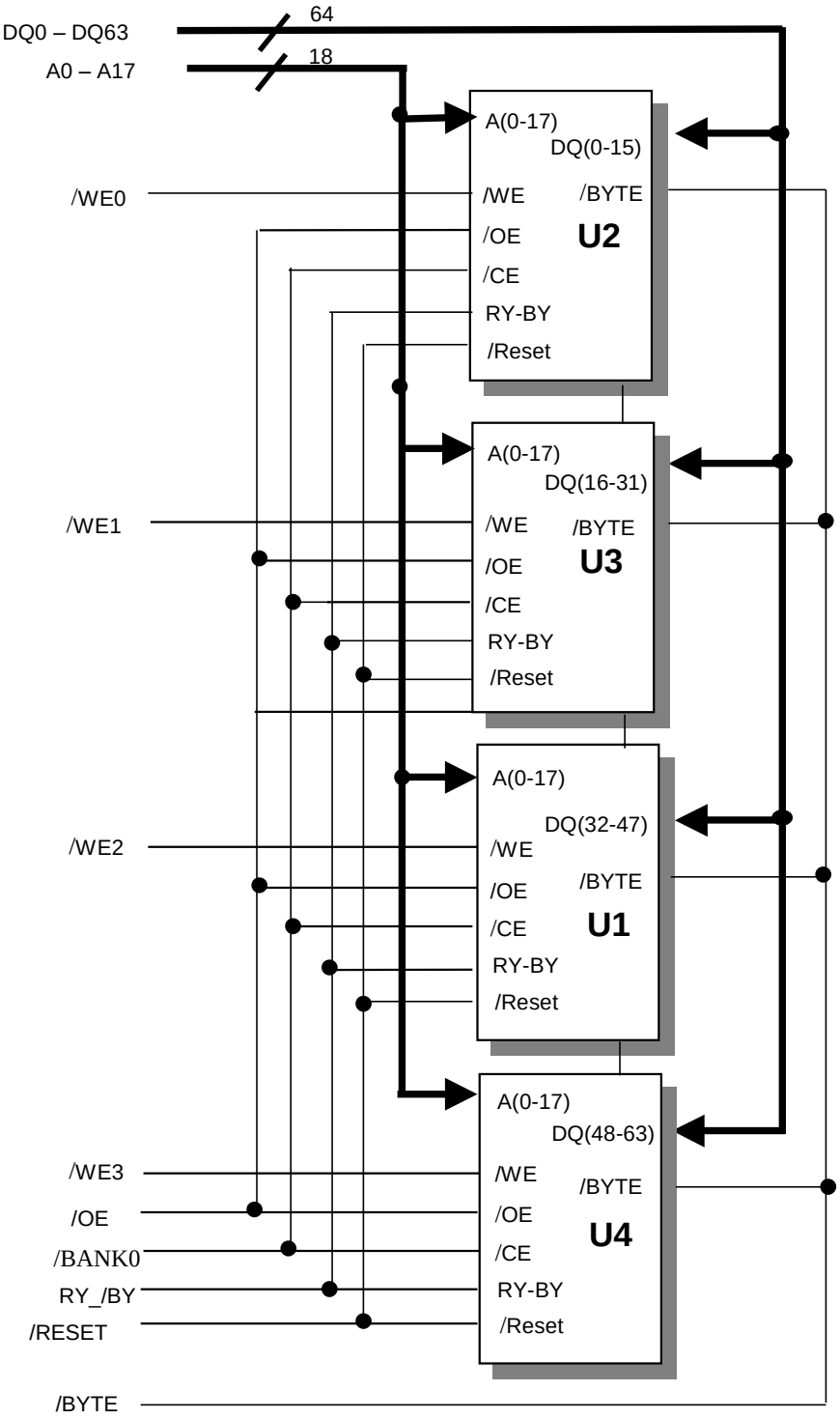
- Packages

120-pin SMM	F

PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vcc	31	Vss	1	Vcc	31	Vss
2	DQ32	32	DQ0	2	DQ16	32	DQ48
3	DQ33	33	DQ1	3	DQ17	33	DQ49
4	DQ34	34	DQ2	4	DQ18	34	DQ50
5	DQ35	35	DQ3	5	DQ19	35	DQ51
6	DQ36	36	DQ4	6	DQ20	36	DQ52
7	DQ37	37	DQ5	7	DQ21	37	DQ53
8	DQ38	38	DQ6	8	DQ22	38	DQ54
9	DQ39	39	DQ7	9	DQ23	39	DQ55
10	Vcc	40	Vss	10	Vcc	40	Vss
11	DQ40	41	DQ8	11	DQ24	41	DQ56
12	DQ41	42	DQ9	12	DQ25	42	DQ57
13	DQ42	43	DQ10	13	DQ26	43	DQ58
14	DQ43	44	DQ11	14	DQ27	44	DQ59
15	DQ44	45	DQ12	15	DQ28	45	DQ60
16	DQ45	46	DQ13	16	DQ29	46	DQ61
17	DQ46	47	DQ14	17	DQ30	47	DQ62
18	DQ47	48	DQ15	18	DQ31	48	DQ63
19	Vcc	49	Vss	19	Vcc	49	Vss
20	A1	50	A10	20	NC	50	NC
21	A2	51	A11	21	A0	51	/BANK0
22	A3	52	A12	22	A16	52	Vss
23	A4	53	A13	23	/WE1	53	/BYTE
24	A5	54	A14	24	/WE2	54	/WE3
25	Vcc	55	Vss	25	Vcc	55	Vss
26	A6	56	A15	26	/OE	56	NC
27	A7	57	A17	27	/RESET	57	NC
28	A8	58	NC	28	/WE0	58	NC
29	A9	59	NC	29	/RY_BY	59	NC
30	Vcc	60	Vss	30	Vcc	60	Vss

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	/RESET	DQ0-DQ7	DQ8-DQ15 /BYTE=V_{IH}
STANDBY	X	Vcc±0.3	X	Vcc±0.3	HIGH-Z	HIGH-Z
NOT SELECTED	H	L	H	H	HIGH-Z	HIGH-Z
READ	L	L	H	H	Dout	Dout
WRITE or ERASE	H	L	L	H	Din	Din

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-0.5V to VCC+0.5V
Voltage with respect to ground Vcc	V_{CC}	-0.5V to +4.0V
Storage Temperature	T_{STG}	-65^{O}C to +150^{O}C
Operating Temperature	T_A	-55^{O}c to +125^{O}C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Vcc for Regulated Voltages Range	V_{CC}	3.0V		3.6V
Vcc for Full Voltages Range	Vcc	2.7V		3.6V
Ground	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS ($0^{O}C \le T_A \le 70\ ^{O}C$; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Load Current	$V_{IN}=V_{SS}$ to Vcc Vcc = Vcc max	I_{L1}		±1.0	µA
Output Leakage Current	Vcc=Vcc max, $V_{OUT}= V_{SS}$ to Vcc	I_{L0}		±1.0	µA
Output High Voltage	I_{OH} = -2.0mA, Vcc = Vcc min	V_{OH1}	0.85V_{CC}		V
	I_{OH} = -100uA, Vcc = Vcc min	V_{OH2}	V_{CC} –0.4		
Output Low Voltage	I_{OL} = 4.0mA, Vcc =Vcc min	V_{OL}		0.45	V
Vcc Active Current for Read(1)	/CE = V_{IL}, /OE=V_{IH},	I_{CC1}	7	12	mA
Vcc Active Current for Program or Erase(2,3)	/CE = V_{IL}, /OE=V_{IH}	I_{CC2}	15	30	mA
Vcc Standby Current(3)	/CE,/RESET= V_{CC} ±0.3V	I_{CC3}	0.2	5	mA
Low Vcc Lock-Out Voltage		V_{LKO}	2.3	2.5	V

Notes: 1. The Icc current listed is typically less than 2mA/MHz, with /OE at V_{IH}. typical V_{CC} is 3.0V.
2. Icc active while embedded algorithm (program or erase) is in progress
3. Maximum Icc current specifications are tested with Vcc=Vcc max

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	0.7	15	Sec	Excludes 00H programming prior to erasure
Byte Programming Time	-	9	300	μs	Excludes system-level overhead
Chip Programming Time	-	11		Sec	Excludes system-level overhead

CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes : Test conditions $T_A = 25^oC$, f=1.0 MHz.

AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP		Speed Options					UNIT
JEDEC	STANDARD				50R	55R	70	90	120	
T_{AVAV}	t_{RC}	Read Cycle Time		Min	50	55	70	90	120	ns
T_{AVQV}	t_{ACC}	Address to Output Delay	/CE = V_{IL} /OE = V_{IL}	Max	50	55	70	90	120	ns
T_{ELQV}	t_{CE}	Chip Enable to Output Delay	/OE = V_{IL}	Max	50	55	70	90	120	ns
T_{GLQV}	t_{OE}	Chip Enable to Output Delay		Max	30	30	30	35	50	ns
T_{EHQZ}	t_{DF}	Chip Enable to Output High-Z		Max	25	25	25	30	30	ns
T_{GHQZ}	t_{DF}	Output Enable to Output High-Z		Max	25	25	25	30	30	ns
T_{AXQX}	t_{QH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First		Min	0	0	0	0	0	ns

Notes : Test Conditions

Output Load : 1TTL gate

Output Load Capacitance

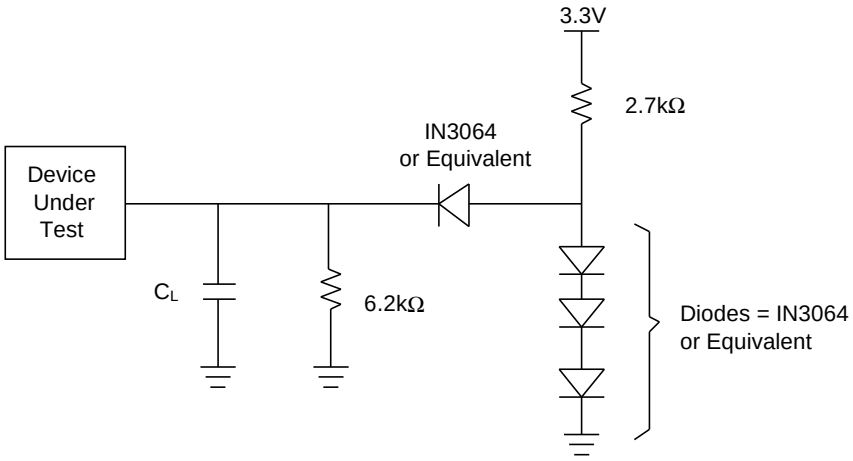
- 50R,55R,70 -30 pF
- 90,120 -30pF

Input rise and fall times : 5 ns

Input pulse levels : 0.0V-3.0V

Timing measurement reference level

- Input : 1.5V
- Output :1.5V



Note : C_L = 100pF including jig capacitance

u Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION		Speed Options					UNIT
JEDEC	STANDARD			50R	55R	70	90	120	
T_{AVAV}	t_{WC}	Write Cycle Time	Min	50	55	70	90	120	ns
T_{AVWL}	t_{AS}	Address Setup Time	Min	0					ns
T_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	45	45	50	ns
T_{DVWH}	t_{DS}	Data Setup Time	Min	45	45	45	45	50	ns
T_{WHDX}	t_{DH}	Data Hold Time	Min	0					ns
	t_{OES}	Output Enable Setup Time	Min	0					ns
T_{GHWL}	t_{GHWL}	Read Recover Time Before write	Min	0					ns
T_{ELWL}	t_{CS}	/CE Setup Time	Min	0					ns
T_{WHEH}	t_{CH}	/CE Hold Time	Min	0					ns
T_{WLWH}	t_{WP}	Write Pulse Width	Min	35	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30					ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	9					µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	0.7					sec
	t_{VCS}	Vcc set up time	Min	50					µs

Notes : 1. This does not include the preprogramming time

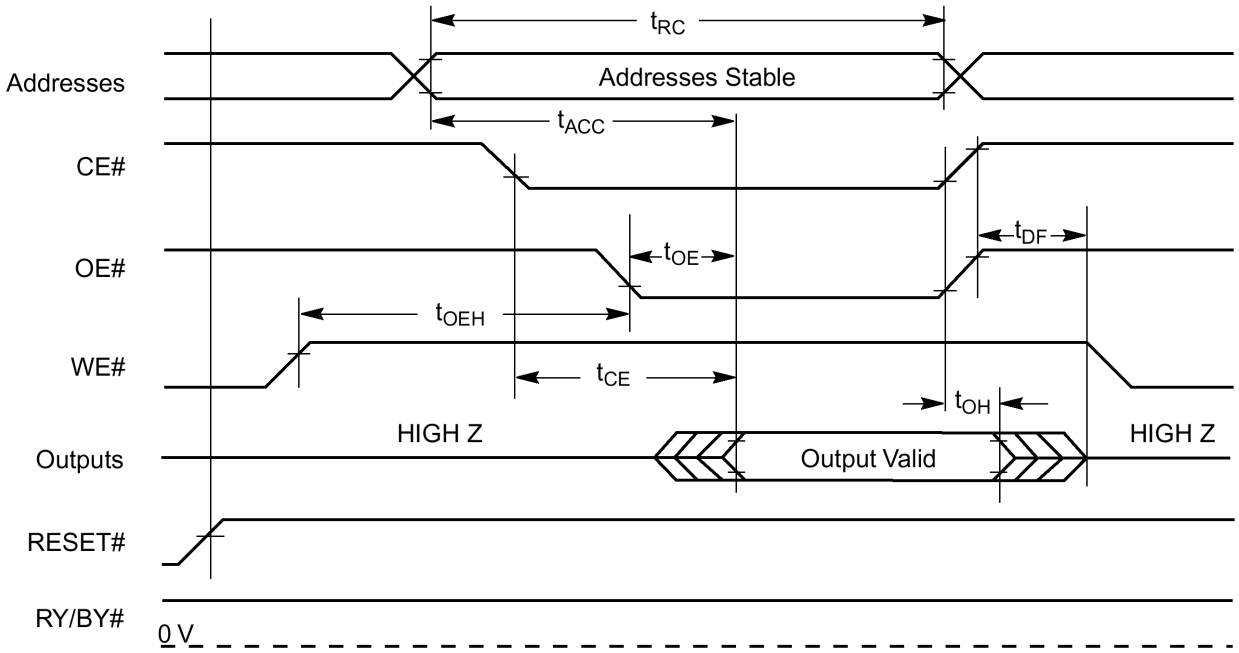
2. This timing is only for Sector Protect operations

u Erase/Program Operations
Alternate /CE Controlled Writes

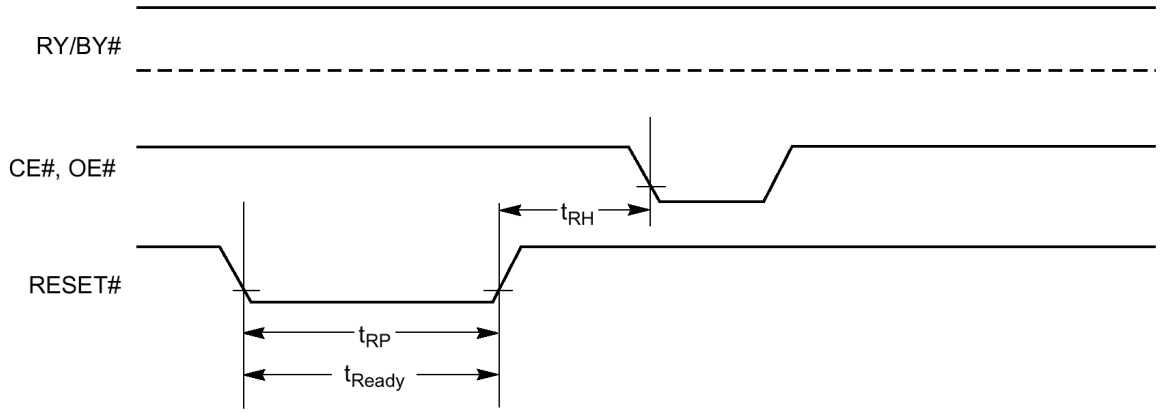
PARAMETER SYMBOLS		DESCRIPTION		SPEED OPTION					UNIT
JEDEC	STANDARD			50R	55R	70	90	120	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	50	55	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0					ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	35	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0					ns
	t_{OES}	Output Enable Setup Time	Min	0					ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min	0					ns
t_{WLEL}	t_{WS}	/WE Setup Time	Min	0					ns
t_{EHWH}	t_{WH}	/WE Hold Time	Min	0					ns
t_{ELEH}	t_{CP}	/CE Pulse Width	Min	35	35	35	35	50	ns
t_{EHEL}	t_{CPH}	/CE Pulse Width High	Min	30					ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	9					µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note)	Typ	0.7					sec

Notes : This does not include the preprogramming time.

u READ OPERATIONS TIMING

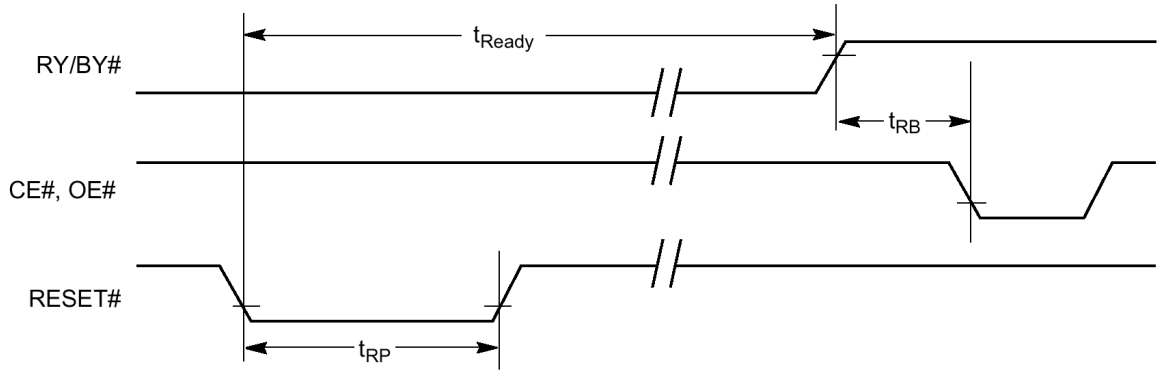


u RESET TIMING

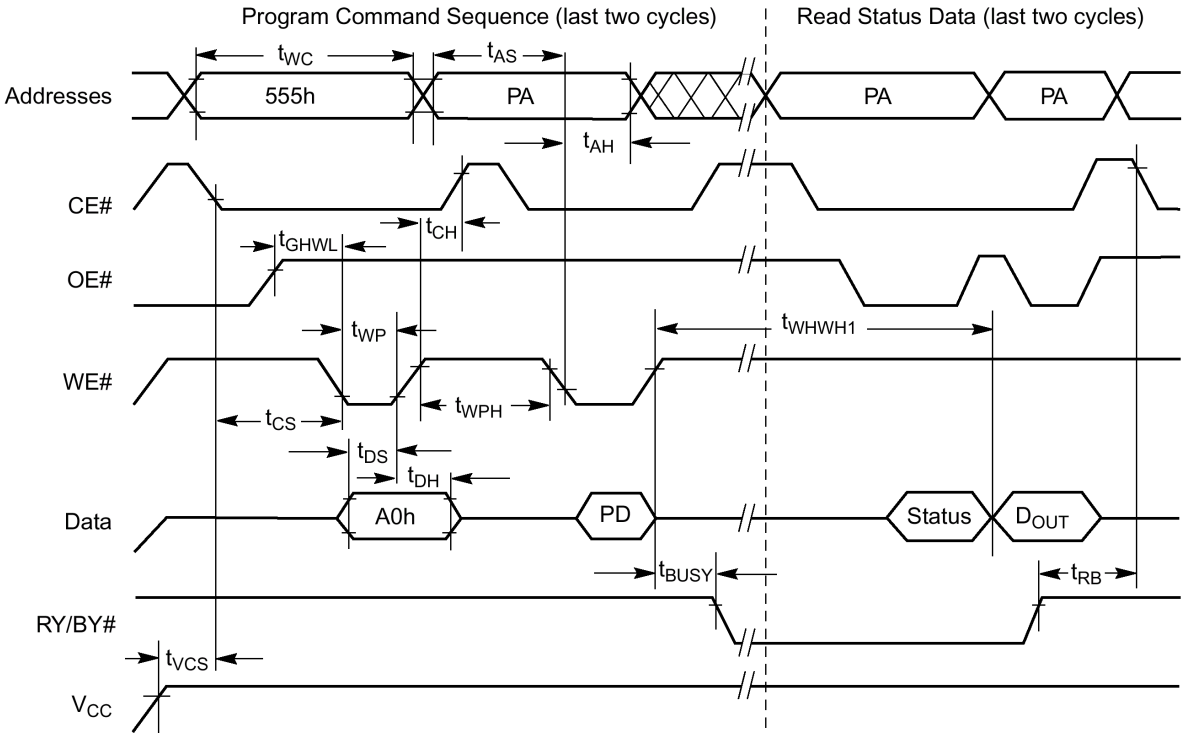


Reset Timings NOT during Embedded Algorithms

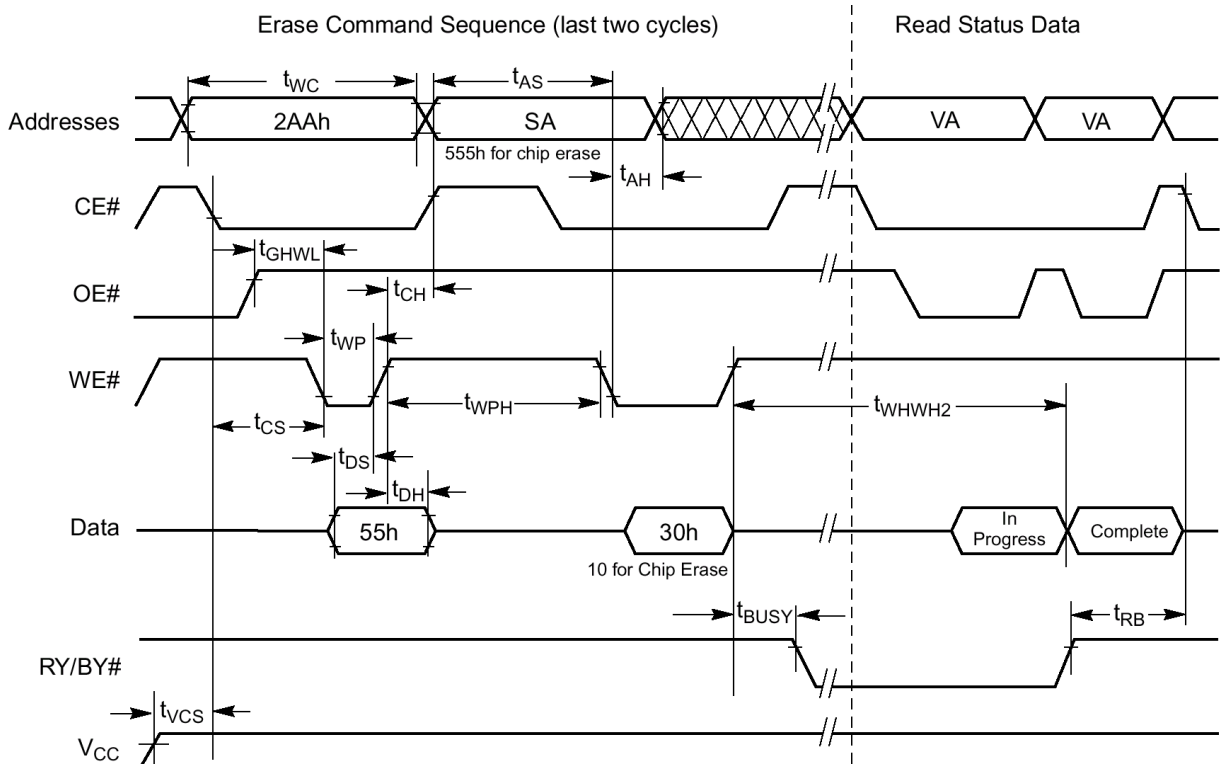
Reset Timings during Embedded Algorithms



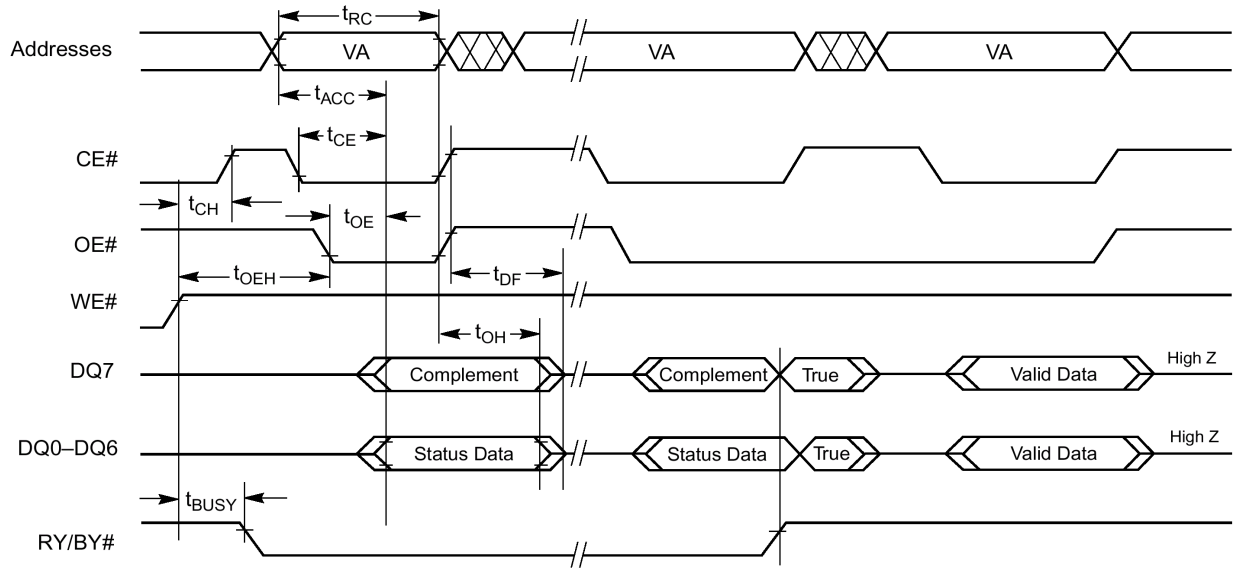
u PROGRAM OPERATIONS TIMING



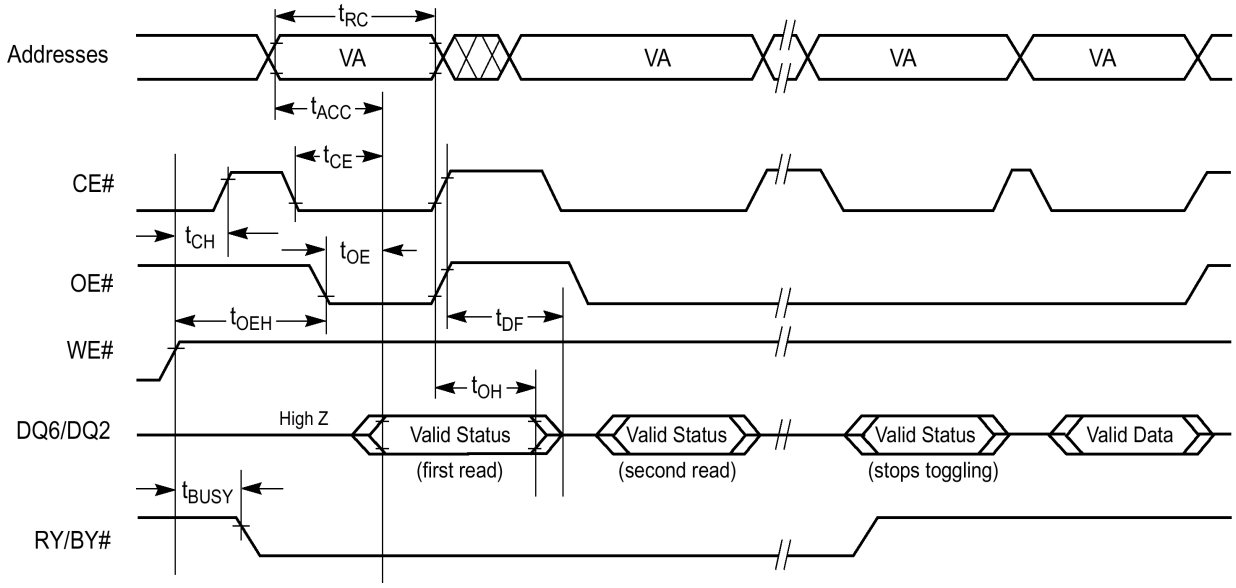
u CHIP/SECTOR ERASE OPERATION TIMINGS



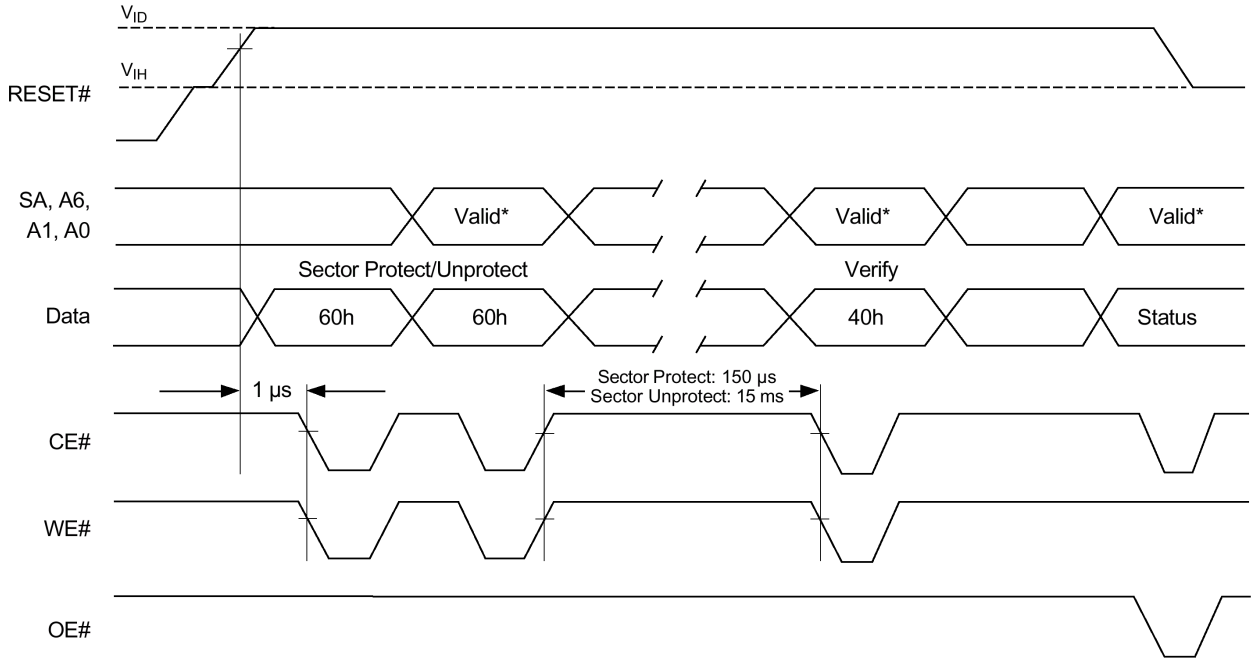
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



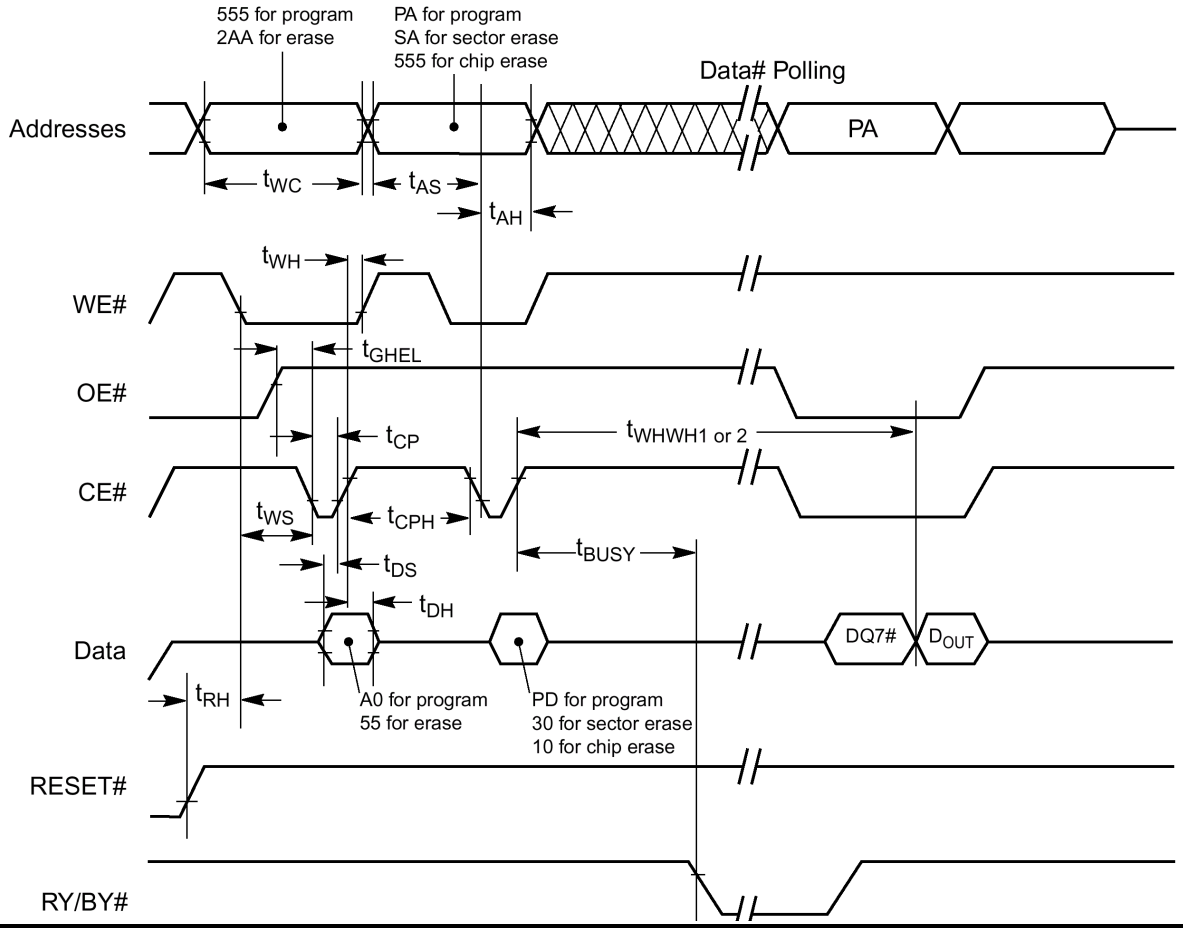
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

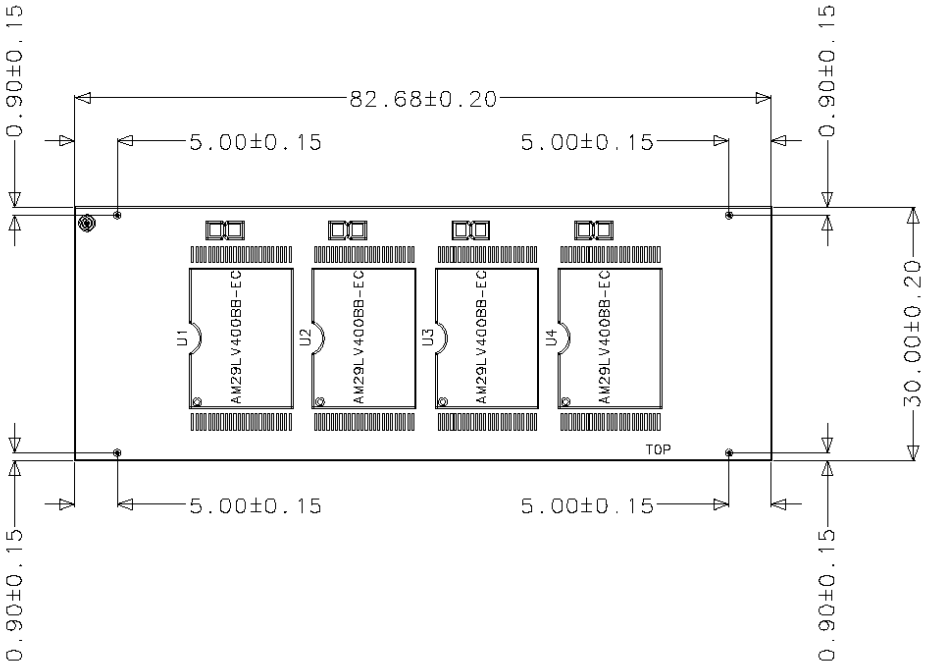


u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS

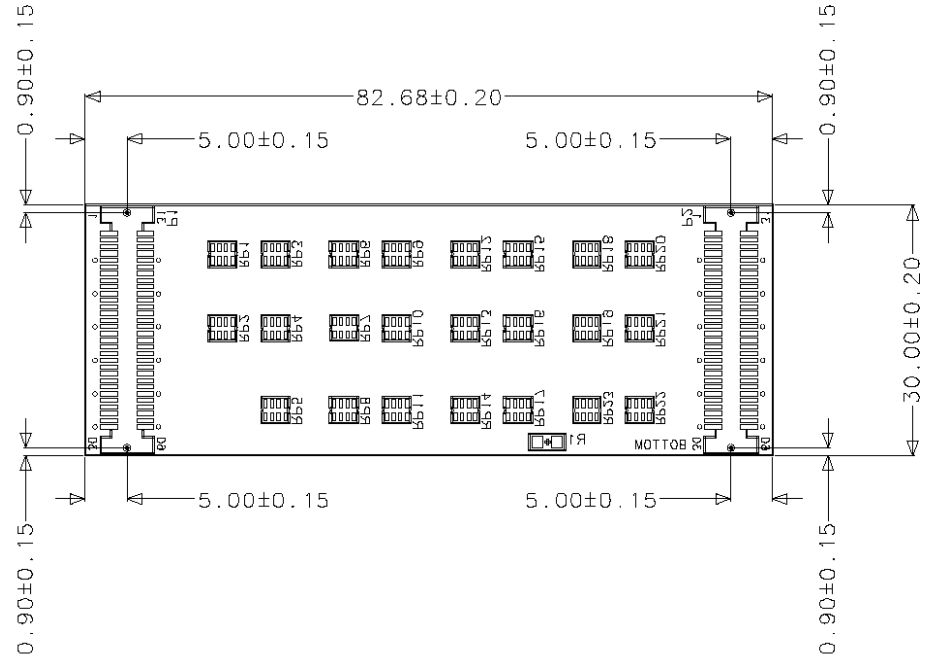


PACKAGE DIMENSIONS

FRONT SIDE



REAR SIDE



ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF25664F4VP-50	2MByte	X 64	120 Pin-SMM	4EA	3.3V	50ns
HMF25664F4VP-55	2MByte	X 64	120 Pin-SMM	4EA	3.3V	55ns
HMF25664F4VP-70	2MByte	X 64	120 Pin-SMM	4EA	3.3V	70ns
HMF25664F4VP-90	2MByte	X 64	120 Pin-SMM	4EA	3.3V	90ns
HMF25664F4VP-120	2MByte	X 64	120 Pin-SMM	4EA	3.3V	120ns

P : PULL UP OF ALL SIGNAL (DATA LINE, ADDRESS LINE, CONTROLL SIGNAL LINE)