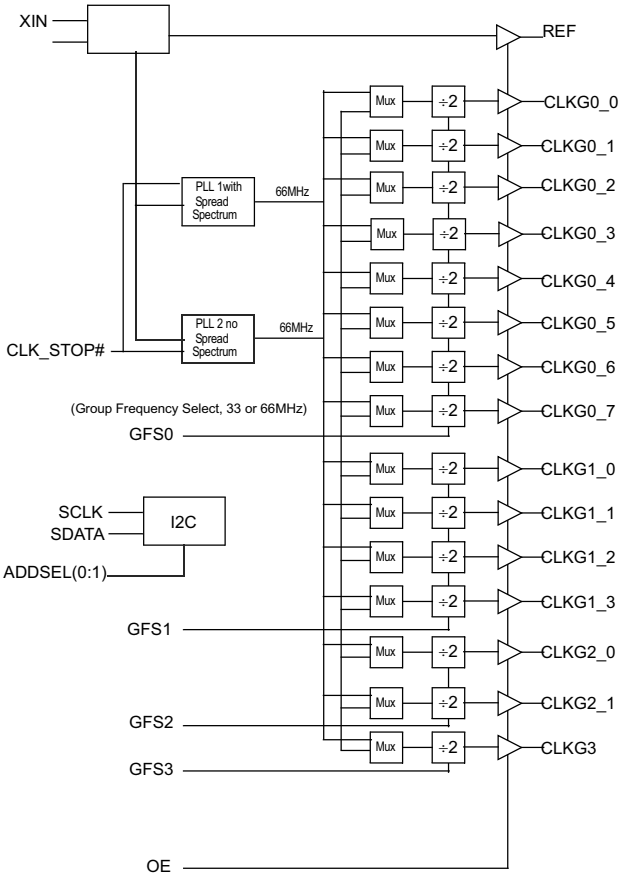
CY28510

Peripheral I/O Clock Generator

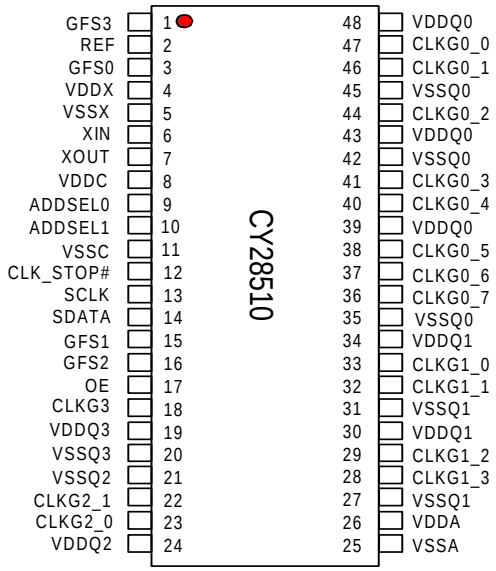
Features

- 15 33.27 MHz or 66.669-MHz clock outputs
- 1 REF 14.318 MHz
- Divide by 2, spread spectrum and output enable all selectable on a per-output basis via I^2C register bits
- Divide by 2 mode default values strappable on a per-group basis
- Output Enable pin controls all outputs
- I^2C Compatible Programmability With Block and Byte Modes
- I^2C Operates Up to 1MHz
- I^2C Address Selection of D0, D2, D4 or D6
- 48-Pin SSOP Package

Block Diagram



Pin Configuration



2200 Laurelwood Road, Santa Clara, CA 95054 Tel:(408) 855-0555 Fax:(408) 855-0550 www.SpectraLinear.com

Pin Description

Pin	Name	Type	Power	Description
2	REF	O	VDDX	Reference Clock: 3.3V 14.318-MHz clock output.
6	XIN	I	VDDX	Crystal Connection or External Reference Frequency Input: This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
7	XOUT	O	VDDX	Crystal Connection for an external 14.318-MHz crystal output.
9	ADDSEL0	I, PU 250 KΩ	VDDC	I^2C address selection. ADDSEL1, ADSEL0: 0,0 = D0; 0,1 = D2, 1,0 = D4, 1,1 = D6
10	ADDSEL1	I, PU 250 KΩ	VDDC	
12	CLK_STOP#	I, PU 250 KΩ	VDDC	Synchronous clock stop pin. When low, all of the clocks except REF are stopped low after completing a normal positive pulse cycle.
13	SCLK	I	VDDC	I^2C compatible SCLOCK.
14	SDATA	I/O	VDDC	I^2C compatible SDATA.
3	GFS0	I, PD 250 KΩ	VDDC	Group frequency select 0. 0 = 33 MHz, 1 = 66 MHz.
15	GFS1	I, PD 250 KΩ	VDDC	Group frequency select 1. 0 = 33 MHz, 1 = 66 MHz.
16	GFS2	I, PD 250 KΩ	VDDC	Group frequency select 2. 0 = 33 MHz, 1 = 66 MHz.
1	GFS3	I, PD 250 KΩ	VDDC	Group frequency select 3. 0 = 33 MHz, 1 = 66 MHz.
17	OE	I, PU 250 KΩ	VDDC	Output enable. 1 = enabled, 0 = disabled (tri-state)
18	CLKG3	O	VSSQ3	Output clock, group 3, 33 or 66 MHz.
22,23	CLKG2_(1:0)	O	VSSQ2	Output clocks, group 2, 33 or 66 MHz.
28,29,32,33	CLKG1_(3:0)	O	VSSQ1	Output clocks, group 1, 33 or 66 MHz.
36,37,38,40,41,44,46,47	CLKG0_(7:0)	O	VSSQ0	Output clocks, group 0, 33 or 66 MHz.
39	VDDQ0_2	PWR		3.3V Power supply for outputs CLKG0_(7:6).
43	VDDQ0_1	PWR		3.3V Power supply for outputs CLKG0_(5:3).
48	VDDQ0_0	PWR		3.3V Power supply for outputs CLKG0_(2:0).
35	VSSQ0	GND		Ground for output buffers CLKG0_(7:6).
42	VSSQ0	GND		Ground for output buffers CLKG0_(5:3).
45	VSSQ0	GND		Ground for output buffers CLKG0_(2:0).
30	VDDQ1	PWR		3.3V Power supply for outputs CLKG1_(3:2).
37	VSSQ1	GND		Ground for output buffers CLKG1_(3:2).
34	VDDQ1	PWR		3.3V Power supply for outputs CLKG1_(1:0).
31	VSSQ1	GND		Ground for output buffers CLKG1_(1:0).
24	VDDQ2	PWR		3.3V Power supply for outputs CLKG2_(1:0).
21	VSSQ2	GND		Ground for output buffers.
19	VDDQ3	PWR		3.3V Power supply for outputs.
20	VSSQ3	GND		Ground for output buffers.
26	VDDA	PWR		3.3V Power supply for analog PLLs.
25	VSSA	GND		Ground for analog PLLs.
4	VDDX	PWR		3.3V Power supply for oscillator.
5	VSSX	GND		Ground for oscillator.
8	VDDC	PWR		3.3V Power supply for core.
11	VSSC	GND		Ground for core.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, yet the interface is available at any time except power-down.

Data Protocol

The clock driver serial protocol accepts Byte Write, Byte Read, Block Write, and Block Read operation from the controller. For Block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*. The Block Write and Block Read protocol is outlined in *Table 2*, while *Table 3* outlines the corresponding byte write and byte read protocol.

The slave receiver address can be D0, D2, D4, or D6 depending on the state of the ADDSEL(0:1) pins.

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte count from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 from master– 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 from master – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data bytes from master/Acknowledge	39:46	Data byte 0 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte 1 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/acknowledge
		....	Data byte N from slave – 8 bits
		....	Not acknowledge
		....	Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not acknowledge
		39	Stop

Serial Control Registers

Byte 0: Clock Enable Register 1

Bit	@Pup	Name	Description
7	1	CLKG0_0	1 = enabled, 0 = tri-state
6	1	CLKG0_1	1 = enabled, 0 = tri-state
5	1	CLKG0_2	1 = enabled, 0 = tri-state
4	1	CLKG0_3	1 = enabled, 0 = tri-state
3	1	CLKG0_4	1 = enabled, 0 = tri-state
2	1	CLKG0_5	1 = enabled, 0 = tri-state
1	1	CLKG0_6	1 = enabled, 0 = tri-state
0	1	CLKG0_7	1 = enabled, 0 = tri-state

Byte 1: Clock Enable Register 2

Bit	@Pup	Name	Description
7	1	CLKG1_0	1 = enabled, 0 = tri-state
6	1	CLKG1_1	1 = enabled, 0 = tri-state
5	1	CLKG1_2	1 = enabled, 0 = tri-state
4	1	CLKG1_3	1 = enabled, 0 = tri-state
3	1	CLKG2_0	1 = enabled, 0 = tri-state
2	1	CLKG2_1	1 = enabled, 0 = tri-state
1	1	CLKG3	1 = enabled, 0 = tri-state
0	1	REF	1 = enabled, 0 = tri-state

Byte 2: Clock Spread Spectrum Control Register

Bit	@Pup	Name	Description
7	0		B2b7, B2b6: 00 = normal, 01 = testb_output, 10 = PD_resetb, 11 = normal
6	0		
5	0	CPNTRL1	Charge Pump Control Bit1. See *Table 4*. Refer to CPNTRL0 in Byte 4, bit 0.
4	0		CLK output strength, 0 = low, 1 = high.
3	0	SWFSEL	0=GFS(3:0) controls output frequency. 1 =I ^{2}C selection of output frequency. Output frequencies should be set in Clock Frequency Select Registers before enabling them.
2	1	MSTRSRD	Master Spread Spectrum Enable. 1 = enabled, 0 = disabled.
1	0	SST1	SST1 Select spread percentage. See *Table 5*
0	0	SST0	SST0 Select spread percentage. See *Table 5*

Table 4. Charge Pump Control [1]

SST1	SST0	% Spread	PLL Bandwidth
0	0	100%	18 to 20 KHz
0	1	114%	21 to 23 KHz
1	0	143%	24 to 26 KHz
1	1	88%	15 to 17 KHz

Table 5. Spread Spectrum Table [2]

SST1	SST0	% Spread
0	0	–0.25% Down spread Lexmark profile
0	1	–0.50% Down spread Lexmark profile
1	0	–1.0% Down spread Lexmark profile
1	1	–1.0% Down spread Linear profile

Notes:
1. The bandwidth of the non-spread PLL is 80 KHz.
2. Glitch free operation for both enabling and disabling Spread Spectrum

Byte 3: Clock Spread Enable Register 1

Bit	@Pup	Name	Description
7	0	CLKG0_0	Spread spectrum control. 0 = disabled, 1 = enabled
6	0	CLKG0_1	Spread spectrum control. 0 = disabled, 1 = enabled
5	0	CLKG0_2	Spread spectrum control. 0 = disabled, 1 = enabled
4	0	CLKG0_3	Spread spectrum control. 0 = disabled, 1 = enabled
3	0	CLKG0_4	Spread spectrum control. 0 = disabled, 1 = enabled
2	0	CLKG0_5	Spread spectrum control. 0 = disabled, 1 = enabled
1	0	CLKG0_6	Spread spectrum control. 0 = disabled, 1 = enabled
0	0	CLKG0_7	Spread spectrum control. 0 = disabled, 1 = enabled

Byte 4: Clock Spread Enable Register 2

Bit	@Pup	Name	Description
7	0	CLKG1_0	Spread spectrum control. 0 = disabled, 1 = enabled
6	0	CLKG1_1	Spread spectrum control. 0 = disabled, 1 = enabled
5	0	CLKG1_2	Spread spectrum control. 0 = disabled, 1 = enabled
4	0	CLKG1_3	Spread spectrum control. 0 = disabled, 1 = enabled
3	0	CLKG2_0	Spread spectrum control. 0 = disabled, 1 = enabled
2	0	CLKG2_1	Spread spectrum control. 0 = disabled, 1 = enabled
1	0	CLKG3	Spread spectrum control. 0 = disabled, 1 = enabled
0	0	CPNTRL0	Charge Pump Control Bit1. See *Table 4*. Refer to CPNTRL1 in Byte 2, bit 5.

Byte 5: Clock Frequency Select Register 1

Bit	@Pup	Name	Description
7	0	CLKG0_0	Frequency select. 0 = 33 MHz, 1 = 66 MHz
6	0	CLKG0_1	Frequency select. 0 = 33 MHz, 1 = 66 MHz
5	0	CLKG0_2	Frequency select. 0 = 33 MHz, 1 = 66 MHz
4	0	CLKG0_3	Frequency select. 0 = 33 MHz, 1 = 66 MHz
3	0	CLKG0_4	Frequency select. 0 = 33 MHz, 1 = 66 MHz
2	0	CLKG0_5	Frequency select. 0 = 33 MHz, 1 = 66 MHz
1	0	CLKG0_6	Frequency select. 0 = 33 MHz, 1 = 66 MHz
0	0	CLKG0_7	Frequency select. 0 = 33 MHz, 1 = 66 MHz

Byte 6: Clock Frequency Select Register 2

Bit	@Pup	Name	Description
7	0	CLKG1_0	Frequency select. 0 = 33 MHz, 1 = 66 MHz
6	0	CLKG1_1	Frequency select. 0 = 33 MHz, 1 = 66 MHz
5	0	CLKG1_2	Frequency select. 0 = 33 MHz, 1 = 66 MHz
4	0	CLKG1_3	Frequency select. 0 = 33 MHz, 1 = 66 MHz
3	0	CLKG2_0	Frequency select. 0 = 33 MHz, 1 = 66 MHz
2	0	CLKG2_1	Frequency select. 0 = 33 MHz, 1 = 66 MHz
1	0	CLKG3	Frequency select. 0 = 33 MHz, 1 = 66 MHz
0	0	DAFEN	M and N register mux selection. 0 = M and N values come from the ROM. 1 = data is loaded from the DAF registers into M and N.

Byte 7: Dial-a-Frequency® Control Register N [default = 66.669 MHz, N = 149d, M = 8d]

Bit	@Pup	Description
7	1	N7, MSB
6	0	N6
5	0	N5
4	1	N4
3	0	N3
2	1	N2
1	0	N1
0	1	N0, LSB

Dial-a-Frequency Operation

VCO Frequency = (14.318180 MHz) x (N/ M)

Output1 = VCO/4 = 66.669 MHz

Output2 = VCO/8 = 33.335 MHz

To operate the Dial-a-Frequency feature, you must select the individual output that is to be modified by selecting the Spread spectrum control enable bit in the Clock Spread Enable Registers to multiplex the SS PLL as the input source, which is the only PLL that can have the “N” register value changed. Then you must disable spread spectrum by setting MSTRSRD in the Clock Spread Spectrum Control Register (Byte 2, bit 2) to 0 so that the spread PLL is not being modulated. It is then possible to change the N value from it’s default value of 149 to any value within ±25%. You must also set the DAFEN bit to a 1 in Byte 6, bit 0 to enable the Dial-a-Frequency feature. Please note that the long-term or accumulated jitter will be about 3nsec, which does not affect the operation of the device since only Cycle-to-Cycle jitter can cause system problems.

Crystal Recommendations

The CY28510 requires a **Parallel Resonance Crystal.** Substituting a series resonance crystal will cause the CY28510 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading. See *Table 6*.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL). The following diagram shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It’s a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal.

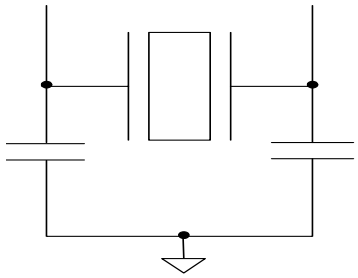


Figure 1. Crystal Capacitive Clarification

Table 6. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	50 ppm	50 ppm	5 ppm

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be 2 times the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

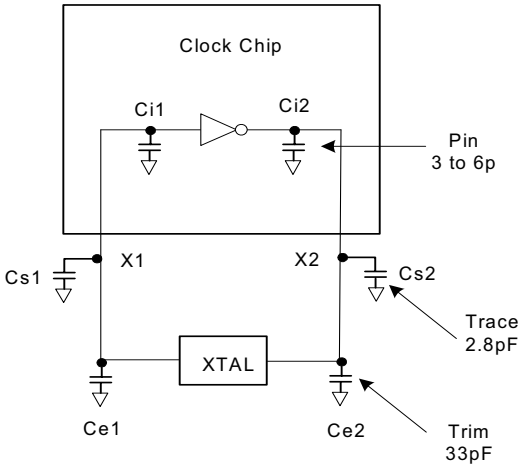


Figure 2. Crystal Loading Example

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be 2 times the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitance loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL ..... Crystal load capacitance

CLeActual loading seen by crystal using standard value trim capacitors

Ce .....External trim capacitors

Cs .....Stray capacitance (trace,etc)

Ci .....Internal capacitance (lead frame, bond wires etc)

Layout and Decoupling Consideration

The V_{DD} nets for each of the subgroups within each group are not connected internally. What this implies is that each group should have a separate V_{DD} pool and it's own 0.1 µF capacitor. The more you can avoid external coupling across VDD planes, the better each sub-net can operate at a different frequency, whether jitter is on or off, or it is at a different frequency.

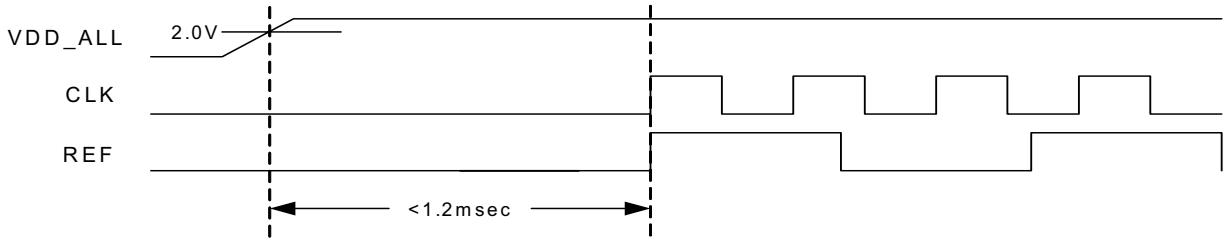


Figure 3. Power-up Signal Timing

CLK_STOP# Clarification

The CLK_STOP# signal is an active low input used for synchronous stopping and starting the CLK output clocks while the rest of the clock generator continues to function.

CLK_STOP# Assertion

When CLK_STOP# pin is asserted low, all CLK outputs will be stopped after being sampled by two rising CLK internal clock edges.

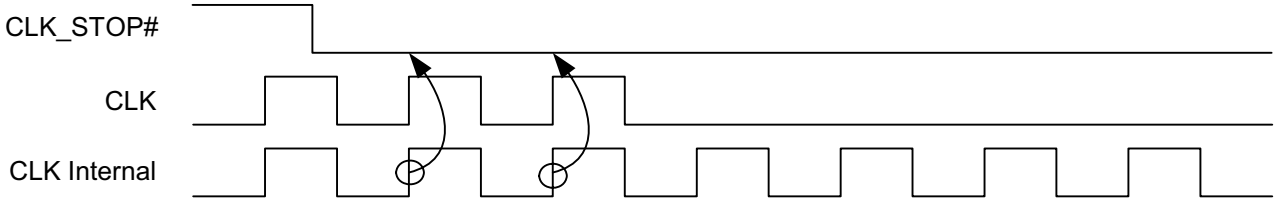


Figure 4. CLK_STOP# Assertion Waveforms

CLK_STOP# Deassertion

The deassertion of the CLK_STOP# signal will cause all CLK outputs that were stopped to resume normal operation in a synchronous manner, synchronous manner meaning that no short or stretched clock pulses will be produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than 2 CLK clock cycles

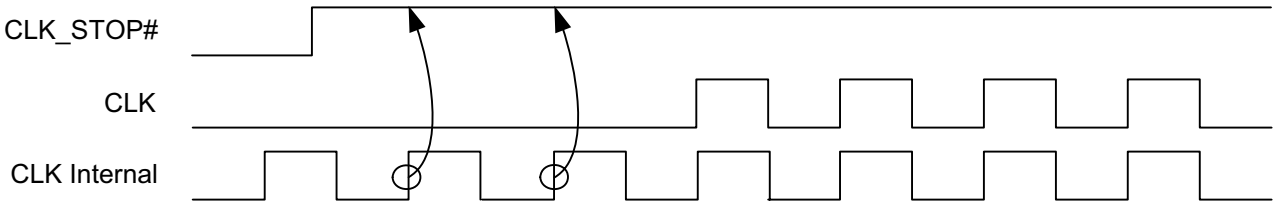


Figure 5. CLK_STOP# Deassertion Waveforms

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}, V_{DDC}, V_{DDA}	3.3V Supply Voltage	Maximum functional voltage	–0.5	5.5	V
V_{DDQ}	Output Buffer Supply Voltage	Maximum functional voltage	–0.5	5.5	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non Functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional		150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1		15	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)		45	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL–94	Flammability Rating	@1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

DC Electrical Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}, V_{DDC}, V_{DDA}	3.3V Supply Voltage	Maximum operating voltage	3.135	3.3	3.465	V
V_{DDQ}	Output Buffer Supply Voltage	Maximum operating voltage	3.135	3.3	3.465	V
V_{IL}	Input Low Voltage		–	–	0.8	Vdc
V_{IH}	Input High Voltage		2.0	–	–	Vdc
I_{ILC}	Input Leakage Current	Except for internal pull-up or pull-down resistors	–5	–	5	µA
I_{IL}	Input Low Current (@V_{IL} = V_{SS})	For internal pull-up resistors	9	–	–	µA
I_{IH}	Input High Current (@V_{IL} =V_{DD})	For internal pull-down resistors	–9	–	–	µA
V_{OL}	Output Low Voltage		–	–	0.4	Vdc
V_{OH}	Output High Voltage		2.4	–	–	Vdc
Ioz	Tri-State leakage Current		–	–	10	µA
C_{IN}	Input pin capacitance		–	–	5	pF
C_{OUT}	Output pin capacitance		–	–	6	pF
L_{IN}	Input pin Inductance		–	–	7	pF
C_{XTAL}	Crystal pin capacitance	Measured from the Xin or Xout to V_{SS}	–	–	5	pF
I_{DD1}	3.3V Core Supply Current	All outputs disabled running at the default frequency	–	61.80	–	mA
I_{DD2}	3.3V REF Supply Current	REF buffer with load from *Table 7,* running at the default frequency	–	4.15	–	mA
I_{DD3}	3.3V CPU Supply Current	1 CLK buffer with load from *Table 7,* running at the default frequency	–	11.81	–	mA
I_{DD4}	3.3V VDDA Supply Current	Running at the default frequency	–	12	–	mA

AC Electrical Specifications

Parameter	Description	Condition	66 MHz			Unit
			Min.	Typ.	Max.	
CLK						
F_{VCO}	VCO Frequency Range	Measured at 1.5V	200	–	333	MHz
T_{DC}	CLK Duty Cycle	Measured at 1.5V	45	–	55	%
T_{RISE}/T_{FALL}	CLK Rise and Fall Times	Measured from 0.4V to 2.4V	0.5	–	3.0	ns
T_{GSKEW1}	Any CLK to Any CLK Clock Skew within a Group	Measured at 1.5V, with Spread Spectrum disabled.	–	–	150	ps
T_{GSKEW2}	Any CLK to Any CLK Clock Skew within any Group	Measured at 1.5V, with Spread Spectrum disabled.	–	–	150	ps
T_{CCJ1}	CLK Cycle-to-Cycle Jitter	Measured at 1.5V and all CLKs running the same frequency with Spread Spectrum disabled.	–	–	150	ps
T_{CCJ2}	CLK Cycle-to-Cycle Jitter	Measured at 1.5V and all CLKs running the same frequency with Spread Spectrum enabled	–		200	ps
T_{CCJ3}	CLK Cycle-to-Cycle Jitter	Measured at 1.5V with CLKs running different frequencies but the same frequency within a Group and Sub-group and Spread Spectrum disabled	–	–	200	ps
T_{CCJ4}	CLK Cycle-to-Cycle Jitter	Measured at 1.5V with CLKs running different frequencies including within a Sub-group and Spread Spectrum disabled	–	–	400	ps
T_{CCJ5}	CLK Cycle-to-Cycle Jitter	Measured at 1.5V with CLKs running different frequencies including within a Sub-group and Spread Spectrum enabled	–	–	600	ps
SCLK						
T_{I2C}	I^2C Clock Period	Measured at 1.5V	1.0	–	–	us
REF						
Xin	XIN being driven by an external clock source		10	–	18	MHz
T_{DC}	REF Duty Cycle	Measured at 1.5V, See *Figure 3*	45	–	55	%
T_{RISE}/T_{FALL}	REF Rise and Fall times	Measured from 0.4V to 2.4V, See *Figure 3*	1	–	4	ns
T_{CCJ}	REF Cycle-to-Cycle Jitter	Measured at 1.5V, See *Figure 3*	–	450	1000	ps
T_{XS}	Power-on Hold Off	Outputs will be as shown in *Figure 3*	–	–	1.2	ms

Table 7. Signal Loading Table

Clock Name	Max Load (pF)
CLK	22
REF	15

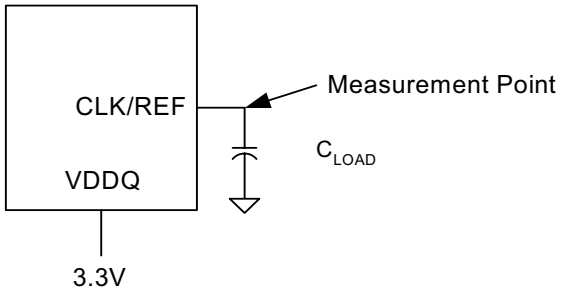


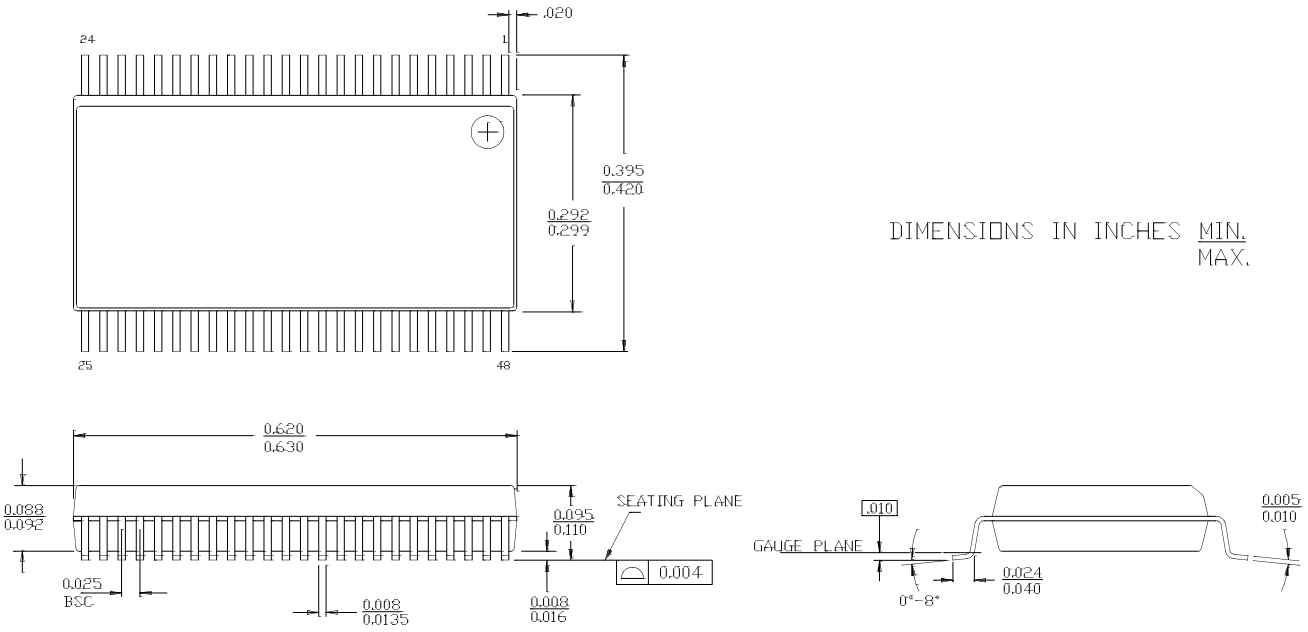
Figure 6. Output Test Loading

Ordering Information

Part Number	Package Type	Product Flow
CY28510OC	48-pin Shrunk Small Outline package (SSOP)	Commercial, 0° to 70°C
CY28510OCT	48-pin Shrunk Small Outline package (SSOP) - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimension

48-Lead Shrunk Small Outline Package O48



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